Design of Virtex-7 FPGA based Data Communication Device.

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***Abstract*- CSIR-NAL has built India's first parallel computer, Flosolver Mk1 in 1986. The current Flosolver Mk8 is a 1024 processors, 10 Tera FLOPS parallel computing system, based on cluster approach for multitasking. Each cluster has multiple processing elements. These processing elements communicate with other through an indigenously developed switch called "FloSwitch". This customized, re-configurable FloSwitch has its own data processing capability along with data passing and can perform read and write operations simultaneously. Currently FloSwitch is based on Virtex-5 Field Programmable Gate Array (FPGA) with 16 optical channels working at 3.125 Gbps per channel per direction. This paper presents a Virtex-7 FPGA based FloSwitch design which aim is to provide high speed serial connectivity of 28.05 Gbps per channel per direction. The design is carried out in OrCAD tool.**

***Keywords*- FloSwitch, Virtex-7 FPGA, OrCAD, optical transceivers, processing elements.**

I. INTRODUCTION

The Flosolver project was started in the year 1986, when the computational fluid dynamists at National Aerospace Laboratories (NAL) were starving for computing power due the restrictions imposed on importing powerful computers to the country. As an indigenous solution to this the Flosolver project was started with the objective to design, fabricate and develop parallel computers, an emerging technology then, for use in fluid dynamical and aero dynamical problems and hence the generic name Flosolver. Thus the **first parallel computer of India, Flosolver Mk1,** was built in 1986 [3]. The current Flosolver Mk8 is customized parallel supercomputer for numerical weather prediction using in-house developed communication devices under New Millennium Indian Technology Leadership Initiative (NMITLI) program of Council of Scientific and Industrial Research (CSIR), consisting of 10 Tera FLOPS, 1024 processors. The Flosolver Mk8 is based on 2.5 GHz Intel Xeon processors with 8 GB RAM, 500 GB HDD per processing elements, where Xeon processors act as processing elements.

Flosolver series of supercomputers are based on cluster approach for parallel computation [4]. A cluster is a type of parallel/ distributed processing architecture consisting of a set of interconnected computers that can work in a single machine. The Flosolver Mk8 is organized as clusters of 128 modules. These 128 modules are interconnected to form a 1024 processor system. The entire computational task is distributed equally among all the clusters. Each cluster will be having multiple processing elements; task assigned to cluster will be distributed between the processing elements. In Mk8 supercomputer, each cluster is having 8 processing elements. These processing elements communicate with each other through an indigenously developed switch called FloSwitch.

The salient feature of FloSwitch is that it has its own data processing capability [1] along with data passing and can perform parallel read and write operations. This customized, re-configurable FloSwitch is developed for integrated local and global communication. Current FloSwitch is based on Virtex-5 Field Programmable Gate Array (FPGA) with 16 optical channels working at 3.125 Gbps per channel per direction. Optical Fiber interconnects provide a flexible, wide- bandwidth transmission medium for a scalable parallel computing system [2].

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In the proposed work FloSwitch is based on Virtex-7 FPGA, optimized for high speed serial connectivity. The high speed serial connectivity is obtained from built- in multi-gigabit transceivers working at 28.05 Gbps per channel per direction.

II. DESCRIPTION

In the parallel machines connectivity plays a major role. In Flosolver Mk8 parallel computing system, the processing elements communicate with each other through customized hardware switch called FloSwitch. FloSwitch supports both data passing and data processing mechanism.

The Flosolver Mk8 consists of 128 clusters; these 128 clusters are connected through an optical link to form a 1024 processor system [4].

A. Existing Work

In the existing work the customized, re-configurable FloSwitch is based on Virtex- 5 FPGA [5]. It is built for integrated local and global communication. The current FloSwitch consists of four 64- bit parallel interfaces and 16 optical channels. Each parallel interface delivers a throughput of 512 MBps. Each optical channel is full duplex and delivers a throughput of 3.125 Gbps.

B. Proposed Work

In the proposed work FloSwitch is based on Virtex-7 FPGA which provides high speed serial connectivity. Virtex-7 based FPGA are optimized for highest system performance and capacity with a 2X improvement in system performance. Virtex-7 HT device has 16 GTZ serial Input/ Output (I/O's) working in full duplex mode. Each transceiver delivers a throughput 28.05 Gbps per direction [6]. The main aim of this work is to have a high speed serial link across the processing elements.

III. IMPLEMENTATION

In the proposed work the Virtex- 7 FPGA based FloSwitch is designed. FloSwitch is a communication switch which is capable of information processing while information passing and can perform parallel read and write operations simultaneously.

Virtex-7 FPGA supports 16 serial I/O's which operate up to 28.05 Gbps per channel per direction. Fig. 1 shows the proposed block diagram of Virtex-7 FPGA based Communication device. GTZ serial I/O's, which perform serial- to- parallel and parallel- to- serial conversion, are connected to C form- factor (CFP2) optical module which in turn are connected to optical link. The power module generates different voltages for different components.

GTZ transceiver is a serializer and deserializer (SerDes) which performs serial- to- parallel and parallel- to-serial conversion [6]. The parallel data from user logic in FPGA is converted to serial data by GTZ transceiver which is called high speed serial I/O. This serial data is fed to CFP2 optical module. The optical module converts the electrical signal to optical signal and is fed to the external optical link. During reception the optical signal is converted back to electrical signal by CFP2 and is given to GTZ transceiver. The serial data is converted to parallel data by GTZ and given back to user logic. The Virtex-7 FPGA stores its customized configuration in the SPROM internal latches.

Each GTZ transceiver has large number of user definable features and parameters. The GTZ transceivers use a single LC tank architecture to allow the ideal blend of flexibility and performance. The serial transmitter and receiver are independent circuits that use an advanced Phase- locked Loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers up to 100 to become bit- serial data clock of 28.05 Gbps. Virtex-7 FPGA is designed to work with CFP2 optical module. The CFP2 module is a hot pluggable form factor for optical networking applications. The optical connection can support 4×25 Gbps links/ interfaces [7].

Virtex-7 FPGA provides highest system performance and provides ultra high speed serial connectivity delivering peak bandwidth of 2.802 Tbps [8]. Highest capability devices in Virtex-7 series FPGA is enabled by Stacked Silicon Interconnect (SSI). They are designed for high performance and lowest power with

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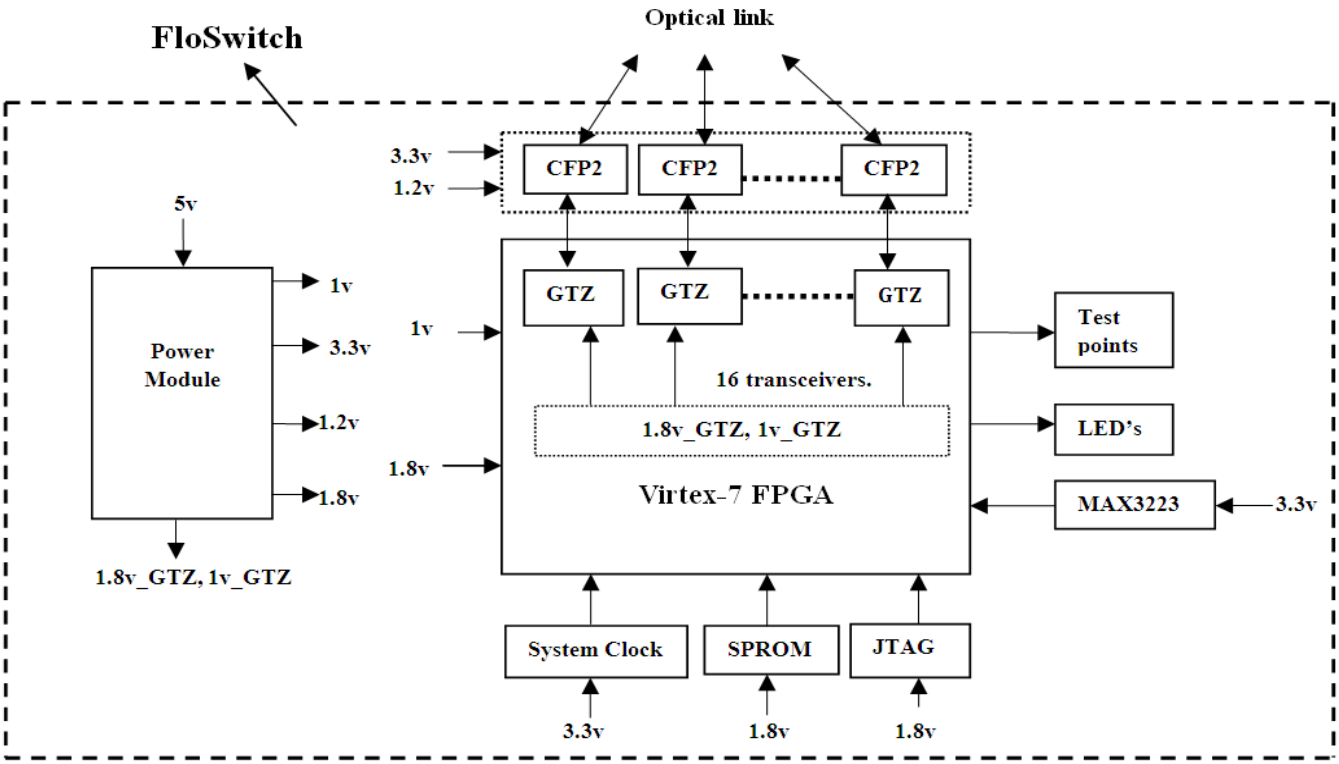

Fig. 1- Block diagram of Virtex-7 FPGA based Data Communication device.

28nm, HKGM, HPL process, 1V core voltage process technology and .9V voltage option for lower power. Input output voltages can range from 1.2V to 3.3V. Virtex-7 FPGA includes 2 million logic cells.

The Serial Peripheral Interface (SPI) flash is used as configuration memory for Xilinx Viretx-7 FPGA. The SPI flash can be directly connected to FPGA, and the FPGA's internal connection logic reads the bit stream out of Flash and configures itself. The FPGA automatically detects the bus width on the fly, eliminating the need for any external control or switches. The Joint Test Action Group (JTAG) is used for programming, debug, probing port and boundary scan testing.

Power module provides high-performance step-down conversion from a 5V input bus voltage. Virtex-7 FPGA requires different voltages like 1.8v, 1v and other peripherals require 3.3v, 1.2v. Hence the power regulator generates different voltages by changing the value of resistor. To generate 1.8v and 1v voltages required for 16 transceivers of Virtex- 7 FPGA separate voltage regulator is used which provides linear start- up time.

The clocking system synchronizes the movement and processing of data through the different modules in the system. The clock management of Virtex-7 series FPGA includes high speed buffers, frequency synthesizing and phase shifting capabilities. The fastest clock in the design will determine the clock rate that the FPGA must be able to handle. The maximum clock rate is determined by the propagation time. Suitable crystal oscillator is used to generate the clock frequency. Two clock frequencies are used in this design; one is for user logic and the other for serial I/O's. Test- points and LED's are used in testing and debugging mechanisms.

The library creation and schematic design is done using OrCAD tool and the Design Rule Check (DRC) is done for any error in the schematic design.

OrCAD is a suite of tools from Cadence Company for the design and layout of printed circuit boards (PCBs). OrCAD offers a total solution for core design tasks schematic and VHDL- based design entry.

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IV. CONCLUSION

The FloSwitch, developed by Flosolver division of CSIR- NAL, is a data communication device for parallel computers. The unique feature of this customized, re-configurable switch is that it can perform information processing while information passing. In this paper a Virtex- 7 FPGA based FloSwitch is presented which will provide high speed serial connectivity. The built- in multi-gigabit transceivers (GTZ) of Virtex- 7 FPGA operates up to 28.05 Gbps per channel per direction delivering a peak bandwidth of 2.802 Tbps. Hence the Virtex- 7 FPGA based FloSwitch design will improve the serial connectivity speed.

V. FUTURE SCOPE

In this paper a Virtex- 7 FPGA based FloSwitch is designed with 16 optical channels each operating up to 28.05 Gbps per direction. A FPGA with more number of channels and delivering higher line rate can be used in designing FloSwitch in future.

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