HIGH ACCURACY FIXED WIDTH BOOTH MUTIPLIER BASED ON MULTILEVEL CONDITIONAL PROBABILITY

Ms.M.Logeshwari
M.E (VLSI),dept of ECE
VCEW
Elayampalayam,India

Mrs.S.Thilakavathi
Assistant professor,dept of ECE
VCEW
Elayampalayam,India

ABSTRACT: This paper describes about reducing truncation error,that occurs in fixed width booth multiplier designs.Fixed width booth multiplier compensates the truncation error using multilevel conditional probability estimator.Compared with existing simulation methods,proposed MLCP method reduces the simulation time and increase accuracy adjustment based on mathematical derivations.the proposed MLCP method follows entire nonzero code to achieve high accuracy and to estimate truncation error .The result of fixed with booth multiplier with MLCP technique is high accuracy with low cost.

Index terms;Multilevel conditinal probability, truncation error,fixed width booth multiplier.

I Introduction;

MULTIPLICATION is one of the most area consuming arithmetic operations in high performance circuits. Fixed width multiplier takes n number of inputs and it produces n number of outputs. Combination of fixed multiplier and post truncated multiplier which truncates half of LSBs produces its result after calculating all the products and gives high accuracy but it takes large circuit area .Direct truncated multiplier with fixed width multiplier truncates half LSBs product directly to

ISSN: 2278 – 909X

reduce circuit area but it produces truncation error. Compensated circuit has been developed in this paper to get balance between accuracy and circuit area.

In earlier adaptive conditional probability estimator was used to improve accuracy,it uses single nonzero code to calculate the truncation errors whereas the MLCP method employing all nonzero code to estimate truncation error.The compensated circuit will respond quickly,produces a closed form with various bitwidths L and column information w.Thus accuracy can be adjusted by changing column information.

II Related work;

To reduce truncation error various error compensatoin methods are used.

A.Full width multiplier

Full width multiplier produces an output whose number of bit is doubled accorance with the input operands.We have to avoid data widening for that it is necessary to compute fixed width multiplier.

B.Linear regression analysis

In fixed width modified booth multipliers,they slightly modified the partial products, this produces tiny mean square error 12.3%.Compensation value has been derived using statistical analysis,this reduces the mean error and truncated error but maximum absolute error is still large.

C.Adaptive technique

In this metod rounding and reduction errors are compensated with fixed bias,where a variable correction is employed to reduce the output error. In many applications, such as function evaluation the maximum absolute error is considered, In these cases, the computational accuracy of every hardware component, including multipliers, is accurately controlled so that the total computation error meets the final target precision.But MAE is not an average quantity,it depends on point to point behavior of multiplier,it makes the analysis much more difficult.Computational complexity increases.

PROPOSED SYSTEM

This system explains about accurcy adjustment fixed width booth multiplier that uses multilevel conditional probability to implement the compensated circuit.

we derive the better error-compensation bias to reduce the truncation

ISSN: 2278 – 909X

error and then construct a lower error fixed-width multiplier, which is area efficient for VLSI implementation

MLCP Estimator

MLCP method produces a closed form with various bitwidth L and column information ω,thus the compensated circuit can be established quickly,and accuracy can be adjusted by changing column information ω.The accuracy is high in MLCP method compare to adaptive conditional probability estimator (ACPE).Although MLCP method has higher complexity to estimate truncation errors when compared with ACPE

Fixed width booth multiplier

Fixed width booth encoding algorithm is mostly used in multiplier designs to reduce the number of partial products.

The partial product array in a booth multiplier for inducing the column information ω, where ω indicates the number of true product columns included in the compensated circuit.

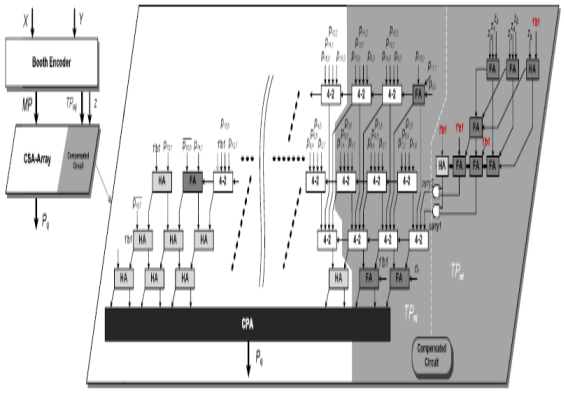
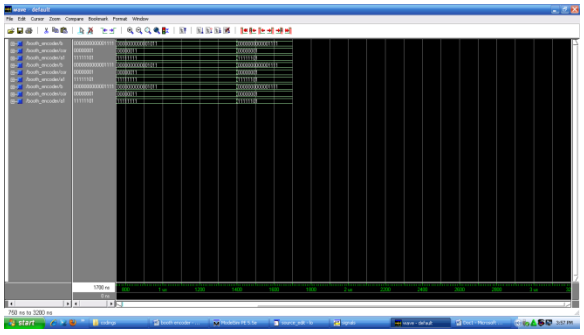


Fig: MLCP circuit

CSA ARRAY

Carry save adder architecture and function of subtracting one is designed by adding all one values for twos complementation representation. The proposed MLCP circuits depend on α, thus, various word lengths L and column information w can use the same MLCP circuit

SIMULATION RESULT



ISSN: 2278 – 909X

III CONCLUSION

This brief estimates the truncation error with high accuracy using MLCP method with the power supply of 1.8V.Therefore MLCP compensated circuit can be used to develop a high accuracy,low cost,and flexible fixed width booth multiplier.

REFERENCES

1.K. K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*. New York, NY, USA: Wiley, 1999.

2.S. N. Tang, J. W. Tsai, and T. Y. Chang, "A 2.4-Gs/s FFT processor for OFDM-based WPAN applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 6, pp. 451–455,jun 2010

3.S. C. Hsia and S. H. Wang, "Shift-register-based data transposition for cost-effective discrete cosine transform," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 6, pp. 725–728, Jun. 2007.

4.Y. H. Chen, T. Y. Chang, and C. Y. Li, "High throughput DA-based DCT with high accuracy error-compensated adder tree," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 4, pp. 709–714,Aprl 2011

5.L. D. Van and C. C. Yang, "Generalized low-error area-efficient fixed- width multipliers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 8, pp. 1608–1619 Aug 2005.

ISSN: 2278 – 909X