MODELLING AND TESTING OF GATE OXIDE SHORTS IN SRAM AND DRAM

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Abstract: **Gate Oxide Shorts has become an dominant failure in MOSFET while designing an IC. This defect will surely affect the yield and reliability of the device and memory. Therefore, A GOS Model that represent the minimum size GOS impacted MOSFET is introduced. First, An 6T SRAM(static random access memory) cell structure is designed and the MOSFET having this defect in SRAM is detected by a test method which results in malfunction of the memory operation.**

Thisr paper proposes a new idea about the 4T DRAM (dynamic random access memory),in which its memory cell structure is designed and its behavior with the GOS defect is analyzed. Comparison of both memory is given based on the power, capacitance change and leakage currents. The simulation is done and corresponding dc and transient characteristics was obtained to represent the GOS impacted MOSFET. The testing in SRAM and DRAM is done by using a test method called DFT write test method that can effectively detect the GOS defect.

Keywords: **Defect modeling, DRAM, Gate oxide short, SRAM, Testing.**

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I.INTRODUCTION

Gate oxide short(GOS) is a defect that occur in MOSFET that cause a low impedance between the gate and source, drain or substrate of a MOS transistor. It is the defect that occur at the gate insulator of

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a MOSFET. Among the wide set of possible failure mechanisms in IC's, the breakdown of gate oxide is the dominant failure. The GOS will slowly degrade the quality of an IC which produce low yield. To improve the reliability or yield, testing of gate oxide shorts are required especially in memories. Semiconductor memories are designed based on arrays that store the digital information which are applicable to all digital systems. The root cause of a GOS defect include the oxide rupturing induced by voltage stress, lithographic particles, deviation of oxide growing or unexpected large tunneling leakage. The GOS defect is classified into2 types: i) gate-to-source/drain GOS ii) gate-to-channel GOS. In the previous work, the testing is done in SRAM cell structure during write operation in which the GOS defect in a MOS is detected using a test method. Its power consumption, dc ,transient and cv characteristics was obtained. In the proposed work, a DRAM cell structure is used and a GOS defect in MOS is analyzed. Comparison of both the memory is provided.

II. GATE OXIDE SHORTS AND CIRCUIT LEVEL MODELS

The GOS defect will form a low impedance path from the gate to source, which may result from a pinhole of gate oxide locating in between the gate and the source. Therefore, it can be modeled as a resistive short between the gate and source of the MOSFET. The gate-to-channel GOS forms a low impedance path from the gate to channel, which is found as a pinhole. In a MOSFET, the gate-to-channel GOS exists as: i)Its gate current is exponentially proportional to its gate voltage. ii)Negative I_D exists.iii)The resistance between the gate and the source/drain is voltage controlled. The detection of GOS is possible if the behaviour at the circuit level caused by defective transistors is known. A MOSFET with GOS may show gate currents some orders of magnitude beyond the nominal values depending upon the device biasing.

Several circuit level model for gate to channel GOS was studied. 1) the bi-dimensional model 2)the split model 3) the non linear split model. The GOS models are used to effectively estimate the GOS defect. The circuit level model is then used to fit the dc and transient characteristics. If any GOS defect present, the characteristics show the negative drain current when the gate voltage is low.

The bi-dimensional model consists of a mutually connected MOSFET array and hence, requires high computation time during simulation. It cannot produce the

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minimum size MOSFET. The split model simplifies the complexity of the bi-dimensional model by splitting of the MOSFET into two serially connected MOSFETs and adding the resistor in the middle. This model cannot represent the minimum size MOSFET. This model only fits the DC characteristics and not the transient characteristics. The nonlinear non split model can represent the minimum size MOSFET by using only one MOSFET in between the source and drain while adding other MOSFETs, current sources, resistors on the other side. This also fails to represent the transient characteristics. Therefore we represent a GOS MODEL in this paper that fit the transient and dc characteristics.

A GOS MODEL:

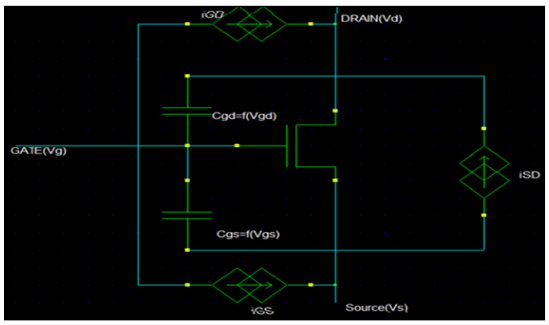

Figure 1: A GOS MODEL

The GOS model consists of 3 current source and 2 voltage controlled capacitors. Hence, the current sources are used to effectively fit the DC characteristics and the voltage controlled capacitors are used to represent the transient characteristics . In addition to this, we also obtain the CV simulation characteristics to represent the capacitance characteristics.

III. 6T SRAM MEMORY CELL

SRAM is a volatile memory because the data stored in the memory is maintained only when the power is applied continuously. An SRAM contains matrix of cells and address decoding functions.

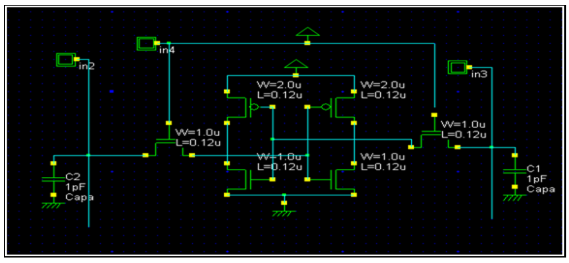

Figure 2: An SRAM CELL

It consists of 2 pass gate NMOS and 2 coupled invereters. SRAM operation: When a write operation is performed, the word line is high and the bitline and the bitline bar is raised to V_{DD} or GND. During the read operation, the corresponding data is placed at the memory cell at the pair of inverters.

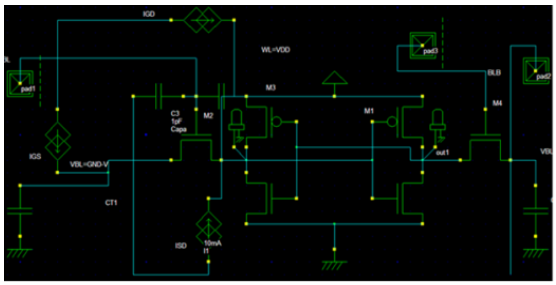

Figure 3: GOS at the pass gate NMOS

Assume the GOS occur in the pass gate NMOS, the data written is stored as the

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complelent or wrongly. If '0'written means '1' gets stored.

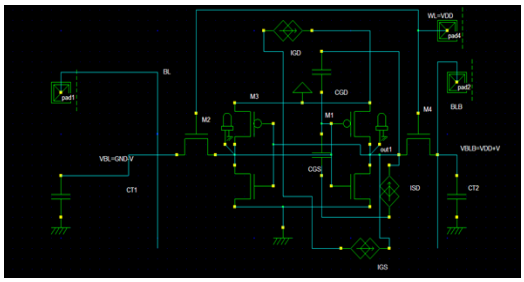

Figure 4: GOS at the PMOS transistor

Assume the GOS occur at the PMOS, whatever data written will not be stored at the memory cell. Therefore, we find a GOS defect at the PMOS.

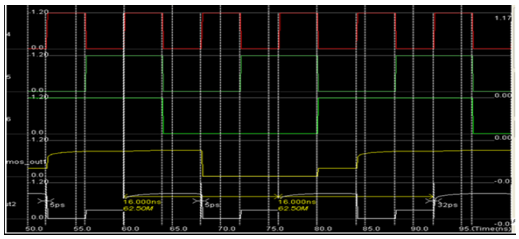

Figure 5:Transient response of an SRAM

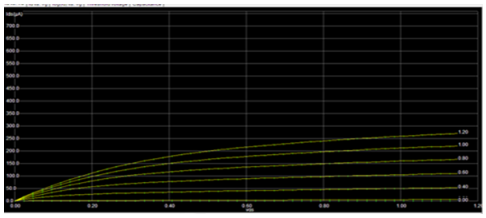

Figure 6: DCcharacteristics of an SRAM.

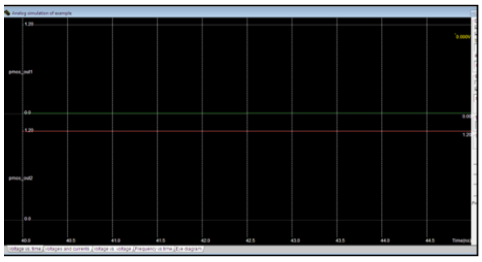

Figure 7: Transient response of a Defected SRAM

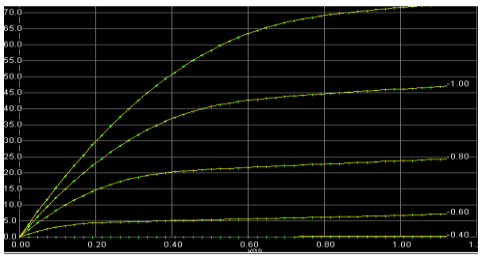

Figure 8: DC characteristics of a defected SRAM

Table 1: Results of SRAM:

Parameters	**Pure SRAM**	**NMOS defect**	**PMOS defect**
Power	4nW	6nW	6nW
DC	350uA	40uA	40uA
Transient	0.28V	1.20V	1.20V
(C_T, ΔV)	(9fF, 0.8V)	(1.5fF, 0.8V)	(1.5fF, 0.8V)

From the simulation results,

Vdd =1.2 v

At nmos(CT,ΔV)=(1.5fF,0.8V)

At pmos(CT,ΔV)=(1.5fF,0.8V)

Therefore , the tolerable range Δv range is 0.8V and the capacitor ocupied Area is 1.42um^2.

IV. 4T DRAM MEMORY CELL

When a capacitor is used to store the data in a RAM, The charge on the capacitor should be refreshed periodically to eliminate leakage current. This capacitor charged mechanism is known as DRAMs(dynamic random access memory). Whatever input we

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give, the data will not get stored at the pair of inverters. The output remain in the high impedance state. The DRAM cell design consists of 4 transistors. A read transistor and a write transistor. The data will stored in DRAM as a "charge" at the capacitance connected with a transistor structure.

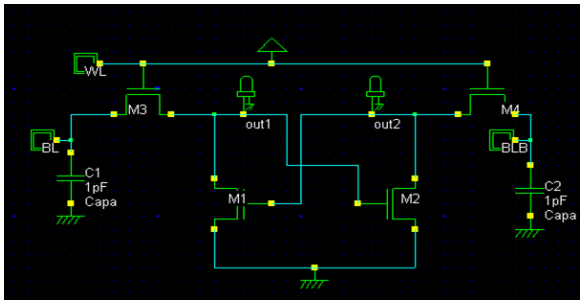

Figure 9: 4T DRAM memory cell

There is no current path to the storage node for restoring the data, hence data is lost due to leakage with the period of time.

DRAM operation: read and write operation is performed when M3 and M4 is ON. The read and write operation is performed only when the word line is in active condition.

i)During write '1' operation: WL-> HIGH,M3 and M4 will be ON. M1 OFF. At final state, V1=1, V2=0 ii)Read '1' operation: WL-> HIGH, M3 and M4 will be ON. M1 OFF . Vc>Vc read as a logic 1.iii)Write '0' operation: WL->HIGH, M3 and M4 ON. M2 OFF. At final state, V2=1,V1=0.iv)Read '0' opearation: WL->HIGH, M3 and M4 ON.M2 OFF. Vc<Vc read as a logic '0'.

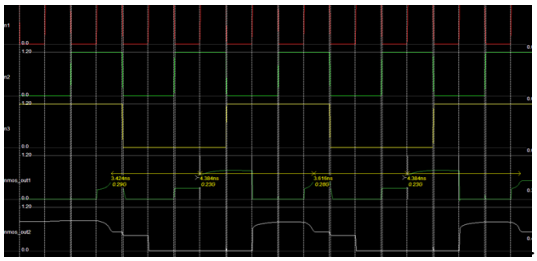

Figure10:Defected DRAM transient response

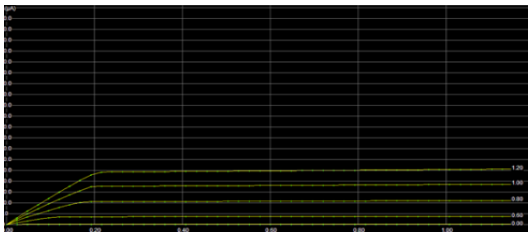

Figure11: DC characterisitics of defected DRAM

Table 2: Results of DRAM

Parameters	DRAM	DRAM With Nmos Defect
Power	1nW	0.76v
Dc	2.3mA	0.5Ma
Transient	0.3v	0.80v
(Capacitance,V)	(4fF,0.8v)	(0.4fF,0.4v)

V .CONCLUSION

In this paper, the GOS model is used to fit the dc characteristics that represent the minimum size GOS impacted MOSFET. Additionally, transient characteristics was also obtained that represents the capacitance change of the GOS impacted MOSFET**.** Using the DFT write test method, the testing

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is done in SRAM cell. Hence, the capacitor occupied area is calculated. Based on the tolerable ΔV range, GOS defect is detected. The proposed work is considered by detecting the GOS defect in DRAM memory cell by using the GOS model and the DFT write test method. When compared to SRAM, DRAM has low dc characteristics and transient charcetrsitics. Capacitance change is also very low. Hence, DRAM consumes less power when compared to SRAM.

REFERENCES

[1] J. Segura and A. Rubio, "A detailed analysis of CMOS SRAM's with gate oxide short defects" IEEE J. Solid-State Circuits, vol. 32, no. 10,Oct. 1997.

[2] X. Lu, Z. Li, W. Qiu, D. M. H. Walker, and W. Shi, "A circuit level fault model for resistive shorts of MOS gate oxide," in Proc. Fibres Opt.Passive Compon., 2005.

[3] Laxmi Singh,Ajay Somkuwar, "4T DRAM based on self-controllable voltage level technique for low leakage power in VLSI."

[4] M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Ohbayashi, Y. Nakase, andH. Shinohara, "A 45 nm 0.6 V cross-point 8T SRAM with negative biased read/write assist," in Proc. Symp. VLSI Circuits, Jun. 2009.

[5] A. Chehab, A. Kayssi, and A. Ghandour, "Transient current testing of gate-oxide shorts in CMOS," in Proc. Int. Design Test Workshop,Dec. 2007.

[6] S. A. Kumar, R. Z. Makki, and D. M. Binkley, "IDDT testing of embedded CMOS SRAMs," in Proc. Design, Autom. Test Eur. Conf.Exhibit., 2002.

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