Low Leakage High Speed Domino Circuit For Wide Fan-in Equality Comparator

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Abstract— Digital Comparator is important in the combinational logic circuit. Digital or Binary Comparators are made up from standard AND, NOR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs. In this paper, 256-bit a new comparator using different domino circuit for wide fan-in applications in ultra-deep sub micrometer technologies is proposed. In this paper, a new technique called current comparison domino circuit is used to design a comparator circuit by using XOR gate. The novelty of the proposed circuit is that our work simultaneously increases performance and decreases leakage power consumption. The proposed technique decreases delay at the output node and improve noise immunity. Simulation result of comparator circuits designed using a 14nm high performance predictive technology model.

Index Terms— Domino logic, comparator, leakage power, power consumption, noise immunity.

I. INTRODUCTION

Dynamic logic gates and circuits have been excellent choice in the design of high-performance modules such as multiple bit adders, subtractors, multipliers, comparators, multiplexers, registers, etc in modern VLSI microprocessors. The advancement in fabrication technology along with the shrinking device size has allowed for placement of nearly two billion transistors on Intel's latest processor . The digital logic gates and circuits designed using dynamic domino technique is considerably faster than the logic gates and circuits designed with standard static logic style. The aggressive technology scaling to i.mprove the performance as well as the integration level makes the noise play a major role in design parameters like area, power and speed . Therefore the digital integrated circuit noise has become one of the most important issues in the design of deep submicron VLSI chips . The robustness and performance of wide fan-in dynamic circuits significantly degrade with increasing levels of process variations and sub threshold leakage.

A number of design techniques such as PMOS feedback keeper transistor method to prevent the dynamic node floating problem, precharging the internal nodes to eliminate the charge sharing problem and weak complementary p-network is constructed to improve the noise tolerance to the level of skewed static CMOS logic gates, have been developed in the past three decades to minimize the effect of noise in dynamic circuits. It is also shown that voltage scaling aggravates the crosstalk noise in the dynamic circuits and reduces circuit noise immunity, motivating the need for noise-tolerant circuit design. To design a high performance domino logic circuit, there are two most important factors to be considered when designing a keeper circuit. The first factor is the additional loading caused by the keeper and its control circuits and the second factor is the keeper circuit should be capable of switching off very fast. If the keeper circuit remains ON during evaluation it will compete for longer time with the NMOS network during the pull down process. Designing feedback keeper circuit for wide fan-in gates is a challenging task since the leakage current largely depends on increase in variability .

In this paper, a comparator circuit is designed using a current comparison domino technique that enables faster switching and tracks the variation across different process corners. In this paper the effect of temperature on the circuit performance is analyzed in detail by sweeping the temperature from 25^0C to 70^0C.

The performance of the dynamic circuits can be significantly improved by precise design and properly sizing the transistors. Usually in all the digital circuits the transistor gate length remains uniform. So the size of the transistor in digital circuits depends on the width of the transistor. In this paper the multiple bit domino comparator circuit is implemented with L=14nm technology along with a supply voltage of 0.7V. The noise sensitivity of the domino circuits depends on the threshold voltage of the transistors used in the circuit and since the transistor size is decreasing year by year due to aggressive scaling trends in modern electrons, due to the low threshold voltage, the circuits should be more sensitive to noise that necessitates the use of noise tolerant circuits design techniques.

1.1 CIRCUIT DESIGN

The circuit diagram of a wide fan-in comparator circuit implemented using current comparison based domino (CCD) technique is shown in fig.1. The wide fan-in comparator circuit implemented using current comparison based domino (CCD) technique uses a current mirror to replicate the leakage current of the pull-up network and it tracks process, voltage, and temperature.

The timing diagram of a 256bit wide fan-in comparator is shown in Fig.2. The timing diagram shows output of the circuit. From this timing waveform, we know that CCD circuit must operate in two phases, predischarge phase and evaluation phase. During the predischage phases clk=0. So dynamic node is fully discharged. So we get output as high.

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During evaluation phase clk=1. It has two state. First state, all inputs are high. When all inputs are high, it has some leakage current in its dynamic node. It can be eliminated using reference current circuit. In second state, one of the input flows to low. It cause dynamic node to charged fully to Vdd. So we get output as low.

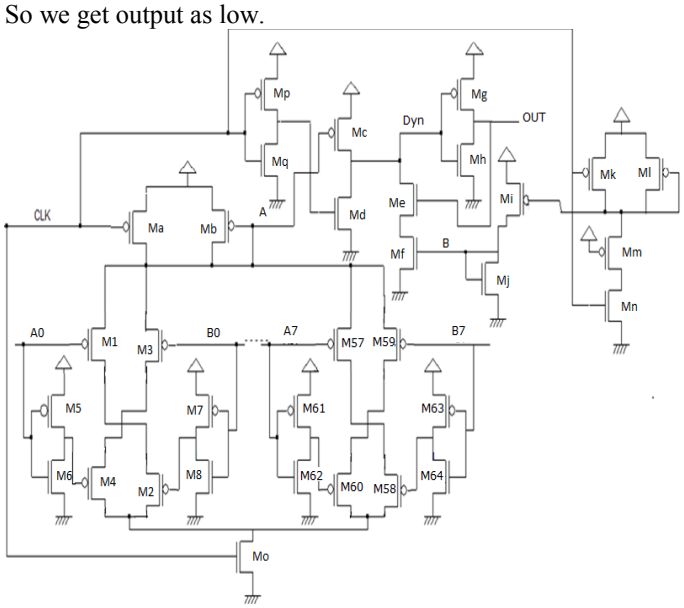

Fig.1 CCD based Comparator

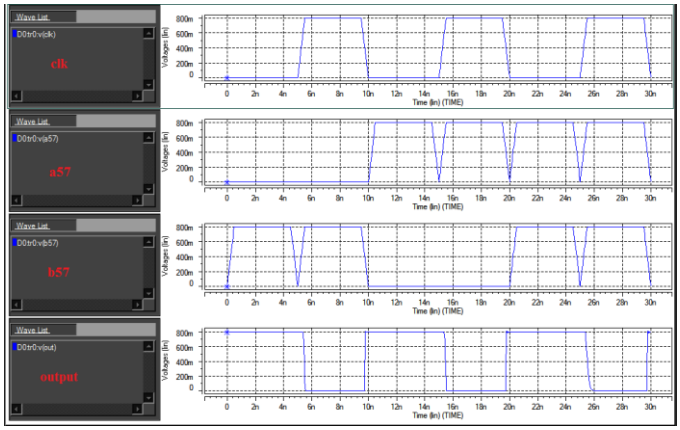

Fig.2 Timing Diagram

The Fig.3 shows, delay of 256-bit comparator using CCD technique. Delay varies depends on the temperature. Temperature is main component of circuit. When the temperature increases gradually, delay of the circuit increases. Because circuit get minimum amount of power. But here the delay is reduced by reducing leakage current.

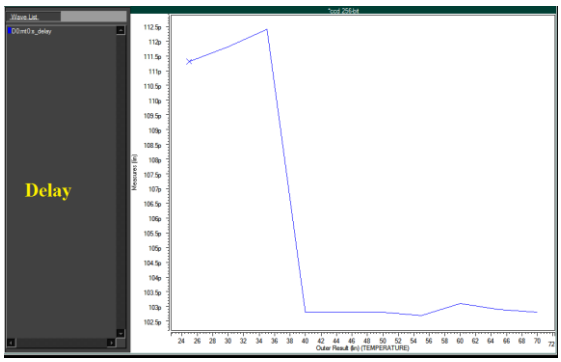

Fig.3 Delay Vs Temperature

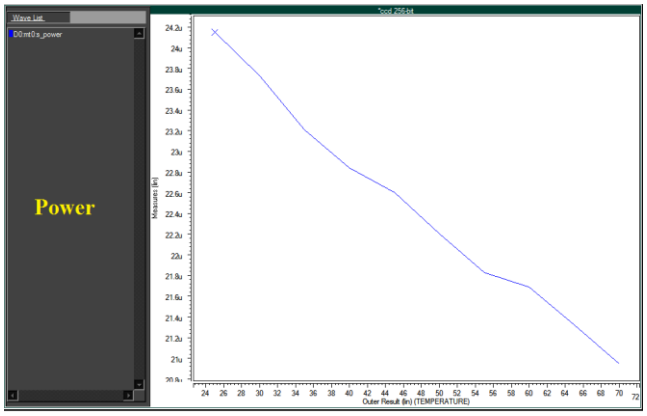

Fig.4 Power Vs Temperature

The Fig.4 shows effect of temperature on the power consumption of the circuit. When temperature increases, power of the circuit decreases. So the circuit performance get reduced.

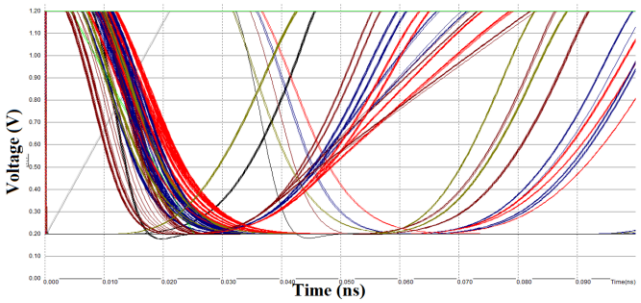

Fig.5 Voltage Vs Time waveforms of 256-bit wide fan-in comparator using CCD

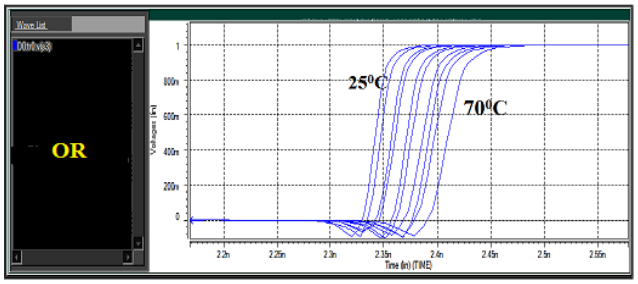

Fig.6 Effect of temperature on the performance of 256-bit Comparator using CCD

The output voltage Vs Time characteristic of the 256-bit wide fan-in OR gate is shown in Fig.5. This eye diagram shows the precharing and evaluation of the circuit. In this wide fan-in comparator circuit a current mirror is connected to the keeper which compensates for the sub threshold leakage current of the pull-down network. This current mirror circuit can be shared for all the logic gates in the circuit. In this configuration the keeper and current mirror circuit minimizes the delay of the circuit (delay in the order of pico seconds) by minimizing the effect of charge sharing. This circuit need proper selection of clock signal. If the clock frequency exceeds 500MHz, the performance of the 64-bit wide fan-in comparator circuit degrades. The effect of temperature on the performance of 64-bit wide fan-in comparator circuit is

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shown in Fig.6. In this work the temperature is varied from 25^0C to 70^0C. From the Fig.6 it is clear that as the temperature increases the transition delay also increases due to the increase in leakage current. The circuit is implemented using L=14nm technology with V_{DD}=0.7V.

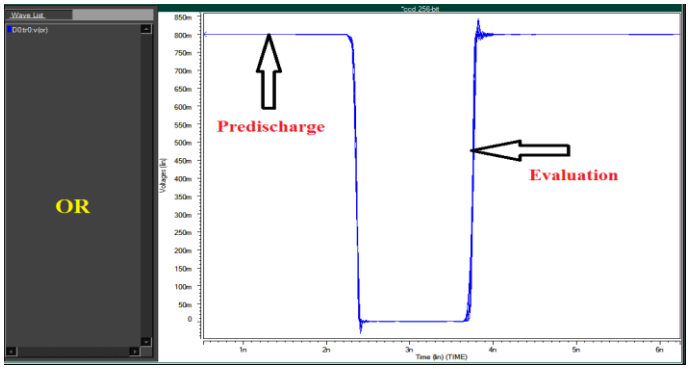

Fig.7 Voltage Vs Time waveforms of 64-bit wide fan-in comparator using CCD

The pre-charge and evaluation phases of the comparator(output) of a 256-bit wide fan-in comparator circuit designed using CCD technique is shown in Fig.7. As the clock frequency increases the output voltage decreases due to the parasitic capacitances. The operation of the circuit is as follows. When clock goes low, the dynamic node will be predischarged to V_{DD} (predischarge phase) and the output remains high in this condition. When the clock signal changes the state from low to high the circuit evaluate the logic function (evaluation phase) and the output remains low.

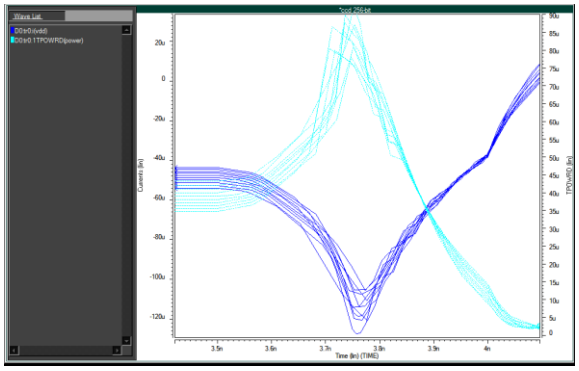

Fig.8 Power Vs Time waveforms of 256-bit wide fan-in comparator using CCD

In Fig.8, the Power Vs Time waveform of 256-bit wide fan-in comparator is shown. When Power is zero, the current is also zero. That means the circuit is in OFF state. When the circuit consumes small amount of power, the current in the circuit is also increases. The current is in negative because PMOS is operate in reverse biased region. The PMOs is operate in negative voltage only. That's why the circuit has negative current.

In this paper 256-bit wide fan-in comparator is presented with L=14nm technology and with a supply voltage of 0.7V. These high performance domino styles improve the scalability of multiple bit domino logic gates. Using these method it is possible to implement the wide fan-in circuits with a transistor gate length of L=14nm along with a supply voltage of 0.7V. These wide fan-in circuits are superior in performance compared to conventional static logic wide fan-in OR and AND gates. These circuits minimize the chip area, minimize the leakage power, and improve the noise tolerance without much speed degradation. Also the delay between the gates is now reduced to the order of pico seconds. These types of domino logic circuits can be used in high performance microprocessors.

2. SIMULATION RESULTS

The simulations were performed using L=14nm technology along with the supply voltage V_{DD}=0.7V. In this paper a 64-bit comparator circuit is constructed using current comparison domino technique. Since a single current mirror structure can be shared among more than one domino logic circuits, the CCD technique is useful for constructing wide fan-in circuits such as multiple bit adders, registers, multiplexers etc. This comparator circuit has the area overhead of an extra NMOS transistor which is connected to the keeper from the current mirror circuit. This comparator circuit has much better noise margin, low leakage current and low power consumption

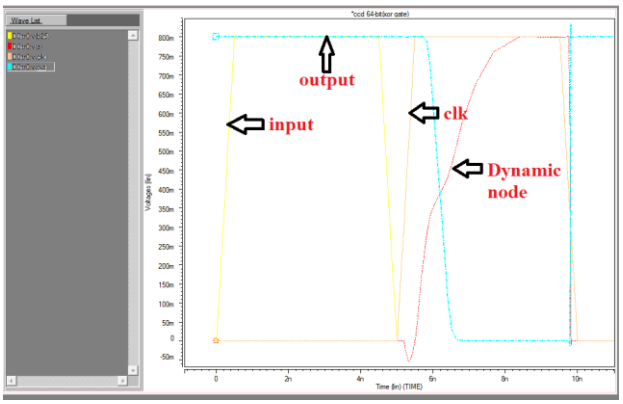

Fig.9 Simulation Result

3.CONCLUSION

As the technology scales down, the leakage current of the pull down evaluation network increases, especially in wide fan in dynamic gates. They are used in microprocessors. This will increase the power consumption and reduce the noise immunity. In this paper the performance of 256-bit wide fan-in comparator circuit is designed using CCD circuit technique. The 256-bit wide fan-in comparator circuit is simulated using L=14nm technology along with supply voltage V_{DD}=0.7V. The experimental results shows that these wide fan in comparator circuit gives superior performance.

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