QDR SRAM DESIGN USING MULTI-BIT FLIP-FLOP

M.Ananthi, C.Sathish Kumar

ABSTRACT:

In memory devices the most important factor is power consumption. Because the power consumption of the memory device increases means, the device reliability and life time is reduced. By using the array of flip-flops the SRAM is designed. The clock network of the flip-flop consumes more power. To reduce this power, the Single-Bit Flip-Flop (SBFF) is replaced by Multi-Bit Flip-Flop (MBFF). While designing the memory by using SBFF means it consumes more power. So MBFF is used to design the memory. The general type of SRAM performs a single operation (Read or Write) in each clock pulse, depending on its control signal. To overcome this limitation, QDR SRAM is designed. It has many real time applications like high speed communications, military applications, etc. In here QDR SRAM is designed by using MBFF.

Keywords: Single-Bit Flip-Flop, Multi-Bit Flip-Flop, QDR SRAM.

Manuscript received on March 20, 2015.

M.Ananthi,*ME(VLSI Design),Srinivasan Engineering college, perambalur, India.*

C.SathishKumar, Assistant Professor, Srinivasan Engineering college, Perambalur, India.

1. INTRODUCTION

In memories the power consumption is one of the major problems. To optimize the power consumption many techniques are proposed. Multi-Bit Flip-Flop is one of the main technique to minimize the clock network power[10]. The Multi-Bit Flip-Flop does not reduce the number of flip-flops, it only reduces the number of inverters in clock networks.

Memory is classified as Random access memory (RAM) and Read only memory (ROM). Compare to ROM, RAM is the fastest access memory. RAM is classified as SRAM and DRAM. By using the flip-flops the SRAM is designed. Depending on feature the SRAM is classified as ZBT, DDR SRAM, QDR SRAM.

2. MULTI-BIT D FLIP-FLOP:

The Single-Bit D Flip-Flop consist one master latch, slave latch and two inverters in clock network. These two inverters consume more power compare to others. To reduce this power consumption the SBFF is replaced by MBFF[8]. Fig.1 shows the 4-bit D flip-flop. It shares the 2 inverters to all flip-flops. So 6 inverters are saved compare to original one.

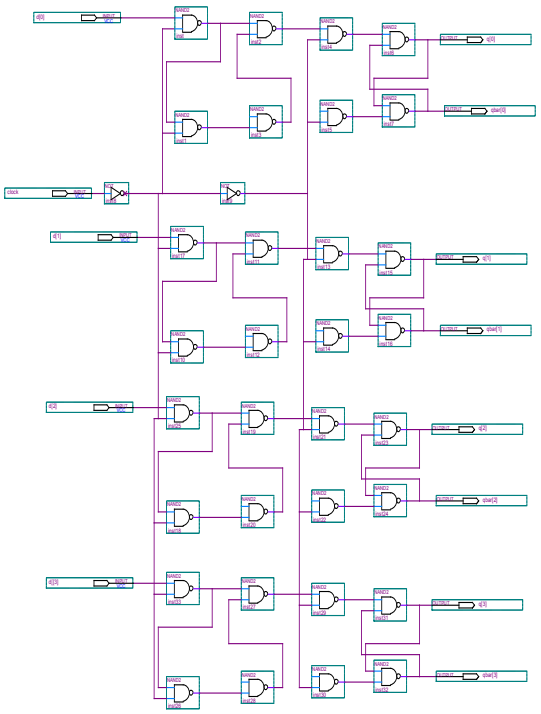

Fig.1. 4-bit D flip-flop

The 4 bit flip-flop has 2 inputs and 1 output. The inputs are data input (d) and clock input (clk) and data output (q). The output for Multi-bit (4-bit) flip-flop is shown in Fig.2.

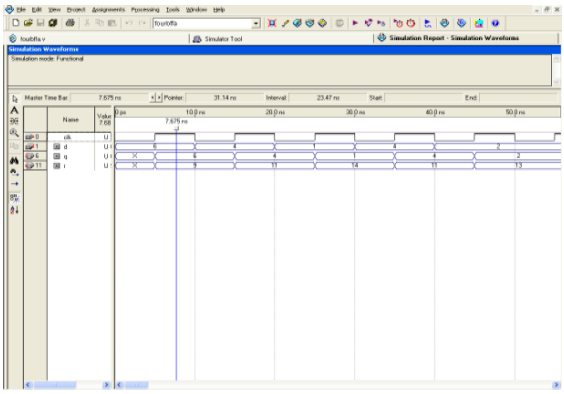

Fig.2. 4-bit flip-flop output

The MBFF has many advantages. That is

i. Area and delay is reduced.
ii. Number of inverters is reduced in clock sinks. So total power consumption is reduced.

3. SRAM:

The data storage in SRAM depends on the d.c source. If the d.c is removed means, the data can be erased. The SRAM is entirely different into DRAM, because DRAM needs refreshing cycle. By using the Multi-Bit Flip-Flops the SRAM is designed. To design 4x4 SRAM, it needs 4 Multi-Bit Flip-Flop. The general SRAM architecture is shown in Fig.3.

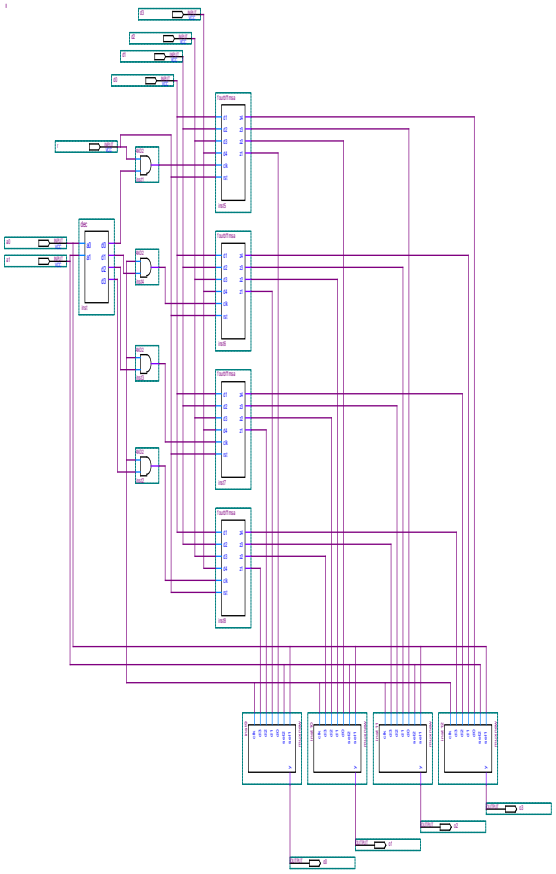

Fig.3. SRAM design using MBFF

The architecture of the SRAM consist one decoder, 4 AND gates, 4 MBFF and 4 multiplexer. It has 4 bit data inputs (d0,d1,d2,d3) and 2 address lines (a0,a1) and one control signal (r). The decoder is used to generate the address lines. By using this address lines the flip-flop is select to write or read the data. The

operation of the SRAM is, when r=0, the write operation is done. When r=1, the read operation is performed. The output for SRAM using MBFF is shown in Fig.4.

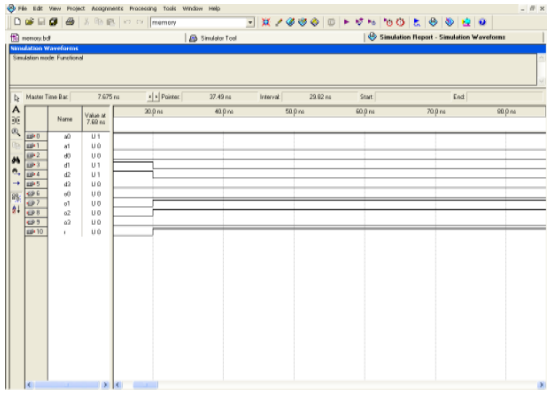

Fig.4. SRAM output

4. QDR SRAM:

This QDR SRAM is designed for high speed communications and networking applications. This technology was introduced by cypress and micron. After that it is followed by IDT then NEC, Samsung, Renesas[7]. In general SRAM any one operation is performed in a single clock pulse. It is the biggest limitation of the general SRAM. Depending on the feature the SRAM is classified as, Zero Bus Turn around (ZBT), synchronous burst (SyncBurst), Double Data Rate (DDR) SRAM, Quad Data Rate (QDR) SRAM. ZBT defines about the latency as zero, in between write and read cycle. SyncBurst is used to increase the write operation. DDR SRAM has double data rate, but it has single read/write port. But the QDR SRAM has separate read/write port with double data rate[6]. By using the SBFF the QDR SRAM is designed. But the SBFF consumes more power because of inverters in clock sinks. So the QDR SRAM is designed by using Multi-Bit Flip-Flop. The QDR SRAM architecture is shown in Fig.5.

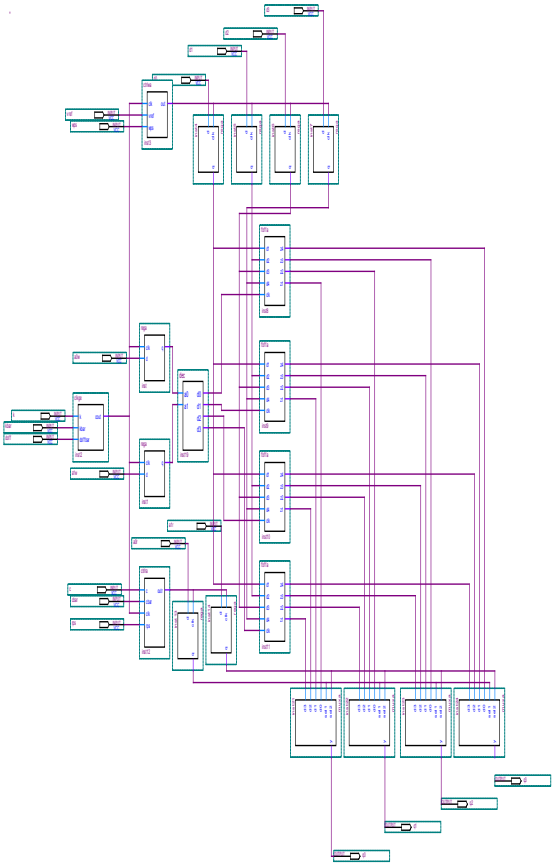

Fig.5. QDR SRAM using MBFF

The architecture consist separate read and write ports. For that it has separate address inputs for Read and Write operation. To control the read and write operation it has two control signals named as RPS and WPS. By using the registers, the data inputs and address lines are connected to the memory array. The memory array is designed by using MBFF. Depending on the control signals the read and write operation is simultaneously performed [5]. The output for QDR SRAM is shown in Fig.6. It performs both read and write operations in simultaneously.

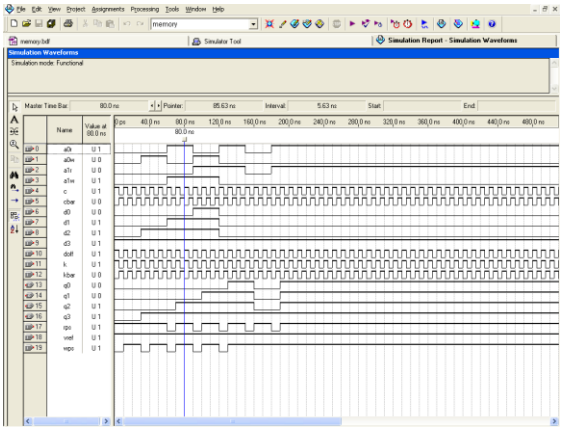

Fig.6. QDR SRAM using MBFF output

5. CONCLUSION

The Single-Bit Flip-Flop consumes more power because of inverters in clock sinks. To reduce this power consumption MBFF is designed. In here Quartus II 8.0 (32 bit) tool is used to design the MBFF and SRAM. Previously, the general SRAM was designed by using both SBFF and MBFF. The SBFF SRAM dissipates the power as 324.16 mW and MBFF SRAM dissipates the power as 323.93 mW. So, 0.23 mW power dissipation is reduced. But it performs a single operation either Read or Write in single clock pulse. To perform both operations, the architecture needs to work in twice. So the power dissipation is also twice from original one. So the QDR SRAM using MBFF architecture is proposed. The QDR SRAM performs simultaneous read and write operation in single clock cycle. So the total power dissipation is reduced 50% of the original one. In future the size of the memory will be increased.

REFERENCES

[1]. An-Chi CHANG. and Ting-Ting HWANG. (2012) 'Synthesis of Multi-Bit Flip-Flops for Clock Power Reduction' Interdisipilinary Information science., Vol 18, pp 145-159.

[2]. G.K.Kharate. (2010) Digital Electronics, Oxford higher education.

[3]. Hiroshi Kawaguchi. and Takayasu Sakurai. (1998) 'A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction' IEEE Journal of Solid-State Circuits., Vol 33, pp 807-811.

[4]. http://www.altera.com/

[5]. http://www.cypress.com/

[6]. http://en.wikipedia.org/wiki/Quad_Data_Rate_SRAM

[7]. http://www.qdrconsortium.org/index.htm

[8]. Lincy.J. and Sivakumar Rajamani.P. (2013) 'Low Power SRAM Design Using Multi-Bit Flip-Flop' International Journal of Technology Enhancement and Emerging Engineering Research., Vol 2, pp 122-125.

[9]. M.Morris Mano (2009) Digital design, third Edition., Pearson prentice hall.

[10]. Mark Po-Hung, Chih-Cheng and Yao-Tsung Chang. (2011) 'Post-Placement Power Optimization with Multi-Bit Flip-flops' IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems., Vol 30, pp 1870-1882.

[11]. Paul E. Gronowski, William J. Bowhill, Ronald P. Preston, Michael K. Gowan and Randy L. Allmon. (1998) 'High-Performance Microprocessor Design' IEEE Journal of Solid-State Circuits., Vol 33, pp 676-686.

[12]. Shao-Huan Wang, Yu-Yi Liang, Tien-Yu Kuo and Wai-Kei Mak. (2012) 'Power-Driven Flip-Flop Merging and Relocation' IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems., pp 180-191

[13]. Ya-Ting Shyu, Jai-Ming Lin, Chun-Po Huang, Cheng-Wu Lin, Ying-Zu Lin and Soon-Jyh Chang. (2013) 'Effective and Efficient Approach for Power Reduction by Using Multi-Bit Flip-Flop' IEEE transactions on Very Large Scale Integration (VLSI) systems' IEEE transactions on Very Large Scale Integration (VLSI) Systems., Vol 21, pp 624-635.

[14]. Yongseok Cheon, Pei-Hsin Ho, Andrew B. Kahng, Sherief Reda, Qinke Wang. (2005) 'Power-Aware Placement' Proc. Design Autom, Conf., pp 795-800.

First Author

M.Ananthi received the Bachelor's degree from Oxford Engineering College Trichy, India and doing Masters degree in VLSI Design at Srinivasan Engineering College Perambalur, India.

Second Author

C.SathishKumar received the Bachelor's degree from Seethai Ammal Engineering College, Sivagangai, India and doing Masters degree in Dhanalakshmi Srinivasan Engineering College Perambalur, India. He is currently an Assistant Professor with the Department of Electronics and Communication Engineering, Srinivasan Engineering college, Perambalur.

