# EDAC by Using Orthogonal Codes

**Reshmi R, Sebin Joseph, Praveen U K**

*Abstract*— **In digital data communication errors will be occurred. The noisy data will change the response of the filters. So the widely used FIR filters have to be protected from errors in many ways. The error detection and correction by using hamming codes is unattractive, because it corrects only single error. So this paper focused on orthogonal codes for Error Detection And Correction (EDAC). Compared to Hamming codes it can correct a large number of errors as the code length varies.**

*Index Terms*— **Antipodal Codes, EDAC, Hamming Codes, Orthogonal Codes.**

## I. INTRODUCTION

In digital communication systems the data is transmitted from a source to the destination .Due to inter symbol interference the digital data will alter .Therefore a bit 0 is received instead of 1.There are different techniques for detecting and correcting the errors. The Hamming codes are a well- known EDAC codes [11]. But it corrects only one bit error. So this paper focused on orthogonal codes to detect and correct the errors [3,4,6].

The conventional techniques don't meet the bandwidth requirements and efficiency. So this paper focused on improving the error detection and correction capabilities of the orthogonal codes. The proposed method has implemented on FPGA kit of Altera Cyclone – II family.

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## II. ORTHOGONAL CODES

Orthogonal codes are binary valued and they have equal number of 1's and 0's.For n-bit orthogonal code has n/2 1's and n/2 0's.that means there are n/2 positions where 1's and 0's differ. Therefore the generation of parity bits are not present in the orthogonal codes. So there is no need of parity calculation compared to other EDAC codes. [3, 7]. The Fig. 1 shows the arrangement of the orthogonal codes. Orthogonal codes have an application in perfectly synchronized environments such as in the forward link of mobile communications. The main reason for using orthogonal code is, it has a zero cross correlation. The cross-correlation value is zero only when there is no offset between the codes[3,6].

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There are several code expansion techniques to generate orthogonal codes. Probably Hadamard transform is the best known technique. A modified Hadamard transforms also appears in a literature. The orthogonal Gold code shows reasonable cross correlation and off-peak autocorrelation values while giving a very good orthogonality condition. Multi-rate orthogonal codes are attractive as they can provide variable spreading factors depending on the information rate.

Fig.1 shows 16 orthogonal codes and 16 antipodal codes and there is a total of 32 bi-orthogonal codes. Antipodal codes are generated by taking the inverse of the orthogonal codes. The orthogonal codes and the antipodal codes have the same properties.

The advantage of using orthogonal codes is given below

(a) No need of Parity Bits
(b)The error correction capability increases compared to Hamming codes.
(c) As the code length increases error detection also increases.
(d) The cross correlation of orthogonal code is zero.

The notable advantage of the orthogonal code is that, it does not have to send the parity bits, therefore the number of parity bit should be always zero in orthogonal codes.

Therefore the destination side ie, the receiver will generate a parity bit. The parity bit generated at the receiver side because of the errors present in the transmitted bits. If k-bit data is present, then it is mapped to n-bit orthogonal codes. For example, if there is a data bit of 7 bits, then it is represented by 64 orthogonal codes and this sixteen bit orthogonal codes are sent without adding the party. So the use of parity bits at the transmitter side is avoided in orthogonal codes.

At the receiver side the receiver decodes the data based on code correlation method. In this process a threshold value is defined between the two orthogonal codes. The threshold value can be set by using the following equation.

$$d_{th} = (n/4) \qquad (1)$$

n = Code length
$d_{th}$ =Threshold value



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The threshold value is placed in the middle of two orthogonal codes. For example, if there are 5 data bits, there will be 16-bit orthogonal codes, which is shown in figure. 2.

$$d_{th} = \frac{16}{4}$$

Where 16 is the number of orthogonal codes and $d_{th}$ is the threshold value for orthogonal codes. Error correction is carried out by a mechanism called decision process. This process will correct the corrupted data. The incoming orthogonal codes are compared with the codes that are stored in the LUT (Look Up Table). In this method the incoming data are checked for a good correlation between the stored codes. If a good correlation is achieved a valid code is obtained otherwise the detection will be false. The correlation process is carried out by using a couple of n-bit codes. The codes are given below

X1, X2, X3…….Xn
and
Y1, Y2, Y3, ……Yn

$$R(x,y) = \sum_{i=1}^{n} x_i \ y_i \leq d_{th} \qquad (2)$$

$R(x,y)$ =Cross correlation function
$d_{th}$ = Threshold value that is already defined

An additional offset bit is added to the equation (2) for valid detection. The number of errors that can be corrected properly can be calculated by the equation (3).

$$N = R(x,y) - 1 \leq (n/4) - 1 \qquad (3)$$

Where,
$N$ = The total number of errors that can be corrected.

The equation (3) can be obtained by combining the equations (1) & (2).

From the equation (3),it is clear that 2 errors can be corrected for 8-bit orthogonal code, 3 errors can be corrected for 16-bit orthogonal code,7 errors can be corrected for 32-bit orthogonal code and so on. The proposed method is done by using the EXOR operations among the impaired received code and each code that is saved in the LUT(Look Up Table).The LUT stores all the codes.

There is a need of a counter to count the number ones present in the resulting data.32 counter result is needed for 16 bit orthogonal codes.

## III. PROPOSED WORK

In orthogonal codes the parity is generated only at the receiver end. No need of adding parity bits from the transmitter side. If the received data is corrupted ,there will generate a parity error.

For detecting the corrupted data ,the received code is split into two equal parts and each part will be processed for parity. If the generated parity is zero the received data contains no error.ie, it is error free data. If the generated parity is one ,then the received code is corrupted. The proposed method will improve the trans-reception system and area.

**Table .1.Orthogonal codes and their error correction capabilities**

| Code Length (n) | Number of errors that can be corrected (N) |
|---|---|
| 8 | 1 |
| 16 | 3 |
| 32 | 7 |
| 64 | 15 |
| 128 | 31 |
| 256 | 63 |

**Table. 2. Error detection rate of the orthogonal codes**

| **Code Length (n)** | **Detection Rate (%)** |
|---|---|
| 8 | 93.47 |
| 16 | 99.54 |
| 32 | 99.89 |
| 64 | 100.00 |

### *A. Transmission of Data*

The transmitter side contains two important modules they are,

(1) Encoder
(2) Shift Register

The purpose of the encoder is ,it encodes the m-bit data stream and the data is mapped to n-bits of orthogonal codes.

$$Nc = 2^{m-1} \qquad (4)$$

Nc = number of orthogonal codes.

The function of the shift register converts the code to a serial data which is shown in Figure .3. A parallel to serial conversion is taken place.

An example can explain this concept. A 5-bit data is encoded, then a 16-bit ($2^4$) orthogonal code is produced. The generated orthogonal code is converted to serial data by using shift register with the rising edge of the clock.



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### *B. Reception of Data*

At the receiver side the codes present in the LUT is compared with the received data. XOR operations are used for this process. First, received serial bits are changed into n-bit parallel code by using serial to parallel converter. A counter is used to count the number of 1's after EXOR operation among the received impaired code and all the LUT entries.

This will give a minimum count of 1's among them. The orthogonal code associated with minimum count is the closest match for the code arrived at the receiver section, which is then decoded to the correct data(That is same as the input data). Three different cases results are present from the simulation[12].

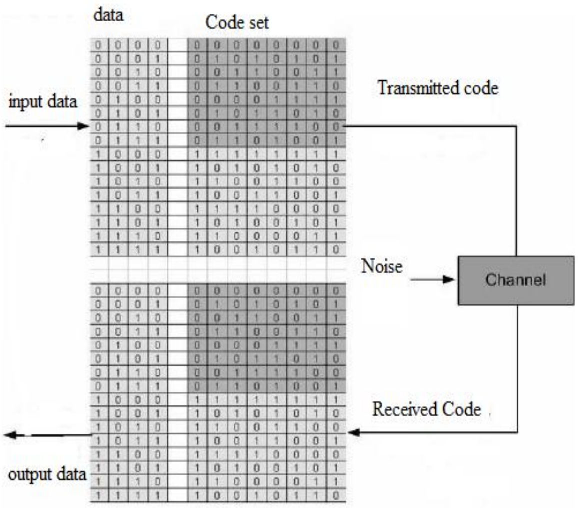


**Fig. 2, Representation of encoding &decoding for 8-bit orthogonal codes**

| 16 BIT ORTHOGONAL CODE | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | P |

| 16 BIT ANTIPODAL CODE | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | P |

**Fig . 1, Representation of 16-bit orthogonal codes.**

(1) Received code has a match in the LUT.
(2) Received code has no match in the LUT
(3) More than one possibility of closest match in LUT

In the second case the single error bit is detected and corrected.. The value of minimum count is associated more than one orthogonal code and thus it is not possible to find the closest match in the LUT for the received code[1,3,12].

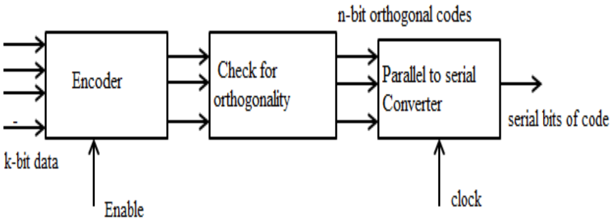


**Fig. 3, 5-bit transmitter**



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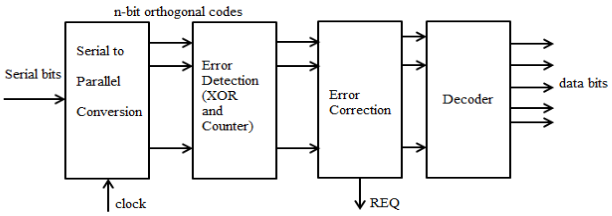


**Fig. 4, Receiver**

## IV. RESULTS

Code is written in Verilog and Altera Quartus-II software is used for code testing. Simulation results are verified for 16-bit orthogonal codes.The error detection rate can be calculated for a *k*- block of n –bit code is given in equation (5).

$$Detection\ Rate\,(\%) = \frac{2^n - 2^k}{2^n} \qquad (5)$$

If a data =00010, then its orthogonal code is 0110011001100110 and a rising edge of clock is used for transmission of data. In Fig. 6 ,the received data bits are not corrupted,that is the count equal to zero. So the received data are decoded as 00010.

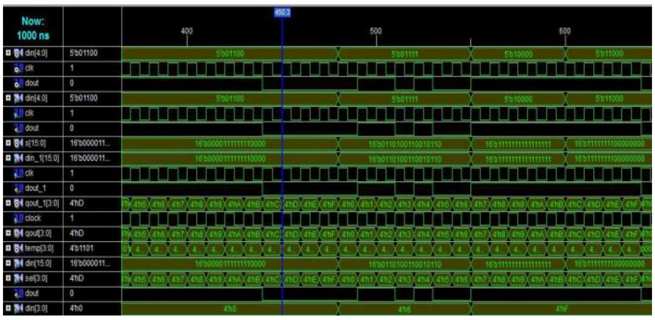

Fig.5,Simulation result of the transmitter

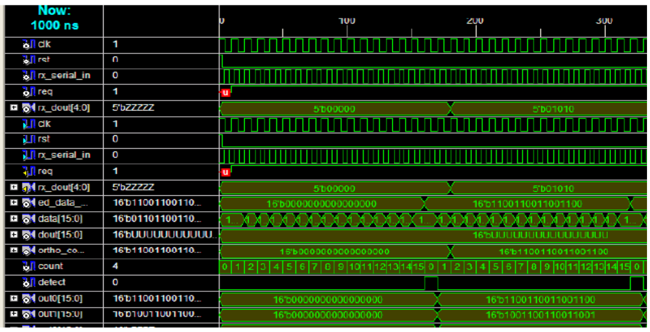

Fig.6, Simulation Result of Receiver

## V. CONCLUSION

Compared to Hamming codes it is better to use the orthogonal codes for error detection and correction. The implementation of the orthogonal convolution on a hardware platform is efficient. Using Verilog code the detection and correction of errors are carried out. The error detection is improved up to 99.89% for 16 bit codes. The main advantage of the orthogonal code is that, there is no parity bits on the transmitting side .

## REFERENCES

[1] S. Faruque, N. Kaabouch, and A. ,Dhirde, "Forward error control coding based on orthogonal code and its implementation using FPGA " Wireless and Optical Communication Proceedings, PP, 565-630, ACTA Press, June 2007 Chakrabarti, S. (2000): Data mining for hypertext: A tutorial survey. SIGKDD explorations, **1**(2), pp. 1–11.

[2] N. Kaabouch, A. Dhirde, and S. Faruque," Improvement of the Orthogonal Code Convolution Capabilities using FPGA Implementation", IEEE Electro / Information Technology Proceedings. Pp. 380-384,2007.

[3] A. Hokanin, H. Delic, and S. Sarin, "Two dimensional CRC for efficient transmission of ATM Cells over CDMA", IEEE Communications Letters, Vol. 4, No. 4, pp. 131-133, April 2000.

[4] S. Faruque, " Error Control Coding based on Orthogonal Codes", Wireless Proceedings, Vol. 2, pp. 608-615, 2004.

[5] U. K. Kumar, and B. S. Umashankar, "Improved hamming code for error detection and correction", 2007 2nd International Symposium on Wireless Pervasive Computing, pp. 498-500.

[6] T. Baicheva, S. Dodunekov, and P. Kazakov, "Undetected error probability performance of cyclic redundancy-check codes of 16-bit redundancy", IEEE Proceedings. Communications, Vol. 147, No. 5, pp. 253-256, Oct. 2000.

[7] V. Stylianakis, S. Toptchiyski, "A Reed - Solomon coding/decoding structure for an ADS modem", in Conf. Rec. 1999 IEEE Int. Conf. on Electronics, Circuits and Systems, pp. 473 – 476.

[8] A.Mitra, "On Pseudo-Random and Orthogonal Binary Spreading Sequences", International Journal of Information and Communication Engineering ,pp.447-454, 2008

[9] Luca Reggiani, Annalisa Tomasetta, Gian Mario Maggio, "Orthogonal Convolutional Modulation for UWB Impulse Radio Communications", IEEE conference ISCAS . pp2441-2444, 2006

[10] Z. Cai, J. Hao, S. Sun, and F. P. Chin, **"**A high-speed reed-solomon decoder for correction of both errors and erasures", 2006 IEEE International Symposium on Circuits and Systems, pp. 281-284.

[11] S. Shukla, N.W. Bergmann, "Single bit error correction implementation in CRC-16 on FPGA", in Conf. Rec. 2004 IEEE Int. Conf. on Field-Programmable Technology, pp. 319-322

[12] Mukesh Gholase , L.P.Thakare, Dr. A.Y. Deshmukh "Enhancement of Error Detection and Correction Capability Using Orthogonal Code Convolution".2013 International Journal of Computational Engineering Research,Vol, 03.pp.66-71

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