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Design And Simulation of 64 bit ALU

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Abstract— **ALU is the fundamental unit of a microprocessor which performs all the basic operations based on the control input selection. There are separate units which work independent of the main ALU for performing secondary operations such as address computation. The ALU performs arithmetic functions such as addition, subtraction etc and logic functions including, logic AND, logic OR, and logic XOR etc. These various functions of the ALU are implemented using a set of functional units each implementing a function. It may also be done using sharing of same hardware with use of certain additional units like multiplexers.**
In this line of thought, the proposed project deals with design and simulation of 64 bit ALU using VHDL with the help of Xilinx ISE software.

***Index Terms*— ALU, VHDL, Xilinx**

I. INTRODUCTION

VHDL is standard language of an industry for the modeling, description, & synthesis of digital circuits & systems. The electronic design automation industry has expanded the use of VHDL from initial concept of design documentation, to design implementation and functional verification. [5] It can be said that VHDL fueled modern synthesis technology and enabled the development of ASIC semiconductor companies. The use of VHDL has evolved and its importance increased as semiconductor devices dimensions have shrunk. Use of VHDL is increased to allow designers, electronic design automation companies and the semiconductor industry to experiment with new language concepts to ensure good design tool and data interoperability.[2] The fundamental motivation to use VHDL is that VHDL is standard technology independent language therefore portable and reusable.[4] Present industry practice has created a high demand for systems designers with knowledge and experience in using programmable logic in the form of CPLDs and FPGAs in addition to hardware description languages.
This paper entitles design and implementation of 64 bit ALU using behavioral modeling and structural modeling. The design of ALU includes logical operations which are implemented with simple gates to operate independently. The mathematical operations of ALU are performed using repeated additions. Multiplication and division are as a single unit.
The design has three modules and outputs are combined at top most level using a multiplexer.

II. SYSTEM DEVELOPMENT

The ALU is implemented using parallel implementation of Functional units which perform individual functions such as addition, subtraction etc. Operands are received and fed to the unit corresponding to the operation to be performed and result is produced by that unit and fed to the output lines of the ALU. The select lines determine the operation to be performed. Also the flags are set by the ALU.

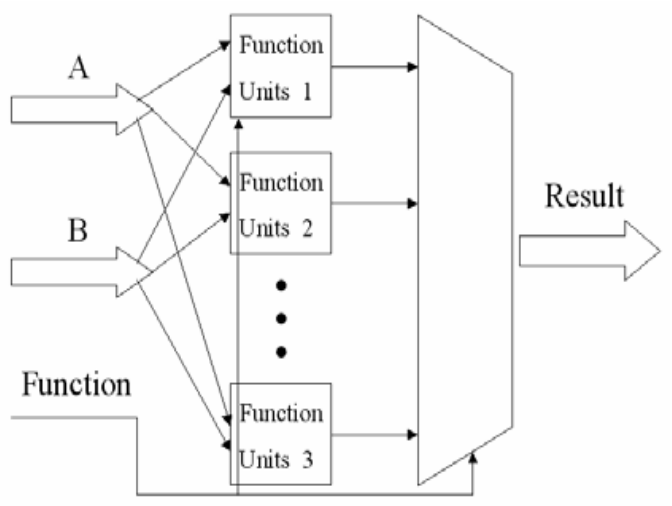

Figure 1. Block diagram

The various functions and the corresponding functional units are

A. Functional Unit-I:-Basic ALU Unit

It performs following logical & arithmetic operations on given operands.

- *Logical operations*

The various logical operations performed by ALU are AND, .OR, XOR, NOT, SHIFT, ROTATE

- *Arithmetic operatons*

The ALU can operate addition, subtraction, increment and decrement between A and B inputs.

B. Functional Unit-II:-Basic ALU Unit

It performs multiplication operation on given operands.

C. Functional Unit-II:- Division unit

It performs division operation on given operands.

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Table I. Function & select lines

FUNCTION	SELECT LINES				OPERATION
	S3	S2	S1	S0	
INCREMENT	0	0	0	0	a + 1
ADC	0	0	0	1	a + b + cin
SBB	0	0	1	0	a – b - cin
DEC	0	0	1	1	a - 1
AND	0	1	0	0	a AND b
OR	0	1	0	1	a OR b
XOR	0	1	1	0	a XOR b
NEG	0	1	1	1	NOT a
SHIFT RIGHT	1	0	0	0	Data shift to right
SHIFT LEFT	1	0	0	1	Data shift to left
ROTATE RIGHT	1	0	1	0	Rotate Data to right
ROTATE LEFT	1	0	1	1	Rotate Data to left
MULTIPLICATION	1	1	0	0	Multiplication of data
DIVISION	1	1	0	1	Division of data

Above table shows various functions performed by proposed ALU. These various functions of the ALU are implemented using a set of functional units each implementing a function, these may also be done using sharing of same hardware with use of certain additional units like multiplexers. The ALU has 3 set of input signals and one output signal. Operands A and B are both 64 bits each. These are fed to these functional units along with select lines which decide the operation to be performed. Each combination of the select lines corresponds to one particular function. There are also some other output signals in the ALU, such as overflow, zero and negative, Arithmetic and logic unit.

III. IMPLEMENTATION & RESULTS

The design consists of four components such as basic ALU to perform logical and arithmetic operation, multiplication component to perform multiply operation, division component to perform division operation and multiplexer to select output of specific component to obtain final output.The top level entity of design consists of two 64 Bit inputs A & B, 4 bit select lines to perform particular function on inputs to gnerate the final output. It also consists of clk, carry, enable and reset input. The final output is 128 bits.

VHDL code for all the modules is written, simulated and synthesized using Xilinx ISE 10.1v. The target device chosen for the same is Spartan XC-3S 1500. The respective results of all the modules are shown below.

The simulation result of basic ALU module is shown below. Simulation results for Increment, add With Carry (ADC) and SBB operation is shown in fig 3.1.:-

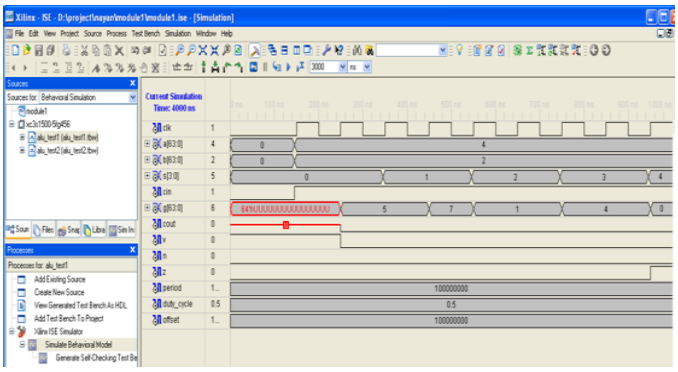

Figure 3.1 Simulation result of Increment,ADC and SSB operation

The Simulation results for DEC, AND and OR operation is shown in fig. 3.2

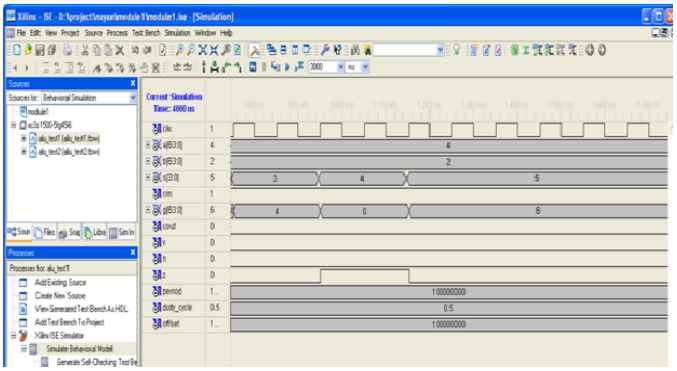

Figure 3.2 Simulation result of DEC, AND and OR operation

The Simulation results for XOR, NOT & Shift right operation is shown in fig. 3.3

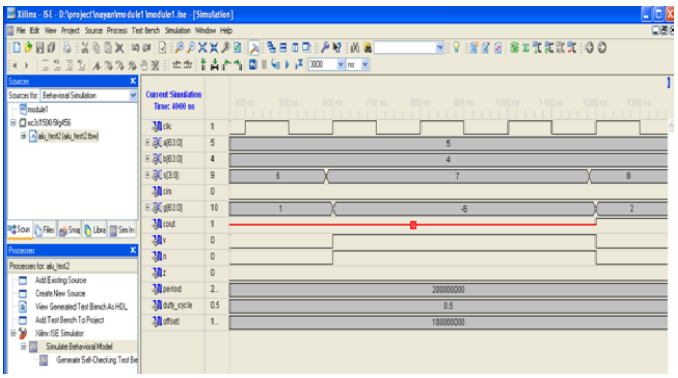

Figure 3.3 Simulation result of XOR, NOT & Shift right operation

The Simulation results for shift left, shift right & rotate left Operation is shown in fig. 3.4

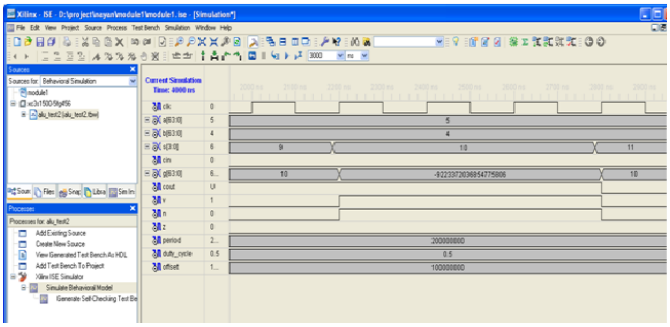

Figure. 3.4 Simulation result of shift left, shift right & rotate left Operation

The simulation result of multiplication module is shown below in fig. 3.5

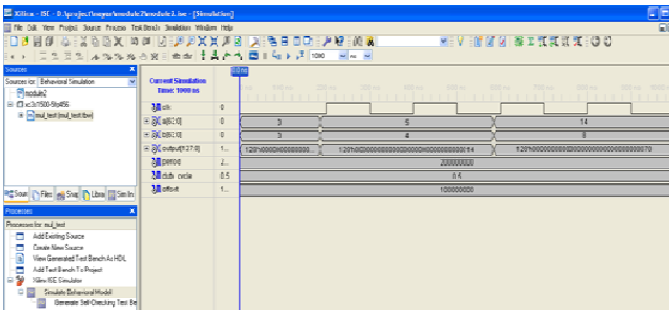

Figure 3.5 Simulation result of multiplication module Operation

The simulation result of division module is shown in fig. 3.6

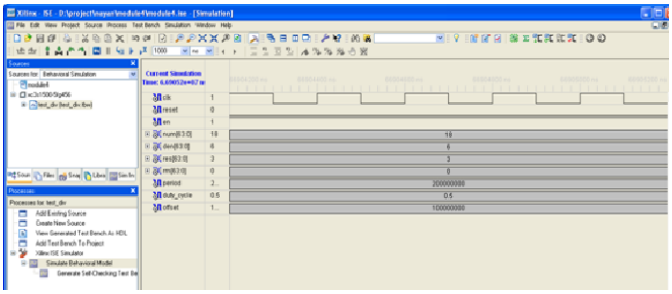

Figure 3.6 Simulation result of division Operation

After verification of all the modules, they are integrated in top level module using structral modelling. Then top level module is simulated & synthesized using xilinx ISE tool. The final results of top level module for rotate left & multiplication operation is shown in fig.

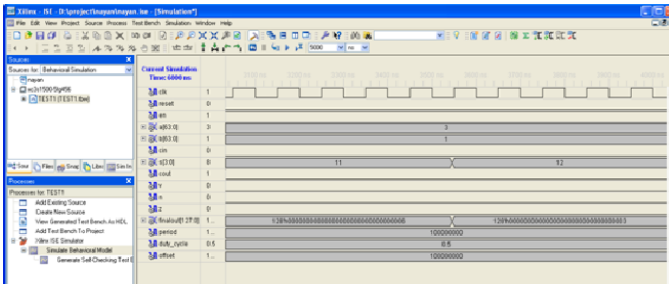

Figure 3.7 Simulation result of top level module

The device utilization summary of proposed ALU is shown in Table II. It shows efficient utilization of slices, slice flip-flops, IOBs, GCLKs and LUTs for implementation of ALU on FPGA device.

Table II. Device utilization summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	5306	13312	39%
Number of Slice Flip Flops	457	26624	1%
Number of 4 input LUTs	9211	26624	34%
Number of bonded IOBs	268	333	80%
Number of GCLKs	1	8	12%

IV. CONCLUSION

The 64 bit arithmetic and logic unit is designed using VHDL and synthesized using Xilinx ISE v10.1 platform. The ALU is implemented using parallel implementation of units which perform various functions such as arithmetic, logical, shift and rotate operations. Operands are received and fed to the unit corresponding to the operation to be performed and result is produced by that unit and fed to the output lines of the ALU. The synthesized top level module is targeted to Spartan device. We have verified the results obtained from Xilinx ISE Design Suit with the theoretical results for all the operations that were performed and found that they match with the theoretical values.

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