International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 4, April 2015

DESIGN OF DOUBLE TAIL COMPARATOR FOR LOW POWER APPLICATION

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ABSTRACT

Dynamic regenerative comparators are need for ultralow power, are efficient and high speed analog to digital converters. An analysis on the delay of dynamic comparators will be presented and analytical expressions are derived. The conventional double tail comparator is modified based on the presented analysis and the new dynamic comparator is proposed for low power and fast operation even in small supply voltage. Without complicating the design and by adding few more switching transistors a new comparator is designed by using the power gating technique. The main idea of modified comparator is to reduce the static power consumption by completely cutoff the flow of the leakage current to ground. Then the modified structure is reducing the power consumption drastically.

Keywords: Double tail comparator, power gating technique

I. INTRODUCTION

Comparators are mostly used in large abundance in A/D converter because it is known as 1 bit analog to digital converter. Comparators are most probably second most widely used electronic components after operational amplifier in this world. In decision making response time of the comparator the speed is limited. Apart from that it is used many applications like zero crossing detector, peek detectors, data transmission and others.

The basic CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with reference signal and outputs a binary signal on comparison.

II. SINGLE TAIL COMPARATOR

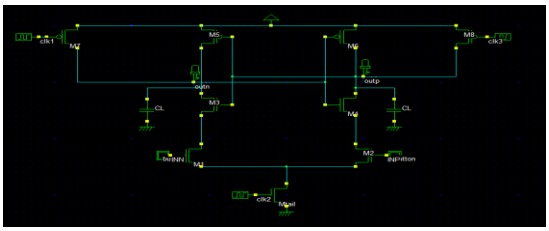

Figure 2.1 Schematic diagram of single tail comparator

ISSN: 2278 – 909X

OPERATION

Following are the two phases of single tail comparator.

1) Reset Phase

2) Comparison Phase

Reset phase

Clk=0, Mtail=off, reset transistor M7-M8 are ON, pull both output nodes to VDD to define start condition and valid logical level.

Comparison phase

Clk=VDD, Mtail=ON, with different rates depending on the corresponding input voltages. Where VINP>VINN, outp discharge faster than outn, where outp falls down to before out the corresponding PMOS transistor M5 will turn on initiating the latch regeneration caused by back to back invertors(M3,M5,M4,M6).Thus outn pulls to VDD and outp discharges to ground. If VINP<VINN, the circuit work vice versa. The delay of the comparator is comprised two delays t0 and latch.

III. THE CONVENTIONAL DOUBLE TAIL DYNAMIC COMPARATOR

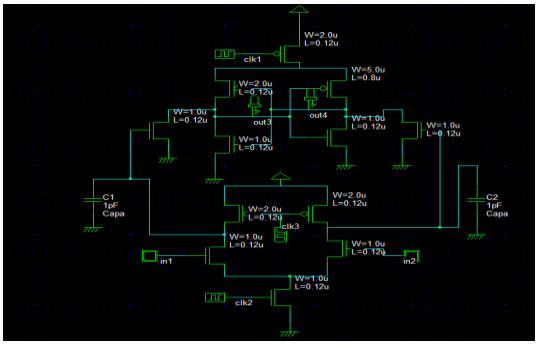

Figure.3.1Schematic diagram of conventional double tail dynamic comparator

OPERATION

The operation of this comparator is as follows (see Fig. 3.1).

During reset phase

Transistors M3-M4 pre charge and nodes fn and fp recharged to VDD and clk is 0, Mtail1 and Mtail2 are off. This change leads transistors MR1 and MR2 to discharge the output nodes to ground.

During decision making phase

M3-M4 turn off and voltages at node fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and input dependent differential voltage Vfn(p) to the cross coupled invertors and also provides a good shielding between input and output ,

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resulting in reduced value of kickback noise. On that clk is VDD, Mtail1 and Mtail2 is turn on.

IV DOUBLE TAIL DYNAMIC COMPARATOR(mainidea)

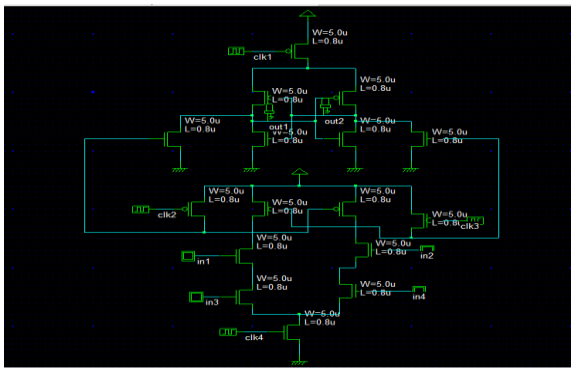

Figure 4.1 Schematic diagram of double tail comparator

OPERATION

The main idea of low voltage low power double tail comparator is to increase differential node voltage of Np and Nn node. The operation of low voltage low power double tail comparator is described as follows. When clock is reset (clk=0), M1 and M6 are off and M8 and M9 are on. Transistor M8 and M9 pull Np and Nn node voltage to VDD, hence transistor M6 and M7 are cut off. Intermediate stage transistor (M15 and M14) are on which reset both latch output voltage to 0 v. when clock is set (clk=VDD), M1 and M16 are on and transistor M8 and M9 are off moreover, at the beginning of evaluation phase (clk=VDD), the control transistor (M6 and M7) remain off since Np and Nn are about VDD). Thus Np and Nn node voltages start to drop with different rates according to the applied input voltages. Let Vinp>Vinn, Nn node voltage drops faster than that of Np.

The operation of control transistor imitates the operation of latch stage. It reestablishes the Np and Nn node voltage through the intermediate transistor M14 and M15 to give full swing output voltage.

V.MODIFIED DOUBLE TAIL COMPARATOR

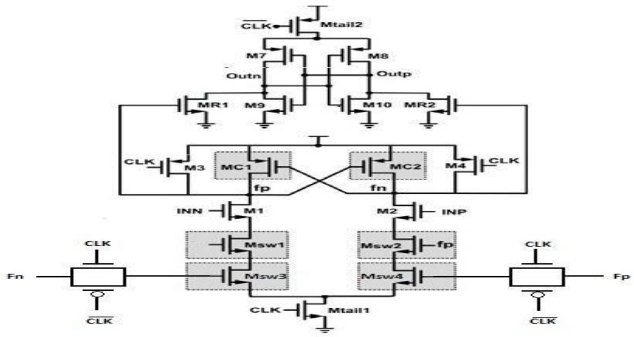

Figure 5.1 Modified double tail comparator

OPERATION

During reset phase

When clk=0, Mtail1 and Mtail2 are off, M3 and M4 transistors are switched on

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and charge the fp and fn nodes to VDD. During this time MC1 and MC2 are in cutoff state. Then MR1 and MR2 intermediate stage transistors reset latch outputs to ground.

During decision making phase

When clk=VDD, Mtail1 and Mtail2 are on, M3 and M4 transistors turn off. At the starting of the phase MC1 and MC2 control transistors are still off(since fn and fp are about VDD). The input voltages fn and fp nodes starts discharging with different rates. fp node discharge faster than fn if VINP>VINN, it causes the MC1 transistor turn on and recharge the fp node to VDD and MC2 will continue to be in off condition.

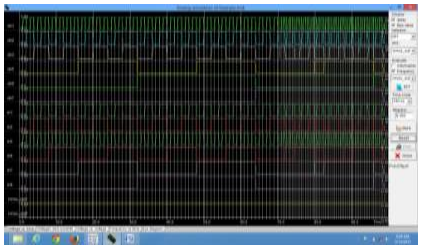
So the voltage difference between fn and fp increases, leading to reduction of latch regeneration time. In the proposed idea, as one of the control transistor turns on, a current from VDD is drawn to ground through MC1, M1, MSW1 and Mtail which leads to static power consumption. Even the switching transistor MSW1 cannot completely reduce the flow of current and solve the static power consumption problem. Adding two more NMOS switches below the switching transistor (MSW1 and MSW2) to solve this problem. The power gating technique is used and the domino logic style is implemented.

During decision making phase

Fn and fp nodes get discharged to ground depending on the input voltage, then fn node discharge faster than fp if INP>INN, which causes the MC1 control transistor to turn on and charge the fp node again and make the voltage difference faster. To maintain the fp node in charged condition and fn node discharged to ground, the switching transistor MSW1 and MSW2 are used, where MSW1 is open means MSW2 is closed switch. In proposed structure two more transistors is added with power gating technique and domino logic. By using this power consumption is reduced.

VI.SIMULATION RESULT

Modified double tail comparator



6.1 output waveform

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TABLE

Comparator structure	**power**
Double tail comparator	P=0.807mw
Modified comparator	P=0.308mw

VII.CONCLUSION

An analysis for clocked double tail dynamic comparators is presented. One structure of double-tail dynamic comparators was analyzed. Also, based on analyses, a new dynamic comparator was proposed in order to improve the performance of the comparator with low power and voltage. Based on the analysis a new dynamic double tail comparator with low voltage, low power capability was proposed to improve the performance o comparator mainly concerned in power consumption. The proposed comparator is reduced to great extent in comparison with all other comparator.

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ISSN: 2278 – 909X