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VLSI Design of Power Efficient Reversible LFSR Using Pseudo Reed-Muller Expressions

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Abstract— **Power dissipation is considered as one of the most important factors while designing a circuit. Reversible logic has become a promising technology in low power design. It is because reversible logic utilizes only very less power, thereby leading to less power dissipation. Conventional circuits which are irreversible in nature are subject to very large amount of minimum power dissipation per signal transition. Reversible logic is considered as a computing paradigm in which there is a one-to-one mapping between the input and the output vectors. In this paper we discuss with reversible circuits and reversibility which in future will be considered as a trend for low power design. Combinational circuits were the primary ones to be implemented using this technique. Later on few researches also contributed toward sequential circuits.**

In this paper we implement a reversible LFSR that dissipate less power than the conventional LFSR circuitry. Here we use Pseudo Reed-Muller expressions (PSDRM) for the synthesis of the design. There are also other methods of synthesis. But it has been found that PSDRM circuits are more efficient than other techniques such as Positive Polarity Reed-Muller (PPRM) expression and Fixed Polarity Reed-Muller (FPRM) expression based circuits. By using this technique there is more optimization as well as improvement in other factors such as number of gates, memory usage, garbage output, quantum cost etc.

Index Terms—**Garbage output, LFSR, PSDRM, Reversible logic.**

I. INTRODUCTION

Launder [1] states that, conventional circuits dissipate large amount of heat energy during computation due to the loss in information. It has been proved that for each bit of information loss there is kTln2 joules of heat energy; where k is Boltzmann's constant and T is the absolute temperature on which computation is performed. Bennett [2] proved that energy dissipation issues can be reduced if all the gates in the circuits are made reversible. It is because reversible logic makes each and every step of computation to be completely reversible, so that no information is lost at any step of computation. The levels of logic in reversible circuits are significantly high than the standard logic and they are considered as a special case of quantum circuits [7].

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Reversible computation can be only made possible by using reversible gates. Most of the gates that we use in digital circuits such as AND, OR, NAND, NOR etc. are irreversible in nature. Only NOT gate among them is reversible. Some other reversible gates include the Peres gate, Toffoli gate, Fredkin gate, Feynman gate etc. The commonly used reversible gates are shown in Fig.1. It should be noted that reversible logic circuits must always be designed using minimum number of reversible gates, and with minimum number of constant inputs. Before using synthesis techniques replacement technique was used, where the irreversible parts of the design was replaced by reversible gates [9].

Reversible circuits are of two types that is reversible combinational and reversible sequential circuits. There are many research attempts focusing on reversible logic synthesis but they are mostly centered on reversible combinational logic synthesis. Only a few researches among them are carried over reversible sequential circuits. Reversible Logic Design is quite different from the traditional Combinational Logic Design. It is important that in Reversible Logic, the number of input lines must be equal to the number of output lines such that each output line is being used only once thereby making the resulting circuit acyclic. Thus Reversible Logic circuitries consist of n-inputs and n-outputs with one-to-one mapping. By this it is possible to determine the outputs from the inputs and vice-versa. Hence we can say that there is a one-to-one correspondence between the input and output vectors. Reversible logic finds application in fields like low power CMOS, nanotechnology [6], DNA computing, optical computing and Quantum computing. Thus in total Reversible logic can be considered as a new trend in Low power circuitry design.

Here in this paper, we deal with the design of a Reversible LFSR which is synthesized using PSDRM expression. The next state of LFSR is expressed in terms of Pseudo Reed-Muller expressions (PSDRM). Prior to PSDRM, the Positive Polarity Reed-Muller (PPRM) and Fixed Polarity Reed-Muller (FPRM) based reversible circuit synthesis was adopted. FPRM-based reversible circuit synthesis method is more efficient than PPRM-based synthesis. Pseudo Reed-Muller (PSDRM) expression is a more generalized class of Reed–Muller expression and requires less or at most equal number of product terms than FPRM expression. Thus we in this paper make use of the effective PSDRM expressions.

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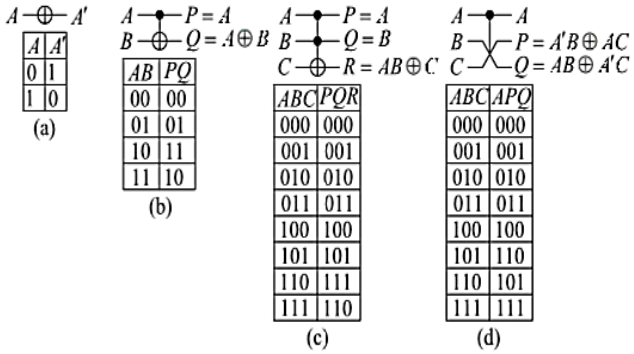

Fig.1. Commonly used reversible gates (a) NOT gate. (b) Feynman gate. (c) Toffoli gate (d) Fredkin gate.

The rest of the paper is organized as follows. Section II gives a brief background on Reversible logic. Section III presents Reversible logic synthesis using PSDRM; Section IV describes the design of reversible LFSR; Section V provides the results and discussion obtained by designing the circuit. Finally we conclude the paper in Section VI.

II. BACKGROUND ON REVERSIBLE LOGIC

A reversible circuit maps every input combination into a unique output combination. This unique mapping implies that a reversible circuit comprise of the same number of inputs and outputs. A reversible logic with n input/output is usually called as an n×n reversible circuit. Thus a network of reversible gates together forms a reversible circuit [8].

For conventional (irreversible) circuit synthesis, we generally start with a universal gate library and some specification of a Boolean function. The primary goal is to find a logic circuit that implements the Boolean functionality and minimizes a given cost metric, e.g., the number of gates or the garbage output etc. At a high level, reversible circuit synthesis is just a special case in which no fan-out is allowed and all gates must be reversible.

A. Cost Metrics: A reversible circuit can be implemented in several ways, resulting in different cost. This section focuses on some of the major cost metrics which are generally used to evaluate and compare reversible circuits.

1) Gate Count: It refers to the number of gates in total that is required to implement the circuit. It is one of the major cost metric used in the evaluation of reversible sequential circuit [3].

2) Garbage Output: Some outputs pins are used only to maintain the reversibility of the logic, but are not used as the final outputs or as input to other circuits. These unused outputs are called as garbage outputs.

3) Quantum Cost: The quantum cost of a reversible gate is referred to as the number of quantum gates or the 1x1 and 2x2 reversible gates required to design the gate. The quantum costs of all reversible such as the 1x1 and 2x2 gates are taken as unity.

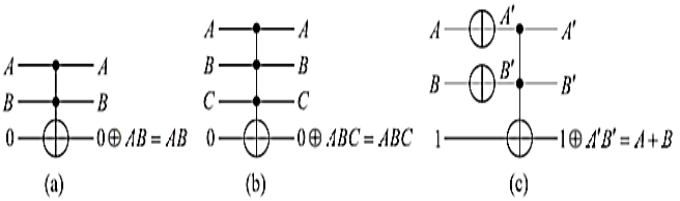

Fig.2. Reversible realizations of classical (a) two-input AND gate, (b) three- input AND gate and (c) two-input OR gate.

A detailed study on different reversible gates is presented in [8]. They can be used for the design of classical gates. Fig.2 shows the realization of classical gates such as AND gate and OR gate using reversible gate. The figure also shows the reversible realization of two input and three inputs AND gates. The complexity of reversible circuit design is generally compared in terms of quantum cost. Reversible realization of two-input AND gate requires five quantum cost and two garbage outputs and that of three-input AND gate requires 14 quantum cost and three garbage outputs. Reversible realization of two-input OR gate is shown in Fig. 2(c), which requires seven quantum cost and two garbage outputs.

III. REVERSIBLE LOGIC SYNTHESIS

Consider an n-variable Boolean function f (x_1, x_2., x_i,.., x_n) , which can be expanded using following equations:

$$f(x_1, x_2., x_i,.., x_n) = f_0 \oplus x_i f_2 \text{ (positive Davio, pD)} \quad (1)$$

$$f(x_1, x_2., x_i,.., x_n) = f_1 \oplus xi' f_2 \text{ (negative Davio, nD)} \quad (2)$$

If we apply pD expansion on all variables of an n-variable Boolean function f (x_1, x_2., x_i,.., x_n), then we obtain two trees corresponding to positive Davio as well as negative Davio[4]. For example consider a function given as below.

$$f(x1,x2,x3) = \sum(3,4,6,7). \quad (3)$$

If we apply equations (1) and (2) the example we obtain two trees as given in Fig.3.

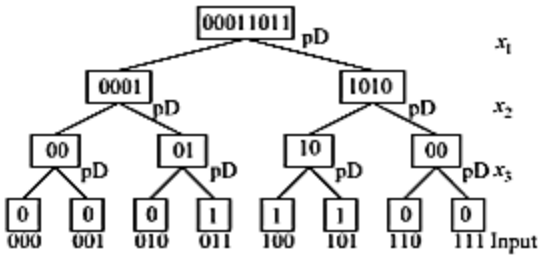

Fig.3 PSDRM tree obtained after applying Eqn.1 on function (3)

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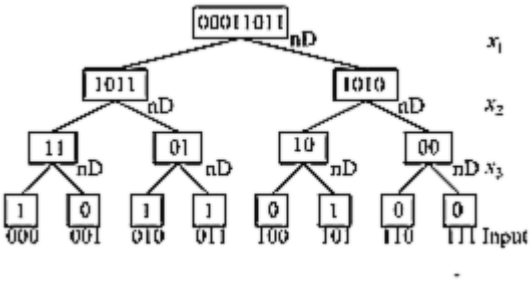

Fig.4 PSDRM tree obtained after applying Eqn.2 on function (3)

Similarly we also get a negative tree as shown in Fig.3. After obtaining both the trees we create an arbitrary tree to synthesis the given functionality. The leaves of the tree represent the coefficient vector. The resulting expression is determined from the ones of the coefficient vector and their corresponding input combinations. The resulting expression of the tree of Fig.2 is given as

$$f(x_1,x_2,x_3)= x_2x_3 \oplus x_1 \oplus x_1x_3. \qquad (4)$$

In this we can obtain output expression for negative tree as

$$f(x_1,x_2,x_3)= x_3 \oplus x_2' x_3 \oplus x_1x_3'. \qquad (5)$$

The PSDRM expression of equation (4) and (5) can be realized using reversible gates. We determine PSDRM expressions for the next states from the constructed PSDRM trees. At the right descendants of the root, apply either pD or nD expansion that produces the minimum number of ones at the next level of the tree. Break the tie by choosing pD expansion. And thus we obtain the PSDRM expression. This similar approach is also adopted for the synthesis of Reversible LFSR which is described in detail in the next section.

IV. DESIGN OF LFSR

A linear feedback shift register (LFSR) is a type of shift register whose input data bit is a linear function of its previous state. One of the most commonly used linear functions of single bits is XOR. Thus, an LFSR is most often considered as a shift register whose input bit is driven by the exclusive-or (XOR) of some bits of the overall shift register value. The initial value given into the LFSR input is called the seed value. As the operation of the register is deterministic; the stream of output values produced by the register is also completely determined by its current (or previous) state. However if we choose an LFSR with a good feedback function, it can produce a sequence of bits which has a very long cycle and which appears to be random. Applications of LFSRs include generating whitening sequences, pseudo-random numbers, pseudo-noise sequences, fast digital counters etc. The block diagram for a 4 bit LFSR is shown in Fig.5.

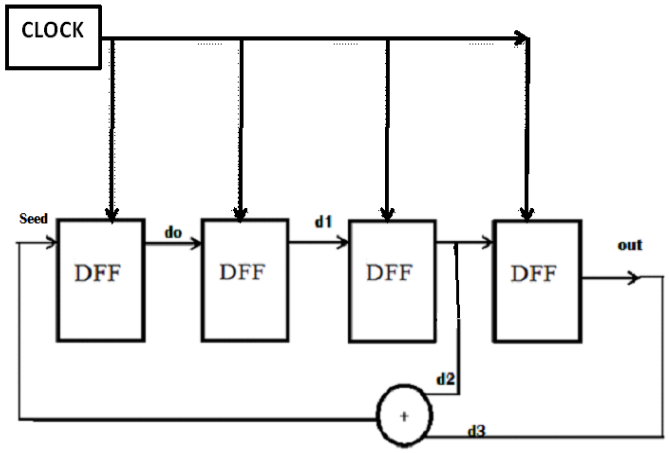

Fig.5. Block diagram for a Reversible LFSR.

The building blocks of LFSR constitute of D flip-flops and XOR gate. From the figure we can see that there are 4 D flip-flops and an XOR gate and thus Feynman and Fredkin gate can be used for the reversible realization of LFSR which were shown in Fig.1. For obtaining the reversible realization of LFSR we replace each of the D flip-flops with the circuits shown in Fig.6 and the XOR gate can be replaced by Feynman gate. In Fig. 6(a), the state output is obtained using a Feynman gate and fed back to the second input of the Fredkin gate.

When the clock C to the circuit is zero, then the feedback is connected to the state output such that it maintains the state output unchanged. When C becomes one, then the D input is connected to the state output that performs the level-triggered load operation. This realization requires about six quantum costs and two garbage output. In Fig. 6(b), the feedback is connected to the third input of the Fredkin gate. When C is one, then the feedback is connected to the state output maintaining the state output unchanged. When C becomes zero, then the D input is connected to the state output that performs the falling-edge triggered load operation. This realization requires six quantum costs and two garbage output. The PSDRM tree for LFSR differs for different LFSR. It is because of the fact that the input or the seed value given to LFSR is a random sequence. Hence there is no generalized form of PSDRM tree for a LFSR.

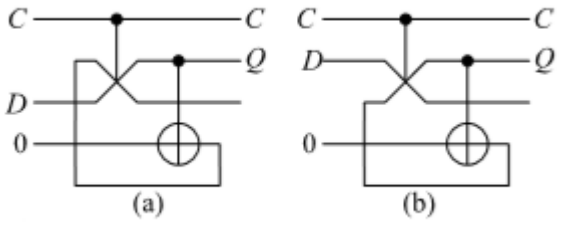

Fig.6. Reversible realization of (a) level-triggered and (b) falling-edge triggered D flip-flops.

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V. RESULTS AND DISCUSSIONS

Simulation of the designed circuit has been carried using Modelsim 9.1f and the power report is obtained using Xilinx ISE 8.1 simulator. The simulation result for a 4 bit LFSR is shown in Figure.7. We are using either VHDL or Verilog codes; hence the simulation can also be viewed using Modelsim. The HTML power report is shown in Figure.8. From the report we observe the fact that reversible circuits dissipate 56mw of power.

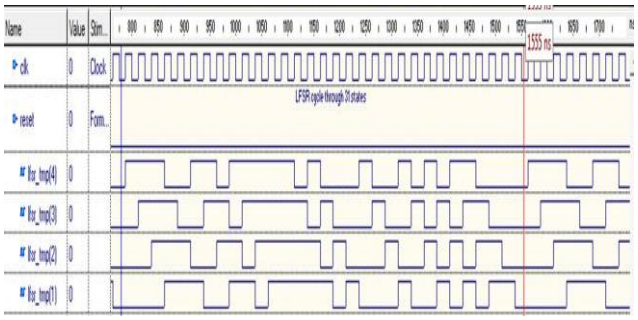

Fig.7. Simulation result for a 4-bit Reversible LFSR

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		56
Vccint 1.80V:	28	50
Vcco33 3.30V:	2	7
Clocks:	0	0
Inputs:	7	13
Logic:	4	7
Outputs:		
Vcco33	0	0
Signals:	1	2
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Fig.8. HTML power report of reversible LFSR

TABLE I. Comparison of conventional LFSR with that of Reversible LFSR

Cost metrics	Conventional LFSR	Reversible LFSR
Power consumption	67mW	56mW
Gate counts	86	36
Garbage output	8	5
Quantum cost	25	16
JTAG count for I/O Blocks	720	144
Peak memory usage	185MB	186MB

TABLE II. Comparison of direct design with the design technique adopted in [9]

	Direct design	Replacement design	% Improvement
Garbage output	112	220	49.09
Quantum cost	17	35	51.43

The comparison of Reversible and a non-reversible LFSR is shown in the tables .The first table gives the comparison of various cost metrics involved in the designing of the circuit. It can be seen from the table that power consumption is reduced in reversible LFSR.

In conventional LFSR the amount of power dissipation is about 67mw .For reversible circuits the power consumption is reduced by 11Mw. The next metric that is taken into account is the Gate counts. From the table it can be clearly seen that there is a great reduction in the gate counts. The reversible logic uses very less number of gates. Other cost metrics like Garbage output and quantum cost is also reduced from 8 to 5 and 25 to 16 respectively. The JTAG count of input-output block is also reduced from 720 to 144 but at a cost of 1MB of memory. But we get very good results for other cost metrics and hence this parameter is usually negligible. Hence the cost incurred during the design of circuits can also be reduced if the factors such as garbage output, quantum cost, number of gates etc. are reduced.

The second table provides a comparison of direct design technique that we use here with that of replacement technique [9]. From the table we can clearly say that direct design technique that we have adopted has great improvements. There is 49.09% reduction in the garbage output. Similarly the quantum cost also decreases by 51.43%.

VI. CONCLUSION

Reversible logic is very much reliable for low power circuits. Reversible gates are used to implement Reversible circuits. Commonly used reversible gates include Fredkin gate, Feynman gate, Toffoli gate etc. Although there is large number of research which is carried over combinational reversible gates, the designing of sequential circuits are still at its primary stage. In this paper we discuss about the designing of reversible sequential circuits. The synthesis method that we adopt is PSDRM expression. And by this method we design a Reversible LFSR that is efficient in terms of power consumption, garbage output, gate counts etc. Thus we can say that reversible LFSR are more efficient than the conventional LFSR. Reversible LFSR finds application in fields like low power CMOS, Quantum computing. In future we can also implement other reversible sequential circuits such as RAM, counters, ALU etc.

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