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Design and Simulation of an Efficient Vedic Booth Multiplier

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Abstract:

A new multiplier design using the combination of modified booth's recoding algorithm and Vedic mathematics is presented in this paper. The basic Vedic multiplication algorithm requires multipliers to perform multiplication internally i.e, vertically and crosswise. If we use normal multipliers as an internal multiplier in Vedic it's performance is high but it consumes much power. The proposed Vedic multiplier design uses modified booth's recoding algorithm to perform internal multiplication. The proposed multiplier design gives high performance and consumes less power .the simulation and synthesis of the design is carried out using quartus II 9.1 tool.

***Index terms*: Vedic multiplication, booth's recoding algorithm**

I.INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multipliers are fundamental blocks in today's Digital signal processing units. Vedic mathematics is based on 16-sutras and 16-sub sutras invented in 1884.In vedic mathematics there are three sutras nikhilam navatascaraman dasatah, ekadhikena purvena and urdhva tiryakbhyam used for multiplication[2,3]. The basic meaning of Sanskrit word "urdhva tiryakbhyam" is vertically and crosswise.the proposed multiplier design was done using this "urdhva tiryakbhyam" suthra.modified booth's recoding algorithm is used to achieve parallel multiplication[1].this method is efficiently useful for redusing power consumption for large input bit sequences. compared to booth's radix-2 and radix-4 multiplication algorithms'vedic multiplier design consumes much power[2]. However,the speed of booth's multiplier was less compared to vedic mathematics[3].so, in order to satisfy both power and performance in a single design the proposed vedic multiplier design is usefull.

II. VEDIC MULTIPLICATION

Vedic mathematics is based on 16-sutras and 16-sub sutras invented by Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960). In vedic mathematics there are three sutras nikhilam navatascaraman dasatah, ekadhikena purvena and urdhva tiryakbhyam are suitable for performing multiplication[2,3].vedic mathematics is not only a mathematical wonder but also it is logical.that's why it has such a degree of eminence which cannot be disapproved. Because of to these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad [6].

The word "vedic" is derived from the word"veda" which means the store house of all knowledge. this vedic mathematics is dealing with various branches of mathematics like arithmetic,algebra,geometry[7]. This method is explained using below given example

let A=>2 B=>3

0000 0010 <= A

0000 0011 <=B

STEP1: according to this algorithm it will first devide the input bits into two equall parts

i.e, A=>A1 A0 and

B=>B1 B0

Where A1=0000

B1=>0000

A0=0010

B0=>0011

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STEP 2: As per urdhva tiryakbhyam sutras in vedic ,the multiplication should be performed vertically and cross wise in between the input bits[6]

Vertical multiplication will be done as follows

A0 x B0=> 0010 x0011=>00000110----→p1

A1 x B1 => 0000 x 0000 => 00000000→p2

Cross wise multiplication will be done as follows

A1 x B0 =>0000 x 0011 =>00000000 →p3

A0x B1=>0010x 0000 =>00000000→p4

STEP 3: The result produced by the cross multiplication should be added here

i.e, let s1=> p3+p4=>00000000

STEP4: at last p1,p2,s1 should be added to produce the final result of the multiplier.

Here p1, s1,p2 just like partial products. Fig.1. shows the addition scheme of partial products in order to shift the partial products to generate final product, we should follow the below given note

Note:

Number of bits to be shifted to add the partial products will depends on the the number of input bits.

Let r=>number of bits to be shifted to add partial products

n=> number of input bits

r=n/2

III.BOOTH'S RECODING ALGORITHM

Multiplication is broadly classified into two types based on the partial product generation

1. Sequential multiplication

2. Parallel multiplication

1. Sequential multiplication:

If the partial product generation requires add and shift operations, then we call that algorithm as "sequential multiplication" algorithm.

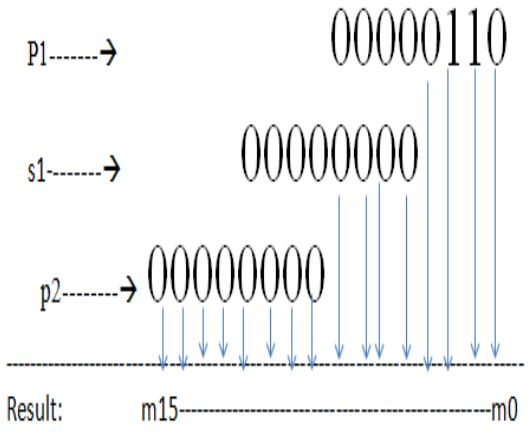

Fig.1.partial product addition scheme

2. Parallel multiplication:

If the partial product generation doesn't requires any add and shift operations, then we call that algorithm as" parallel multiplication" algorithm.

On comparing the speed, power and area parameters the parallel multiplication is better one.To achieve parallel multiplication booth's algorithm is widely used[1].in this multiplier we have reduced the number of adders required in partial product generation. In order to achieve multiplication, partial products can be generated using booth's recoding table an idea of getting partial products is explained in[1].

A.RADIX 2

Here we have the recoding unit using multiplexers. Select lines to multiplexer are input bit sequence of multiplier and output is according to the table1.here

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partial products are always one bit more than input bits. If our input is 'n' bit then, the number of bits in the partial product is n+1.

Table.1 .Booth's recoding table for radix2

X_i	X_{i-1}	Y	Partial Product Explanation
0	0	0	All 0's
0	1	1.A	$[A_{(n-1)}, A]$
1	0	-1.A	$[\overline{A_{(n-1)}}, (-A)]$
1	1	0	All 0's

This can be explained with simple example

A=1100(-4)

X=1010(-6)

So,partial products obtained for these inputs using recoding scheme are shown in table1.

PP0=00000

PP1=00100

PP2=11100

PP3=00100

Multiplexers are important hardware for booth's recoding unit. Architecture of modified booth's recoding unit is shown in fig.2

in its architecture we have used 4 multiplexers out of which three are 4x1 and one is 2x1.each input vector is of n+1 of input bits of multiplier.

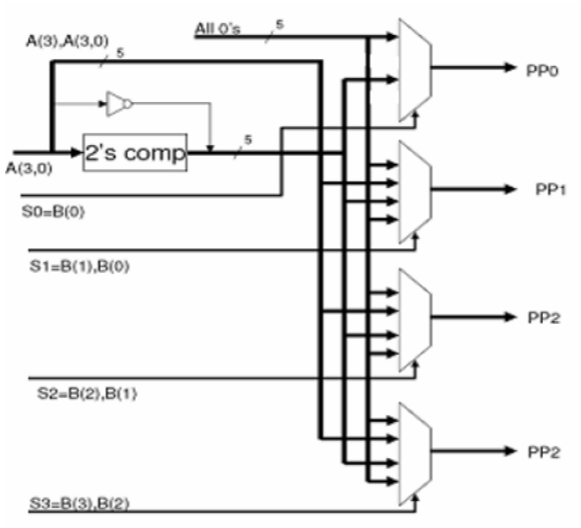

Fig.2 Architecture of booth's recoding unit radix2.

B.RADIX4

This is also same scheme as explained above that reduces partial products so it is very helpful for fast multiplication of long input bit sequences.but,here partial product which we got from recoding unit is always 2 bit more than input bits. If our input is of n bit then the partial products are of n+2 bit. Similar to radix2,radix4 partial product generation also depends on booths recoding table, which is shown in below table2.

Table 2.booth's recoding table for radix-4

X_{i+1}	X_i	X_{i-1}	Y	Partial Product Explanation
0	0	0	0	All 0's
0	0	1	1.A	$[A_{(n)}, A_{(n)}, A]$
0	1	0	1.A	$[A_{(n)}, A_{(n)}, A]$
0	1	1	2.A	$[A_{(n)}, A, 0]$
1	0	0	-2.A	$[\overline{A_{(n-1)}}, -A, 0]$
1	0	1	-1.A	$[\overline{A_{(n-1)}}, \overline{A_{(n-1)}}, -A]$
1	1	0	-1.A	$[\overline{A_{(n-1)}}, \overline{A_{(n-1)}}, -A]$
1	1	1	0	All 0's

Similar to the architecture of radix2, the architecture of radix4 will be drawn. In its architecture, we have used only 2 multiplexers. Where the 1st one is 4x1 and the 2nd one is 8x1[1].

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C.ADDITION SHEME:

The partial product addition scheme is similar to normal multiplication addition scheme except for MSB's.MSB's of partial products need to be added carefully. For that, new structure of an adder is proposed. The partial product adder arrays for 4bit input sequence using radix 2 and radix 4 algorithms are shown in fig.3 and fig.4.

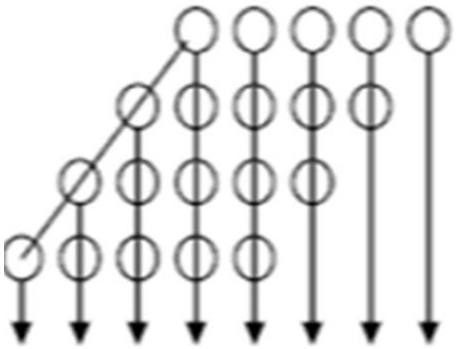

Fig.3.addition scheme for radix 2(4 bit input)

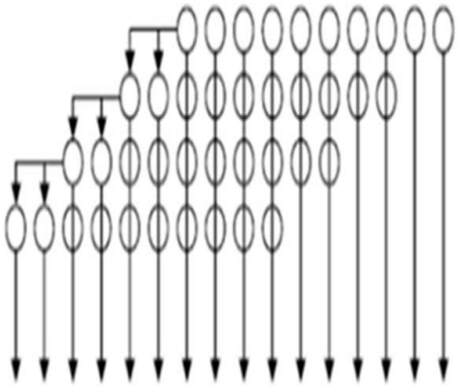

Fig 4.addition scheme for radix 4(8 bit inputs)

IV.PROPOSED VEDIC BOOTH MULTIPLIER

In section II basic Vedic mathematics was studied. In section III we discussed booth's radix4 algorithm. On comparing these two methods with respect to power and performance parameters, we observed that the performance of the Vedic multiplier is high compared to booth's radix4 algoritm.similarly, the power consumption in booth's radix4 algorithm is less compared to vedic multiplier. So, both the algorithms have it's own advantages and disadvantages. So, inorder to overcome with these drawbacks the proposed Vedic booth multiplier is used.

In this proposed design we will combine both the concepts of Vedic and booth's radix4 techniques. According to section II Vedic multiplier requires multipliers' internally to perform vertical and cross wise multiplication. Instead of using normal multipliers as internal multipliers in Vedic, if we use booth's radix4 multiplier, we can observe a lot of decrease in power and increase in performance i.e, decrease in delay in the proposed design compared to the existing methods.

Another advantage of the proposed design is, to design an 8 bit multipliers it requires two 4bit booth's radix 4multipliers.but in case of existing booth radix 4 ,to design higher order bits lower order multipliers are not used. Each and every higher order input multipliers the architecture will be changed. In both the cases. Let us see one example for this proposed design. The total procedure is similar to Vedic. Which is explained in section II. But ,In step III we will use booth's radix 4 algorithm to perform the multiplication.i.e,p1 p2 p3,p4 are generated using booth's radix 4 algorithm.

STEP1.below figure shows the partial product generation scheme in vedic booth multiplier.

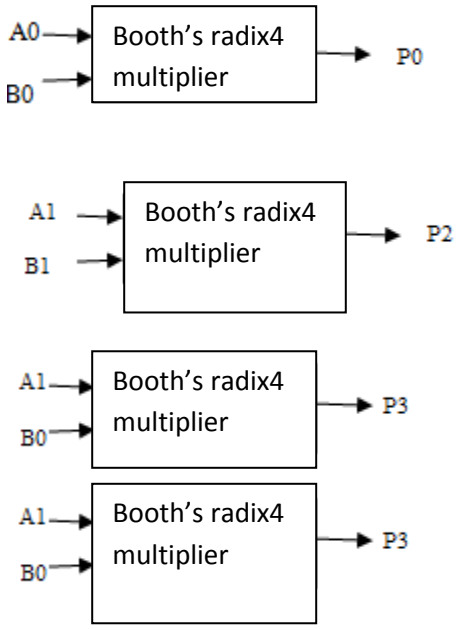

Fig.5.partial products generation using Vedic booth multiplier

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STEP 3: The result produced by the cross multiplication should be added here

i.e, let s1=> p3+p4=>00000000

STEP4: at last p1,p2,s1 should be added to produce the final result of the multiplier as shown in fig1.

V.RESULTS:

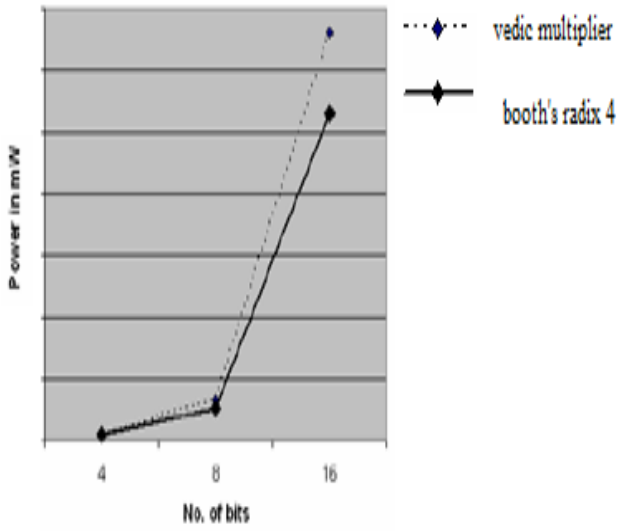

Fig 6.power comparison between existing methods

The proposed design has been simulated and synthesized using quartus II 9.1 and Xilinx 10.1.conventional booth's radix-4 algorithm and conventional Vedic mathematics has been taken as an ideal. We found that all the output results of the conventional methods and proposed methods are same. a synthesis result shows that area, power required for proposed design is less compared to the conventional methods. And it also shows that the performance of the multiplier was increased considerably compared to previous methods. As we move for larger number of input bits delay reduces as compared to the previous methods.

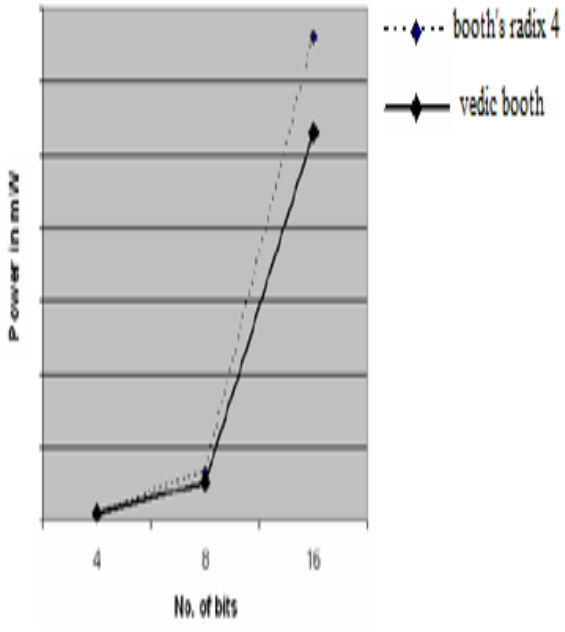

Fig.7.power comparison between booth's radix 4 and vedic booth multiplier

Table3: delay comparison between various multipliers

Number of input bits	Algorithm used	Delay(ns)
8	Booth's radix-4 algorithm	23.760
	Vedic multiplier design using normal multiplier	23.50
	Vedic multiplier design using booth's radix-4 algorithm	23.24
16	Booth's radix-4 algorithm	48.424
	Vedic multiplier design using normal multiplier	41.936
	Vedic multiplier design using booth's radix-4 algorithm	39.756

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table3. shows the delay comparision.the power comparison between various multipliers was shown in below fig.6 and fig.7

VI.CONCLUSION

From all these observations, we present vedic booth multiplier using both vedic mathematics and booth's radix-4 recoding algorithm. This multiplier is suitable for both signed and unsigned input vectors. More delay will be reduced for higher order input bits.

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