DESIGN AND IMPLEMENTATION OF BIST USING CPLD

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Abstract— **A new BIST scheme uses multiple single input change (MSIC) vector in a test pattern for testing low energy to increasing the switching activity. In this method SIC vector generator that is applied to each scan chain, this can decrease the switching activity in scan cells during scan shifting operation. The main goal of this technique to minimize the total power consumption during test mode in the BIST technique. For this purpose a reconfigurable Johnson counter or scalable SIC counter are used to generate a minimum transition sequences. MSIC-TPG sequences should not also to achieve the target fault coverage. To reduce the test power and low hardware overhead. By using this method easy to achieve both the test-per-clock and test-per-scan of test pattern applied to circuit under test (CUT) and implemented in VHDL. The experimental results are provided high performance which is applied to ISCAS circuitry. Design is verified on FPGA Spartan3E.**

Index terms: Built-in self-test (BIST), low power, single-input change (SIC), test pattern generator (TPG).

I. INTRODUCTION

The system on chip circuits depends on testing to eliminate various defects caused by the manufacturing process. With the advance in semiconductor manufacturing technology, VLSI device can now contain tens to hundreds of millions of transistor, increasing a chip complexity while maintaining its size. Many challenges are imposed on tools and methodologies used to design and test complex VLSI circuits. The most important issues in the development process of an integrated circuit during testing are manufacturing yield, product quality, and test cost. The test issues, Design for testability is a methodology that improves the testability, in terms of controllability and observability, thereby making the test generation and circuit fault coverage is east to test.

Test patterns are generator which is applied to the circuit under test (CUT) and to detect faulty circuits can be done either externally using automatic test equipment (ATE) or internally using built-in self-test (BIST). External testing using ATE are expensive and become more and more inefficient.

BIST is a fast becoming an alternative solution to Automatic test equipment, which is a design for testability method, which parts of the circuit are used to test the circuit itself. The test pattern generator generate the test pattern for the CUT. It compact and analyzes the test response to determine correctness of the CUT. A test control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions are executed through a test controller circuit.

II. BACKGROUND

Built-in self-test (BIST) method can be classified into two types (1) test-per-clock and (2) test-per-scan, according to the circuits are applied to circuit under test (CUT), in test pattern generation method. In test-per-clock BIST, the output of the test pattern generator are directly connected to the input of the circuit under test. Each test vectors are applied in every clock cycle from the Test pattern generation method, and the test responses are analyzed in the ORA and compared to a reference value. This advantage of the scheme has running much faster in applying the tests and higher fault coverage than test-per-scan BIST. The drawbacks of this scheme are high area overhead with scan design.

In test-per-scan BIST, also called scan-based BIST, a test pattern is applied to circuit under test are first shifted into the scan chains during shift operation; the test responses to these patterns are captured in scan cells during the capture operation. The test responses are shifted o to the ORA for response compaction while a new test is being shifted in. That uses a random pattern generator ,that is LFSR, it also uses MISR as the signature analyzer at the output of the scan chains to receive the response. Which can excessive power distribution. They can also damage the circuit product yield and lifetime. And also causing heat dissipation which may permanently damage the CUT.

several techniques are developed to reduce the power dissipated during scan-based test. Bit-swapping LFSR technique. In this technique, power reduction is possible, but

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speed will decrease by using this technique, power reduction of upto 63%. During the test mode is easy to implement, significantly increases the test application time. The design of low transition RTPGs, is one of the common and efficient techniques for low power test. These techniques can reduce the transitions in the scan inputs by assigning the same value to most neighboring bits in the scan chain. The main drawback of these algorithms lower fault coverage and higher test application time since some random features are lost in the patterns generated by these techniques. Another technique smoother is used at the output sequence of a LFSR, which is applied to scan-chain input of test-per-scan scheme.

This paper presents a new approach, a Multiple Single Input Change (MSIC) vectors are used as test pattern generators for BIST circuits. MSIC sequence had the favorable features of uniform distribution, low input transition density, and low area overhead. The proposed design achieves the target fault coverage without increasing the test length and also increase the test efficiency. Hence proposed TPG is flexible to both the test-per-clock and the test-per-scan schemes.

III. OVERVIEW

Proposed technique for designing on-chip test generators that can generate an effective test patterns are reducing the low transition density in the circuit under test. MSIC test vectors are converted to single input change vector and are applied in all the multiple scan chain using test pattern generation method.

The low power test pattern are generated while decreasing low transitions for each scan chain. The minimum transition sequence are used to generate an SIC vector are develop to either a reconfigurable Johnson counter or a scalable SIC counter. can to decrease the switching activity and low hardware overhead in scan cells. A Johnson counter is to generate an single input change sequence. For short scan length and to reduce the area overhead in scan length.

The MSIC-TPG of Test per clock schemes is illustrated in fig. 1, TPC BIST, vectors are applied in every clock cycle, from the TPG, and the test response are captured are output response analyzer, and compered to reference value. In this method is advantage of running faster in applying test and higher fault coverage then test per scan BIST. The main drawbacks of this method are high area overhead in scan design. In these test-per-scan to reduce the area overhead in scan design and thereby also reducing switching activity in test-per-scan of MSIC-TPG scheme is illustrated in fig.2.

The schematic view of the code help us to analyzer, our design by seeing a graphical in the RTL viewer. In test-per-clock and test-per-scan of Multiple single input change circuits has been implemented in VHDL programming language. Xilinx 14.2 ISE simulator is used to produce RTL schematic view for proposed BIST scheme. The RTL view for Test-per-Clock and Test-per-Scan as shown in fig. 3 and 4.

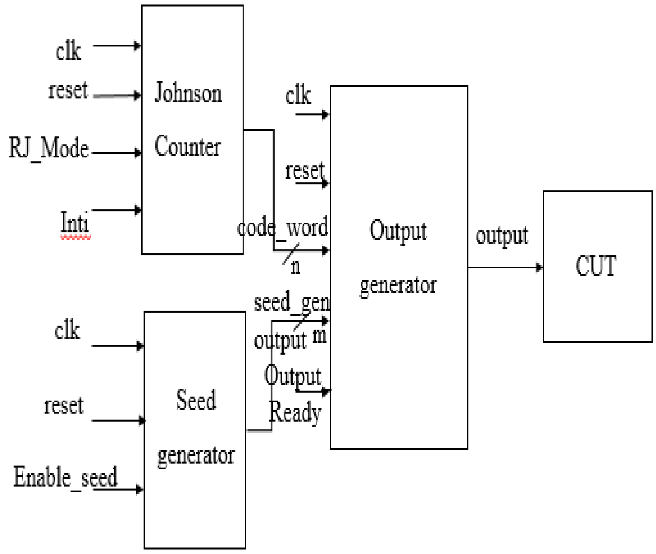

Fig.1. Test-per-clock MSIC-TPG structure

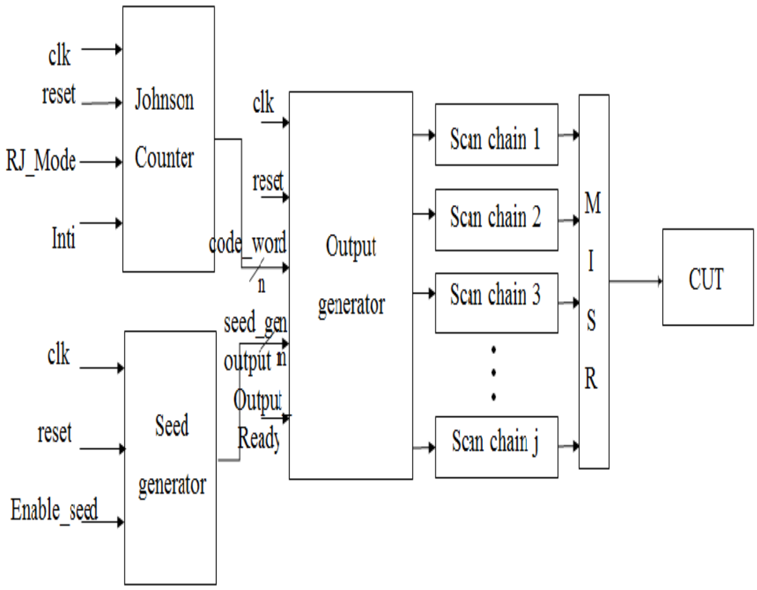

Fig.2. Test-per-scan MSIC-TPG structure

A. *Overview of the Algorithm*

The steps in the algorithm can be summarized as follows:

1) The seed generator generates a new seed by clocking CLK1 one time.

2) Johnson counter generates a new vector by clocking CLK2 one time.

3) After a new Johnson vector is generated, RJ_Mode and Init mode are set to 1. The reconfigurable Johnson counter

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operates as a circular shift register, and generates n johnson codewords by clocking CLK n times.

4) If 2n Johnson vectors are generated and XOR output of seed_generator with Johnson codeword in the output generator.

5) J number of scan chain are applied to output generator to achieved the minimum transition sequences.

6) The procedure are repeated until the expected fault coverage or test length is achieved.

B. Construction of a Reconfigurable Johnson Counter

A switch-tail ring counter, also known as the Johnson counter, if inverted output of last flip flop is connected to the input of first flip flop. If these register cycles which is applied to a sequence of bit-patterns. The fig.5, shows that the reconfigurable Johnson counter, it consists of AND gate, mux, and n number of D flip flop is used. If n represents the maximum scan chain number, and MUX is used to select the mode of operation.

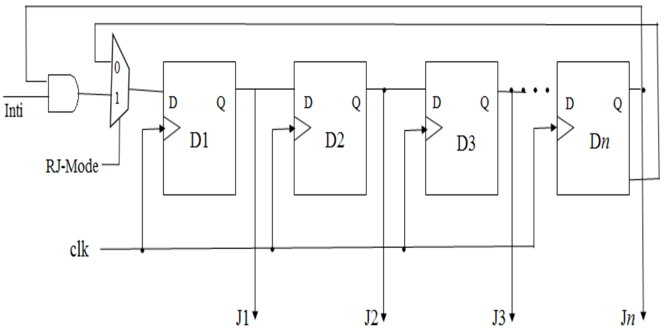

Fig. 3. Reconfigurable Johnson counter structure

Three mode of operation in Johnson counter.

1) Initialization

When RJ_Mode is set to logic 1 and Init is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK more than n times.

2) Circular shift register mode

When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will output of Johnson codeword by clocking CLK n times.

3) Normal mode

When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate 2n unique SIC vectors by clocking CLK2 2n times.

In the MSIC pattern, each generated vector applied to each scan chain is an SIC vector, which can minimize the input transition and reduce test power. Hence uniqueness of pattern is also achieved, these sequence does not contain any repeated patterns, and also meet the requirement of the target fault coverage for the CUT. Hence, the MSIC TPG can be easily implemented by hardware.

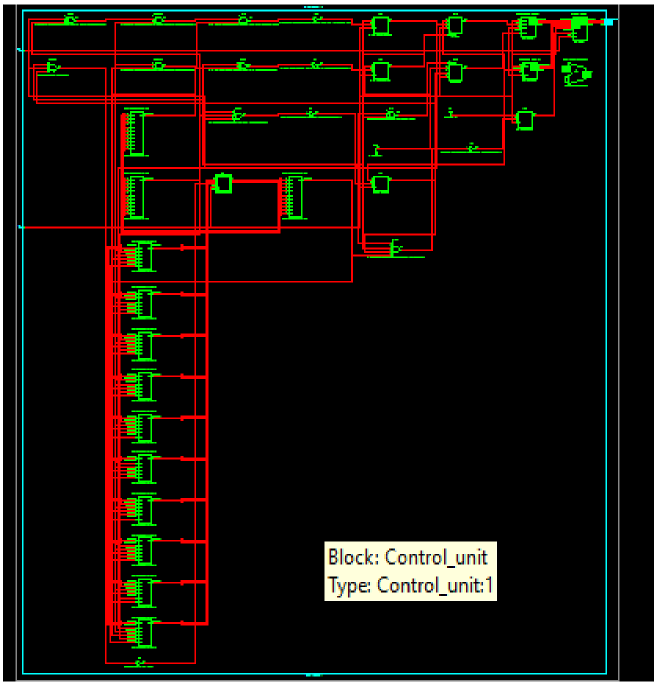

Fig. 4. RTL schematic for Test-per-Clock

Fig.5. RTL schematic for Test-per-Scan

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IV. RESULT

The ModelSim simulator using verifying the operation. The Xilinx 14.2 ISE simulator tool is verifying the area and power reduction output of the design. It produces the waveform can be analyzed the waveform for test-per-clock and test-per-scan are displayed in fig. 6 and fig. 7. The total number of flip flops and logic gates that are used for test-per-clock are 74 and 139. And the test-per-scan flip flop are used for 152. Hence the design summary provide a device result, and a list of all the messages generated by the implementation device as shown in the fig. 8.

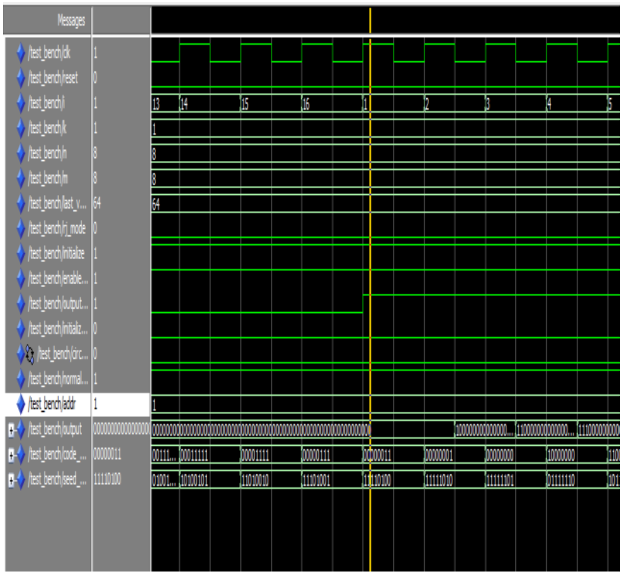

Fig. 6. Waveform for Test-per-Clock

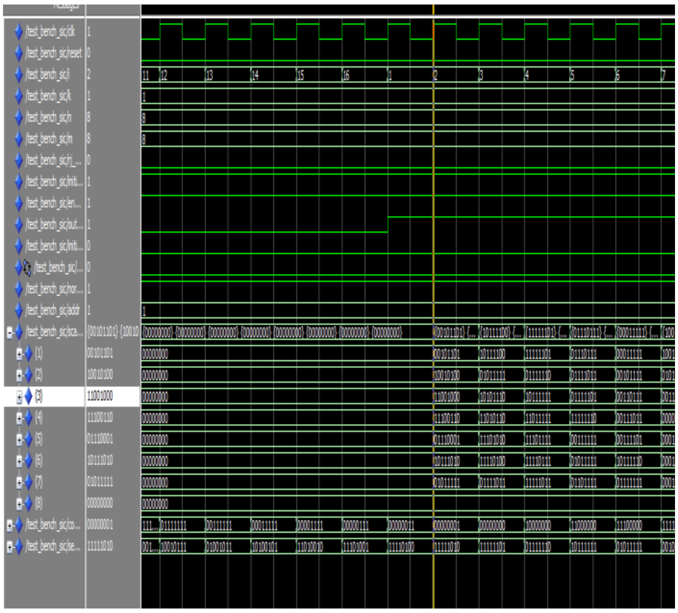

Fig.7. Waveform for Test-per-scan

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	152	9,312	1%
Number of 4 input LUTs	2,640	9,312	28%
Number of occupied Slices	2,359	4,656	50%
Number of Slices containing only related logic	2,359	2,359	100%
Number of Slices containing unrelated logic	0	2,359	0%
Total Number of 4 input LUTs	4,579	9,312	49%

Fig.8. Synthesis Result

The result of compilation of Xpower analyzer

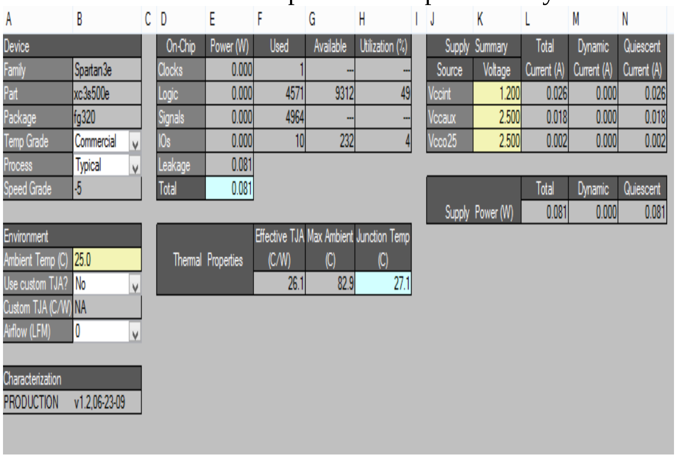

Fig.9. Power analysis

V. CONCLUSIONS

This paper has proposed a new low power test pattern generation method of Multiple single input change is achieved during the transition of test mode. The power consumption or our system has low power because of the low transition behavior of the system. Low switching activity in the Circuit under test are also reduced by using Single input change sequence. Combined with the proposed reconfigurable Johnson counter and scalable SIC counters. The MSIC-TPG can be easily implemented in flexible to Test-per-clock and Test-per-scan technique. Implementation of the above work into hardware will be carried out the design. And also the ISCAS benchmark circuits will be tested based on this proposed technique.

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