

Implementation of Data Encoding and Decoding Architecture for NOC Application

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Abstract— In this paper we present data encoding and decoding schemes to reduce the power dissipation of the communication system in a Network-on-Chip (NoC). In NoC the major source of power dissipation is the network on chip links. The self-switching and coupling-switching activities are responsible for link power dissipation. In this paper we present a set of data encoding and decoding schemes operating at flit level and on an end-to-end basis, which allows us to minimize both self and coupling switching activities. The self-switching is reduce by checking the switching transition and then the coupling technique is incorporated with the wormhole routed network, that is flits are encoded by the network interface before they are injected in the network and are decoded by the destination NI (network interface). Especially the decoding schemes are focused on reducing hardware. This paper analyzes the power and delay reduction of both encoding and decoding schemes in Xilinx Virtex-5 family (XC5VLX50).

Index Terms— Data encoding, Data decoding, Network-on-Chip (NoC), Links, Coupling switching activity, Wormhole routed network.

I. INTRODUCTION

As the number of IP modules in System-on-Chip (SoC) increases, bus-based interconnection architectures may prevent these systems to meet the performance required by many applications. For systems with intensive parallel communication requirements buses may not provide the required bandwidth, latency, and power consumption. A solution for such a communication bottleneck is the use of switching network, called Network-on-chip (NoC). NoC is an on chip packet based communication system between blocks connected via routers. However, in recent years research has shown that Network-on-Chip (NoC) is likely to replace buses in future SoCs [1].

NoC architectures popularity comes directly from the growing interest around System-on-Chip (SoC) and Multi-Processor-System-on-Chip (MPSoC) technologies. NoC topology is composed by an arbitrary number of instances of three basic kind of functional blocks Network Interfaces, Switches and Links. Network Interfaces connect all the IP cores to the network. Switches carry out the task of dispatching packets inside the network, depending on the particular routing scheme. Links connect switches with NIs is shown in the Fig.1.

In this paper, we focus on techniques aimed at reducing the power dissipated by the network links. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution

is expected to increase as technology scales [2]. In particular, we present a set of data encoding and decoding schemes operating at flit level and on an end-to-end basis, which allows us to minimize both the self and coupling switching activities on links of the routing paths traversed by the packets. The proposed data encoding and decoding schemes, which are transparent with respect to the router implementation, are presented and discussed at both the algorithmic level and the architectural level. The analysis takes into account several aspects and metrics of the design, including silicon area, delay, power dissipation and energy consumption.

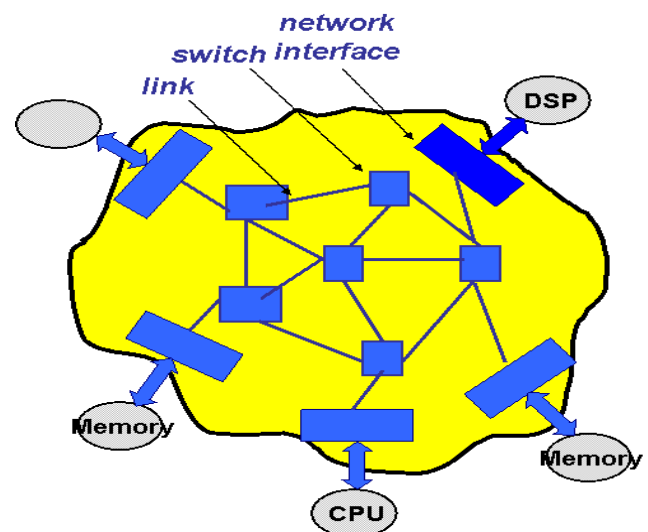


Fig.1 Network on chip topology

The rest of this paper is organized as follows. We briefly discuss related works in Section II. The proposed data encoding and decoding schemes along with possible hardware implementations and their analysis are described in Section III. In Section IV proposed data encoding and decoding schemes are simulated and verified using verilog HDL in Xilinx ISE 10.1i for the target device xc3s500e-5fg320. Finally, this paper is concluded in Section V.

II. RELATED WORKS AND CONTRIBUTIONS

This paper concentrates on reducing the power dissipated by the links. The data encoding scheme is one of the major method that was employed to reduce the link power dissipation. The data encoding techniques may be classified into two categories. In that first category, Bus invert (BI) encoding method is widely used technique to reduce dynamic

switching power. The basic idea behind Bus invert (BI) encoding method originated by noting that a lot of power is wasted during data transmission in off-chip bus lines. This is due to the switching of the high capacitance lines, therefore power could be saved by minimizing the number of transitions occurring on these bus lines. The Bus invert method uses one extra control bit called invert. By convention then invert = 0 the bus value will equal the data value. When invert = 1 the bus value will be the inverted data value [3] is shown in the below figure.

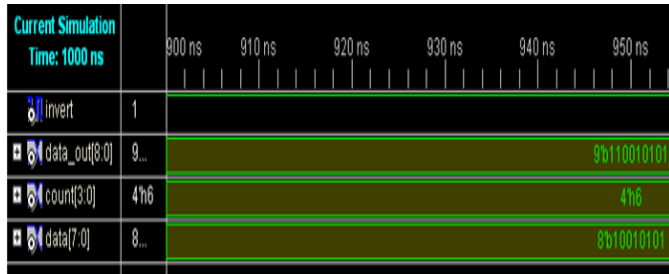


Fig.2 Bus-invert Encoding method

So the first category of encoding technique concentrates on lowering the power due to self-switching activity of individual bus lines. In that second category, gray code encoding method is widely used technique to reduce power dissipation by minimizing the coupling transition activities on the links of the interconnection network and to reduce errors using gray code. It consists of a binary to gray converter, encoder, decoder and gray to binary converter.

The binary to gray converter is used to convert the input data to gray number since it is used to facilitate error correction in digital communication [4] is shown in the below figures.

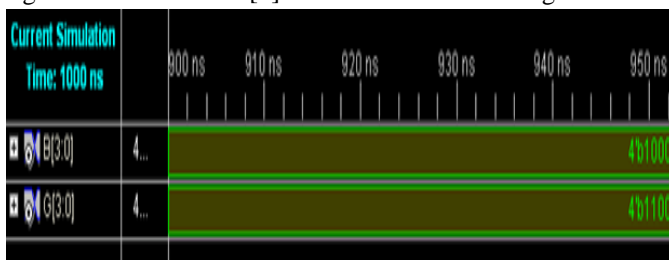


Fig.3 binary to gray conversion

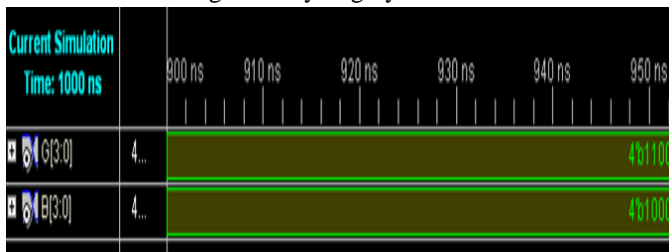


Fig.4 gray to binary conversion

The self-switching activity and coupling-switching activity causes the power dissipation due to the self transitions and coupling transitions. Self transition on the data bus is defined

as transition on the capacitance between a data bus line and the substrate. Coupling transition on data bus is defined as transition on capacitance between adjacent bus lines [5].

In this paper, we present three proposed encoding schemes. In scheme I, we make use half inversion and focus on reducing Type I transitions. In scheme II, both Types I and II transitions are taken into account for deciding between half and full invert, depending the amount of switching reduction. Finally in scheme III, we consider the fact that Type I transitions show different behaviors in the case of odd and even inverts [6] and make the inversion which leads to the higher power saving.

TABLE I

EFFECT OF ODD INVERSION ON CHANGE OF TRANSITION TYPES

Time	Normal			Odd Inverted		
	Type I			Types II,III, and IV		
$t - 1$	00,11	00,11,01,10	01,10	00,11	00,11,01,10	01,10
t	10,01	01,10,00,11	11,00	11,00	00,11,01,10	10,01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t - 1$	Type II			Type I		
t	01,10			01,10		
	10,01			11,00		
$t - 1$	Type III			Type I		
t	00,11			00,11		
	11,00			10,01		
$t - 1$	Type IV			Type I		
t	00,11,01,10			00,11,01,10		
	00,11,01,10			01,10,00,11		

III. PROPOSED ENCODING AND DECODING SCHEMES

In this section, we present the proposed encoding scheme and decoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activities on the links of the interconnection network. Let us first describe the power model that contains different components of power dissipation of a link. The dynamic power dissipated by the interconnects and drivers is

$$P = [T_{0 \rightarrow 1} (C_s + C_l) + T_c C_c] V_{dd}^2 F_{ck} \quad (1)$$

Where $T_{0 \rightarrow 1}$ is the number of 0→1 transitions in the bus in two consecutive transmissions, T_c is the number of correlated switching between physically adjacent lines, C_s is the line to substrate capacitance, C_l is the load capacitance, C_c is the coupling capacitance, V_{dd} is the supply voltage, and F_{ck} is the clock frequency. One can classify four types of coupling transitions as described in [7].

A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high while the other makes transition from high to low. A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change.

The effective switched capacitance varies from type to type, and hence, the coupling transition activity, T_c is a weighted sum of different types of coupling transition contributions [7].

Therefore

$$T_c = K_1 T_1 + K_2 T_2 + K_3 T_3 + K_4 T_4 \quad (2)$$

Where T_i is the average number of Type i transition and K_i is its corresponding weight. According to [7], we use $K_1=1$, $K_2=2$, and $K_3=K_4=0$. The occurrence 1/2 and 1/8, respectively. This leads to a higher value for $K_1 T$ compared with $K_2 T$ suggesting that minimizing the number of Type I transition may lead to a considerable power reduction. Using (2), one may express (1) as

$$P = [T_{0 \rightarrow 1} (C_s + C_l) + (T_1 + 2T_2) C_c] V_{dd}^2 F_{ck} \quad (3)$$

According to [3], C_l can be neglected

$$P \propto T_{0 \rightarrow 1} C_s + (T_1 + 2T_2) C_c \quad (4)$$

Here, we calculate the occurrence probability for different types of transitions. Consider that flit ($t - 1$) and flit (t) refer to the previous flit which was transferred via the link and the flit which is about to pass through the link, respectively. We consider only two adjacent bits of the physical channel. Sixteen different combinations of these four bits could occur (Table I). Note that the first bit is the value of the generic i th line of the link, whereas the second bit represents the value of its $(i + 1)$ th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively. In the rest of this section, we present three data encoding schemes designed for reducing the dynamic power dissipation of the network links along with a possible hardware implementation of the decoder.

A. Scheme I

In scheme I, we focus on reducing the numbers of Type I transitions (by converting them to Types III and IV transitions) and Type II transitions (by converting them to Type I transition). The scheme compares the current data

with the previous one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction.

1) *Power Model*: If the flit is odd inverted before being transmitted, the dynamic power on the link is

$$P' \propto T'_{0 \rightarrow 1} + (K_1 T'_1 + K_2 T'_2 + K_3 T'_3 + K_4 T'_4) C_c \quad (5)$$

Where $T'_{0 \rightarrow 1}$, T'_1 , T'_2 , T'_3 and T'_4 are the self transition activity, and the coupling transition activity of Types I, II, III and IV, respectively. Table I reports, for each transition, the relationship between the coupling transition activities of the flit when transmitted as is and when its bits are odd inverted. Data are organized as follows. The first bit is the value of the generic i th line of the link, whereas the second bit represents the value of its $(i + 1)$ th line. For each partition, the first (second) line represents the values at time $t-1$ (t). As Table I shows, if the flit is odd inverted, Types II, III, and IV transitions convert to Type I transitions. In the case of Type I transitions, the inversion leads to one of Types II, III, or Type IV transitions. In particular, the transitions indicated as T_1^* , T_1^{**} , and T_1^{***} in the table convert to Types II, III, and IV transitions, respectively. Also, we have $T'_{0 \rightarrow 1} = T_{0 \rightarrow 0(\text{odd})} + T_{0 \rightarrow 1(\text{even})}$ where odd/even refers to odd/even lines. Therefore, (5) can be expressed as

$$P' \propto (T_{0 \rightarrow 0(\text{odd})} + T_{0 \rightarrow 1(\text{even})}) C_s + [K_1 (T_2 + T_3 + T_4) + K_2 T_1^{***} + K_3 T_1^* + K_4 T_1^{**}] C_c \quad (6)$$

Thus, if $P > P'$, it is convenient to odd invert the flit before transmission to reduce the link power dissipation. Using (4) and (6) and noting that $C_c / C_s = 4$ [7], we obtain the following odd invert condition

$$\frac{1}{4} T_{0 \rightarrow 1} + T_1 + 2T_2 > \frac{1}{4} (T_{0 \rightarrow 0(\text{odd})} + T_{0 \rightarrow 1(\text{even})}) + T_2 + T_3 + T_4 + 2T_1^{***} \quad (7)$$

Also, since $T_{0 \rightarrow 1} = (T_{0 \rightarrow 1(\text{odd})} + T_{0 \rightarrow 1(\text{even})})$, one may write

$$\frac{1}{4} T_{0 \rightarrow 1(\text{odd})} + T_1 + 2T_2 > \frac{1}{4} T_{0 \rightarrow 0(\text{odd})} + T_2 + T_3 + T_4 + 2T_1^{***} \quad (7)$$

Which is the exact condition to be used to decide whether the odd invert has to be performed. Since the terms $T_{0 \rightarrow 1(\text{odd})}$ and $T_{0 \rightarrow 0(\text{odd})}$ are weighted with a factor of 1/4, for link widths greater than 16 bits, the misprediction of the invert condition will not exceed 1.2% on average. Thus, we can approximate the exact condition as

$$T_1 + 2T_2 > T_2 + T_3 + T_4 + 2T_1^{***} \quad (8)$$

of course, the use of the approximated odd invert condition reduces the effectiveness of the encoding scheme due to the error induced by the approximation but it simplifies the hardware implementation of encoder. Now, defining

$$T_x = T_3 + T_4 + T_1^{***}$$

and

$$T_y = T_2 + T_1 - T_1^{***} \quad (9)$$

One can rewrite (8) as

$$T_y > T_x \quad (10)$$

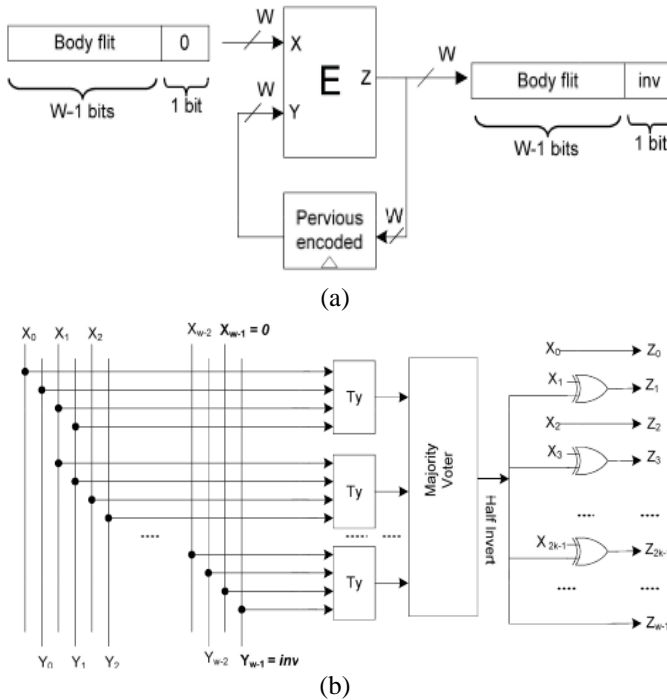


Fig.5 Encoder architecture scheme I. (a) Circuit diagram (b) Internal view of the encoder block (E).

Assuming the link width of w bits, the total transition between adjacent lines is $w - 1$, and hence

$$T_y + T_x = w - 1 \quad (11)$$

Thus, we can write (10) as

$$T_y > (w - 1)/2 \quad (12)$$

This presents the condition used to determine whether the odd inversion has to be performed or not.

2) *Proposed Encoding Architecture*: The proposed encoding architecture, which is based on the oddinvert condition defined by (12), is shown in Fig.1. We consider a link width of w bits. If no encoding is used, the body flits are grouped in w bits by the NI and are transmitted via the link. In our approach, one bit of the link is used for the inversion bit, which indicates if the flit traversing the link has been inverted or not. More specifically, the NI packs the body flits in $w - 1$ bits [Fig. 1(a)]. The encoding logic E, which is integrated into the NI, is responsible for deciding if the inversion should take place and performing the inversion if needed. The generic block diagram shown in Fig. 1(a) is the same for all three encoding schemes proposed in this

paper and only the block E is different for the schemes. To make the decision, the previously encoded flit is compared with the current flit being transmitted. This latter, whose w bits are the concatenation of $w-1$ payload bits and a “0” bit, represents the first input of the encoder, while the previous encoded flit represents the second input of the encoder [Fig. 1(b)]. The $w-1$ bits of the incoming (previous encoded) body flit are indicated by X_i (Y_i), $i = 0, 1, \dots, w-2$. The w th bit of the previously encoded body flit is indicated by inv which shows if it was inverted ($inv = 1$) or left as it was ($inv = 0$). In the encoding logic, each T_y block takes the two adjacent bits of the input flits (e.g., $X_1X_2Y_1Y_2$, $X_2X_3Y_2Y_3$, $X_3X_4Y_3Y_4$, etc.) and sets its output to “1” if any of the transition types of T_y is detected. This means that the odd inverting for this pair of bits leads to the reduction of the link power dissipation (Table I). The T_y block may be implemented using a simple circuit. The second stage of the encoder, which is a majority voter block, determines if the condition given in (12) is satisfied (a higher number of 1s in the input of the block compared to 0s). If this condition is satisfied, in the last stage, the inversion is performed on odd bits. The decoder circuit simply inverts the received flit when the inversion bit is high.

B. Scheme II

In the proposed encoding scheme II, we make use of both odd (as discussed previously) and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction.

1) *Power Model*: Let us indicate with P , P' and P'' the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, and full inversion, respectively. The odd inversion leads to power reduction when $P' < P''$ and $P' < P$. The power P'' is given by

$$P'' \propto T_1 + 2T_4^{**} \quad (13)$$

Neglecting the self-switching activity, we obtain the condition $P' < P''$ as

$$T_2 + T_3 + T_4 + 2T_1^{***} < T_1 + 2T_4^{**} \quad (14)$$

Therefore, using (9) and (11), we can write

$$2(T_2 - T_4^{**}) < 2T_y - w + 1 \quad (15)$$

Based on (12) and (15), the odd inversion condition is obtained as

$$2(T_2 - T_4^{**}) < 2T_y - w + 1 \quad T_y > (w-1)/2 \quad (16)$$

Similarly, the condition for the full inversion is obtained from $P'' < P$ and $P'' < P'$. The inequality $P'' < P$ is satisfied when

$$T_2 > T_4^{**} \tag{17}$$

Therefore, using (15) and (17), the full inversion condition is obtained as

$$2(T_2 - T_4^{**}) > 2T_y - w + 1 \tag{18}$$

When none of (16) or (18) is satisfied, no inversion will be performed.

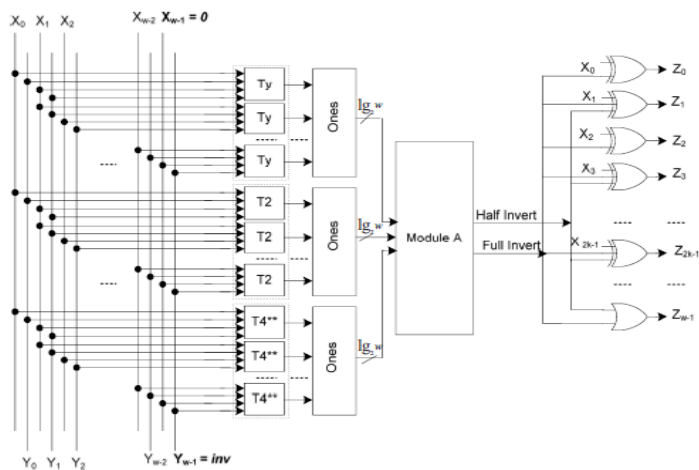
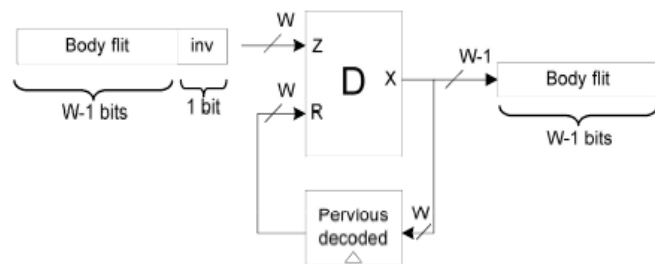
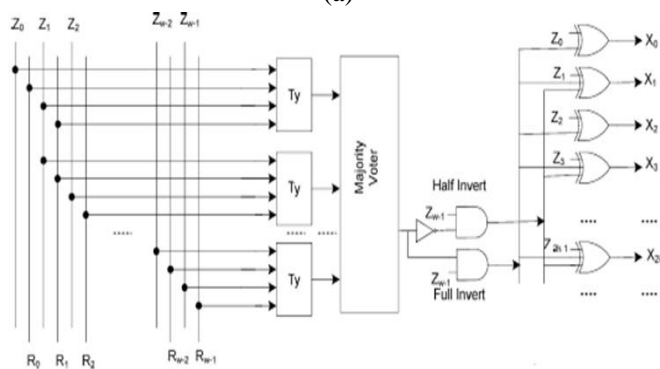


Fig.6 Encoder architecture Scheme II

2) *Proposed Encoding Architecture:* The operating principles of this encoder are similar to those of the encoder implementing Scheme I. The proposed encoding architecture, which is based on the odd invert condition of (16) and the full invert condition of (18), is shown in Fig. 2. Here again, the *w*th bit of the previously and the full invert condition of (18) is shown in Fig. 2. Here again, the *w*th bit of the previously encoded body flit is indicated with *inv* which defines if it was odd or full inverted (*inv* = 1) or left as it was (*inv* = 0). In this encoder, in addition to the *T_y* block in the Scheme I encoder, we have the *T₂* and *T₄* blocks which determine if the inversion based on the transition types *T₂* and *T₄* should be taken place for the link power reduction. The second stage is formed by a set of 1s blocks which count the number of 1s in their inputs. The output of these blocks has the width of $\log_2 w$. The output of the top 1s block determines the number of transitions that odd inverting of pair bits leads to the link power reduction. The middle 1s block identifies the number of transitions whose full inverting of pair bits leads to the link power reduction. Finally, the bottom 1s block specifies the number of transitions whose full inverting of pair bits leads to the increased link power. Based on the number of 1s for each transition type, Module A decides if an odd invert or full invert action should be performed for the power reduction.



(a)



(b)

Fig.7 Decoder architecture Scheme II. (a) Circuit diagram. (b) Internal view of the decoder block (D).

For this module, if (16) or (18) is satisfied, the corresponding output signal will become “1.” In case no invert action should be taken place, none of the output is set to “1.” Module A can be implemented using full-adder and comparator blocks. The circuit diagram of the decoder is shown in Fig. 3. The *w* bits of the incoming (previous) body flit are indicated by *Z_i* (*R_i*), *i* = 0, 1, . . . , *w* - 1. The *w*th bit of the body flit is indicated by *inv* which shows if it was inverted (*inv* = 1) or left as it was (*inv* = 0). For the decoder, we only need to have the *T_y* block to determine which action has been taken place in the encoder. Based on the outputs of these blocks, the majority voter block checks the validity of the inequality given by (12). If the output is “0” (“1”) and the *inv* = 1, it means that half (full) inversion of the bits has been performed. Using this output and the logical gates, the inversion action is determined. If two inversion bits were used, the overhead of the decoder hardware could be substantially reduced.

C. Scheme III

In the proposed encoding Scheme III, we add even inversion to Scheme II. The reason is that odd inversion converts some of Type I (*T₁*) transitions to Type II transitions. As can be observed from Table II, if the flit is even inverted, the transitions indicated as *T₁***/*T₁* in the table are converted to Type IV / Type III transitions. Therefore, the even inversion may reduce the link power dissipation as well. The scheme compares the current data with the previous one to decide

whether odd, even, full, or no inversion of the current data can give rise to the link power reduction.

1) *Power Model*: Let us indicate with P' , P'' , and P''' the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, full inversion, and even inversion, respectively. Similar to the analysis given for Scheme I, we can approximate the condition $P''' < P$ as

$$T_1 + 2T_2 > T_2 + T_3 + T_4 + 2T_1^* \quad (19)$$

TABLE II

EFFECT OF EVEN INVERSION ON CHANGE OF TRANSITION TYPES

Time	Normal			Odd Inverted		
	Type I			Types II,III, and IV		
$t-1$	01,10	00,11,01,10	00,11	01,10	00,11,01,10	00,11
t	00,11	10,01,11,00	01,10	10,01	00,11,01,10	11,00
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01,10			01,10		
	10,01			00,11		
$t-1$	Type III			Type I		
t	00,11			00,11		
	11,00			01,10		
$t-1$	Type IV			Type I		
t	00,11,01,10			00,11,01,10		
	00,11,01,10			10,01,11,00		

Defining

$$T_e = T_2 + T_1 - T_1^* \quad (20)$$

We obtain the condition $P''' < P$ as

$$T_e > (w - 1)/2 \quad (21)$$

Similar to the analysis given for scheme II, we can approximate the condition $P''' < P'$ as

$$T_2 + T_3 + T_4 + 2T_1^* < T_2 + T_3 + T_4 + 2T_1^{***} \quad (22)$$

Using (9) and (20), we can rewrite (22) as

$$T_e > T_y \quad (23)$$

Also, we obtain the condition $P''' < P''$ as [see (13) and (19)]

$$T_2 + T_3 + T_4 + 2T_1 < T_1 + 2T_4^{**} \quad (24)$$

Now, define

$$T_r = T_3 + T_4 + T_1^*$$

and

$$T_e = T_2 + T_1 - T_1^* \quad (25)$$

Assuming the link width of w bits, the total transition between adjacent lines is $w - 1$, and hence

$$T_e + T_r = w - 1 \quad (26)$$

Using (26), we can rewrite (24) as

$$2(T_2 - T_4^{**}) < 2T_e - w + 1 \quad (27)$$

The even inversion leads to power reduction when $P''' < P$, $P'' < P'$, and $P''' < P''$. Based on (21), (23), and (27),

We obtain

$$T_e > (w-1)/2, T_e > T_y, 2(T_2 - T_4^{**}) < 2T_e - w + 1 \quad (28)$$

The full inversion leads to power reduction when $P''' < P'$, $P'' < P'$, and $P''' < P''$. Therefore, using (18) and (27), the full inversion condition is obtained as

$$2(T_2 - T_4^{**}) > 2T_y - w + 1, (T_2 > T_4^{**}) \quad (29)$$

Similarly, the condition for the odd inversion is obtained from $P' < P$, $P' < P''$, and $P' < P'''$. Based on (16) and (23), the odd inversion condition is satisfied when

$$2(T_2 - T_4^{**}) < 2T_y - w + 1, T_y > (w - 1)/2 \quad (30)$$

When none of (28), (29), or (30) is satisfied, no inversion will be performed.

2) *Proposed Encoding Architecture*: The operating principles of this encoder are similar to those of the encoders implementing Schemes I and II. The proposed encoding architecture, which is based on the even invert condition of (28), the full invert condition of (29), and the odd invert condition of (30), is shown in Fig. 4. The w th bit of the previously encoded body flit is indicated by *inv* which shows if it was even, odd, or full inverted ($inv = 1$) or left as it was ($inv = 0$). The first stage of the encoder determines the transitions types while the second stage is formed by set of 1s blocks which counts the number of ones in their inputs. In the first stage, we have added the T_e blocks which determine if any of the transition types of T_2 , T_1^{**} , and T_1 is detected for each pair bits of their inputs. For these transition types, the even invert action yields link power reduction. Again which determine if any of the transition types of T_2 , T_1^{**} , and T_1 is detected for each pair bits of their inputs. For these transition types, the even invert action yields link power reduction. Again, we have four Ones blocks to determine the number of detected transitions for each T_y , T_e , T_2 , T_4^{**} , blocks. The output of the Ones blocks are inputs for Module C. This module determines if odd, even, full, or no invert action corresponding to the outputs “10,” “01,” “11,” or “00,” respectively, should be performed. The outputs “01,” “11,” and “10” show that whether (28), (29), and (30), respectively, are satisfied. In this paper, Module C was designed based on the conditions given

in (28), (29), and (30). Similar to the procedure used to design the decoder for scheme II, the decoder for scheme III designed shown in the below figure.

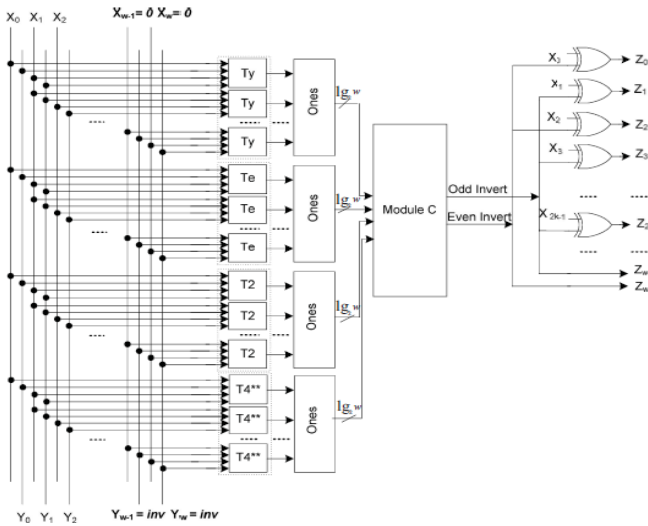


Fig.8 Encoder architecture Scheme III

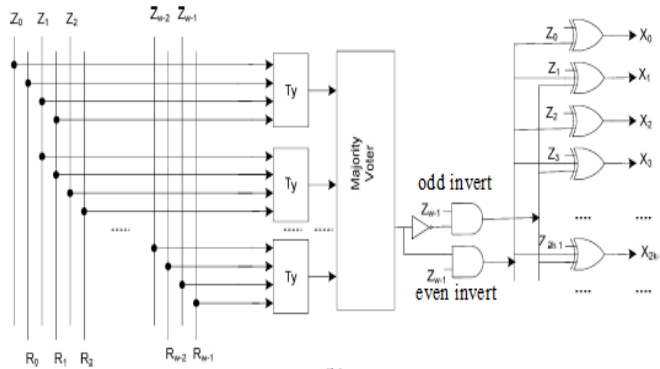
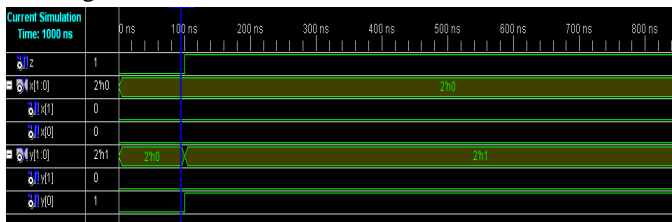


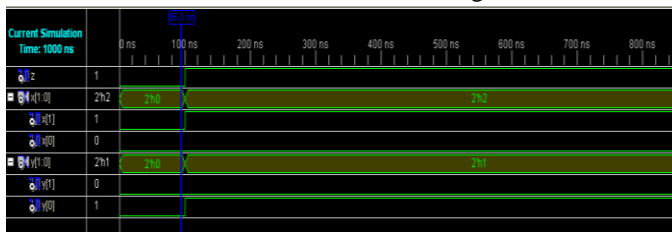
Fig.9 Decoder internal view of scheme III

IV. RESULTS AND DISCUSSION

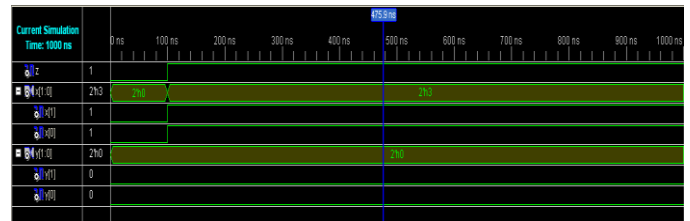
The proposed Encoding and Decoding schemes include four types of transitions. A Type I transition occurs when one of the lines switches when the other remains unchanged.



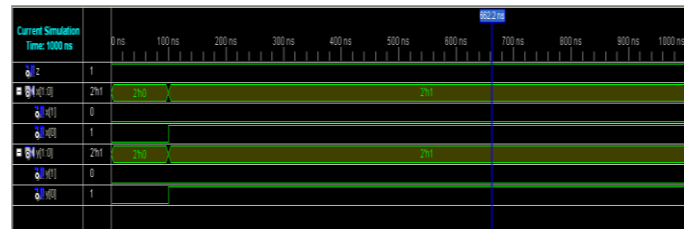
In a Type II transition, one line switches from low to high while the other makes transition from high to low.



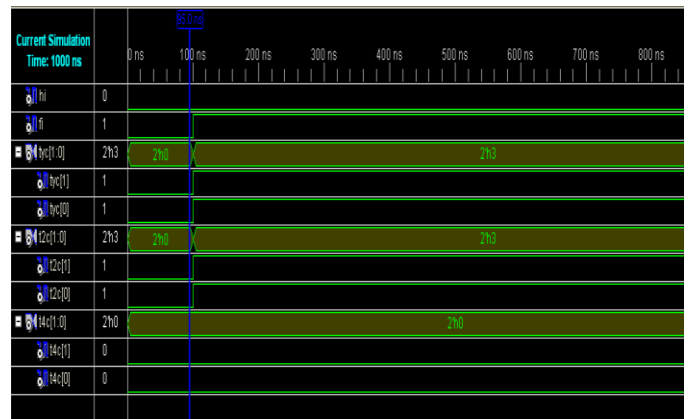
Type III transition corresponds to the case where both lines switch simultaneously.



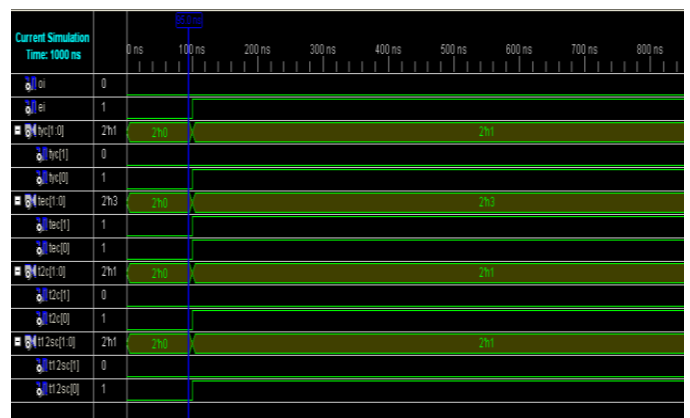
Finally, in a Type IV transition both lines do not change.



In the proposed encoding scheme I, we make use half invert and in scheme II, we make use of both half and full inversion.



Finally in scheme III, we make use even inversion and odd inversion.



Delay in existing method

EXISTING METHOD	DELAY
(First category)Bus-Invert	30.77 ns

Delay in proposed schemes

PROPOSED SCHEME	DELAY
SCHEME 1(half invert)	5.895 ns
SCHEME 2 (half and full inversion)	4.632 ns
SCHEME 3(even and odd inversion)	4.632 ns

The proposed Encoding and Decoding schemes are simulated and verified using Verilog HDL in Xilinx ISE 10.1i for the target device xc3s500e-5fg320.

V. CONCLUSION

In this paper, we have presented a set of new data encoding and decoding schemes aimed at reducing the power dissipated by the links of an NoC. In fact, links are responsible for a significant fraction of the overall power dissipated by the communication system. In addition, their contribution is expected to increase in future technology nodes. As compared to the previous encoding schemes proposed in the literature, the rationale behind the proposed schemes is to minimize not only the switching activity, but also (and in particular) the coupling switching activity which is mainly responsible for link power dissipation in the deep submicrometer technology regime. The proposed encoding schemes are agnostic with respect to the underlying NoC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder logic in the NI. The encoders implementing the proposed schemes have been assessed in terms of power dissipation and silicon area. Especially the decoders are mainly focused on reducing hardware. Overall, the application of the proposed encoding and decoding schemes allows savings up to 51% of power dissipation and 14% of energy consumption without any significant performance. The proposed Encoding and Decoding schemes are simulated and verified using Verilog HDL in Xilinx ISE 10.1i.

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