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An Efficient High-Speed 9-bit Parity Checker using 4-2 Compressors

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Abstract **– In this paper, an efficient and simple implementation of 9- bit parity checker design using 4-2 Compressors is presented; for generation of quick results of parity, especially for use in Communications while transmission of binary message data from a transmitter side to a receiver side. Parity Checkers are used for single bit error detection in the receiver end. The Parity Checkers detects both odd and even parity bits and are used as monitoring devices on high speed communication lines. Using 4-2 Compressors in designing of Parity Checkers instead of conventional XOR modules is proven to have minimal output delay facilitating high speed communication; and further it leads to reduction in the power-delay product (PDP). The Simulation results were obtained using Synopsys HSPICE tool at 0.18µm standard CMOS technology.**

Keywords- 4-2 Compressors, Parity Checkers, Error Detection, XOR module, HSPICE tool, minimum Delay.

I. INTRODUCTION

With the growing necessitate for having high speed communication of data bits form a source/transmitter end to destination/receiver end. During the process of data transmission in the form of binary bits, it should be ensured that the data is error free i.e., no stuck-at or bridging faults etc., have occurred during transmission through a channel. There may be various reasons for occurrence of errors like power supply surges, interference due to electro-magnetic waves, cross-talk caused due to closely connected signal wires, logical noise etc., So, the detection of faults is a major concern for the present communications as the data transmission should not loose information that was sent.

Parity Checker is one method to detect the errors/ faults that have occurred during data transmission. The data will found defective, when the data entered at the receiver side has different parity compared to the parity present at the transmitter output. Most of the communication systems use parity checkers for detecting single bit errors. Having quick parity checker results will lead to fast validation of data bits and so if the data is proven to be valid, then the data bits are given to the receiver circuitry with very minimal delay. Occurrence of fault is detected by parity checker either considering even or odd parity.

This present paper is organised as follows, in section.2, Xor modules and 4-2 Compressors are discussed in detail. In section 3, Parity Checkers functioning is described. In section 4, our present parity checker design is explained. In section 5, the experimental results of the parity checker using compressors is evaluated next to normal parity checker of 9-bits. The work is at final concluded in Section 6.

II. XOR MODULES AND 4-2 COMPRESSOR DESIGN

A. XOR Module

A large number of XOR modules are present in literature. The XOR module is used as a building block in various circuits like Comparators, Oscillators, Multipliers, pulse generators etc., Static CMOS style XOR will use both nMOS and also pMOS transistors [2]. It consumes large amount of power and larger area as the transistors used are more. Feed-back transistors type of XOR-XNOR circuit uses pull-up and pull-down circuitry and so used at lower voltages, but the output response is slower as the input load is doubled [3]. So, it is convenient to use XOR gate as shown in Fig. 1, to have high speed performance with low power consumption and also uses only 6 transistors providing good driving capability [1].

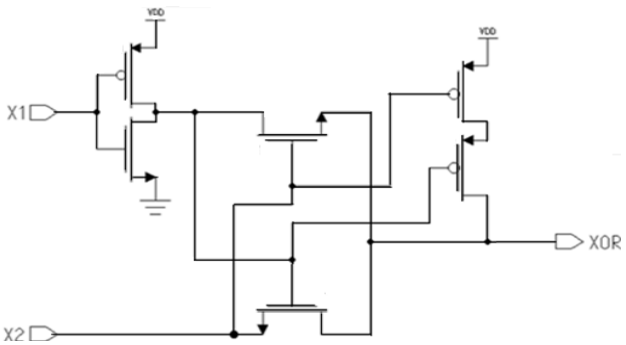

Fig.1: Circuit diagram of XOR for good driving capability.

B. 4-2 Compressor Design

A 4-2 Compressor has 5-inputs along with Cin (Carry-in) and it produces 3 outputs namely, Sum bit, Carry bit and Cout. In general, 4-2 Compressors are made from two 3-2 Compressors (Full Adder Cells). The delay of normal 4-2 Compressor is about 4 XOR delays. Efficient way of logical composition of 4-2 Compressor [4] will result in the critical path delay to one XOR and two multiplexer (MUX) delays.

The Multiplexer (MUX) with lesser critical delay [5] and lesser area is made of transmission gates. The transmission gate based multiplexer can be used in designing low power cells and consumes only just 6 transistors. MUX is to be used in the compressor design for carry generation. When MUX is used instead of XOR for producing Sum output, the delay gets minimized as the select bit is given to MUX prior to inputs, switching of transistors is fast.

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The transistor model of 4-2 compressor is as shown in Fig. 2. This circuit of 4-2 Compressor has only 40 transistors, and it consumes lesser power consumption. The equations governing the Sum, Carry and Cout bits are,

$$Sum = (X1 \oplus X2) \bullet \overline{X3 \oplus X4} + \overline{(X1 \oplus X2)} \bullet (X3 \oplus X4) \bullet \overline{Cin} + \overline{(X1 \oplus X2) \bullet \overline{X3 \oplus X4} + \overline{(X1 \oplus X2)} \bullet (X3 \oplus X4) \bullet Cin}$$

$$Carry = (X1 \oplus X2 \oplus X3 \oplus X4) \bullet Cin + \overline{(X1 \oplus X2 \oplus X3 \oplus X4)} \bullet X4$$

$$Cout = (X1 \oplus X2) \bullet X3 + \overline{(X1 \oplus X2)} \bullet X1$$

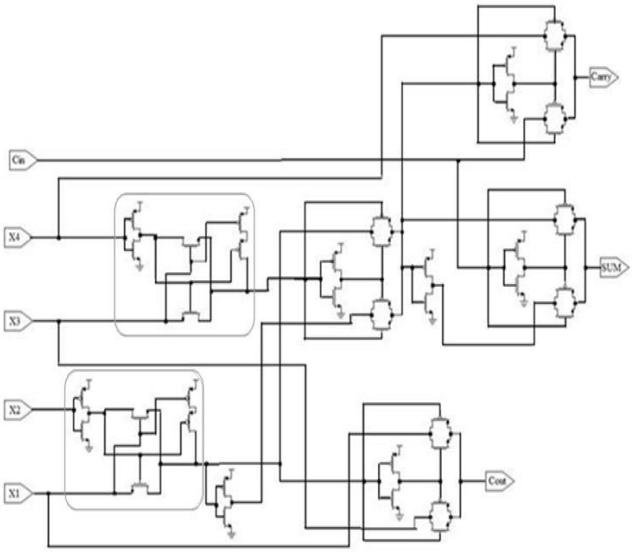

Fig. 2: Transistor model of 4-2 Compressor

III. PARITY CHECKERS

The Parity Checkers are used for even or odd parity checking on high speed transmission and retrieval systems. A parity bit can be append to any n-bit word for generating an even or odd number of logic 1's. A parity bit is considered as an extra bit that is to be included with the input binary word for making the total number of 1's in the binary word either an odd or even number. At the transmitter/sender side, a parity generator is used, which produces parity bit at the transmitter side and at receiver side, a parity checker is used for checking the parity of the received bits. A 3-bit parity generator with both even and odd outputs for 3-bit message (ABC) signal is shown in Table1.

Table 1
Even and Odd Parity bits of 3-bit input

A	B	C	Odd Parity	Even Parity
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

The Even parity signal is 1, if the message signal has odd number of logic 1's and 0 when there are even number of 1's. The odd Parity bit is 1, if the message signal has even number of 1's. The even and odd parity bits are complementary. The concept of parity generation and parity checking is shown for a 8-bit word for which extra bit is appended (as seen in braces).

1 1 1 0 0 1 0 1 [1] –> Even parity generation = Odd parity recognition

1 1 1 0 0 1 0 1 [0] –> Odd parity generation = Even parity recognition

1 0 0 1 0 1 0 1 [0] –> Even parity generation = Odd parity recognition

1 0 0 1 0 1 0 1 [1] –> Odd parity generation = Even parity recognition

The number in braces is included for parity generation and the bit is excluded in the parity checker/ recognizer. The parity checker produced the bit indicated in braces as above. Parity bits are generated using XOR modules. A 9-bit parity checker with XOR gates is as shown in Fig. 3, which shows a 9-bit message (A to I) and also the Even and Odd Parity bits are shown. The critical path delay of the circuit is 4 XOR delays.

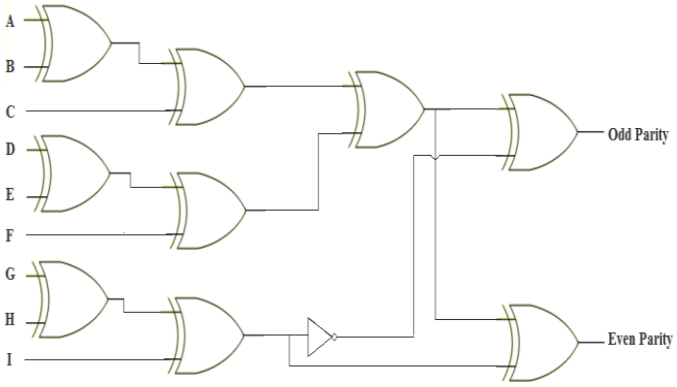

Fig.3: Typical 9-bit Even and Odd Parity Checker using XOR gates

The parity checker detects single bit errors that have occurred in the transmission lines of communication system and so parity checkers can be embedded for online monitoring of circuits and to build a Self-Checking Circuit (SCC) Design. Both the even and odd parity outputs are available for generating or checking even or odd parity up to 9 bits. The Even parity result is complementary to odd parity bit and vice versa. The maximum output delay of 9-bit parity checker in terms of XOR gates is 8 XOR Delays when inputs are applied serially. The equations governing the even and odd parity results for the above mentioned 9 – bit parity checker are as follows,

$$Even\ Parity = A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G \oplus H \oplus I$$

$$Odd\ Parity = A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus \overline{G \oplus H \oplus I}$$

The single bit error checking system for an 8-bit input message data along with an 8-bit parity generator at the transmitter side and a 9-bit Parity Checker to detect the output data as valid or faulty is shown in Fig. 4 [6]. A 9-bit Parity Checker acts as an 8-bit parity generator also, if one

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of the inputs is logic 0. Only single bit errors can be detected using the below figure, but they cannot be correctly located. So, multiple numbers of parity checker units are to be placed at intermediate places in-between input message and receiver, which requires some hardware cost. The present modern computers have memory systems with error correction capability.

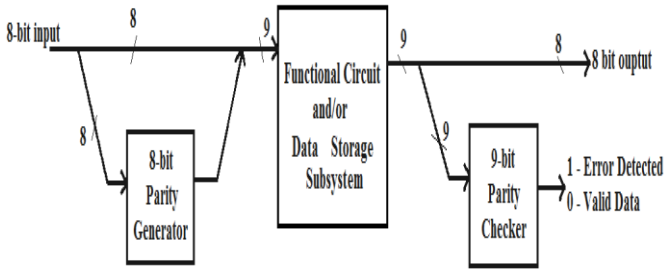

Fig. 4: Error checking system for an 8-bit input message data with 9-bit parity checker

IV. PARITY CHECKER USING 4-2 COMPRESSORS

The parity checker output can be obtained as quickly as possible in order to facilitate high speed communication as soon as the data is found to be fault free. Also when the data is found faulty, the correction mechanisms can be applied immediately. The compressors can be used for parity checking (also parity generation), as the sum bit acts as the XOR output of the input bits (Sum = XOR of 4-inputs and input Cin).

The use of 4-2 Compressor shown in Fig.2, will have lesser delay due to use of MUX at Sum bit. The Sum output of first 4-2 Compressor with A, B, C, D and E inputs will have one XOR and two MUX delays instead of 4 XOR delays when only XOR gates are used. So, a high speed even and odd parity checker is obtained using Sum output of 4-2 Compressors as shown in Fig. 5. The critical path delay of the proposed 9-bit parity checker with 4-2 Compressors is 1 XOR and 3 MUX delays. The presented 9-bit parity checker can be used as 8-bit parity generator for single error detection that might have occurred while transmitting an 8-bit message from the transmitter end.

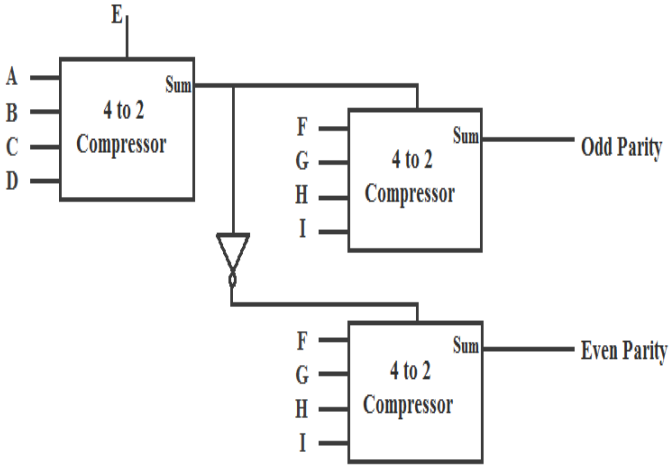

Fig.5: 9-bit Even and Odd Parity Checker using 4-2 Compressors

V. EVALUATION OF SIMULATION RESULTS

On using the presented form of 9-bit parity Checker using 4-2 Compressors, the maximum output delay and then the power delay product (PDP) will be reduced because 4-2 Compressor is having lesser output delay than general parity checker. The Table 2 shows the comparison of the present parity checker using 4-2 Compressors with typical parity checker using XOR gates. In both the parity checkers, XOR module of good driving capability is used as it has low power consumption along with minimum output delay. The Simulation results of the proposed 9-bit Parity Checker with 9-inputs (A to I) and the Even and Odd Parity outputs are shown in Fig. 6. The simulation results have been obtained at a supply voltage source of 3.3V.

Table 2
Delay and PDP Comparison of proposed Parity Checker using 4-2 Compressors against Typical Parity Checker.

9-bit Parity Checker	Delay (Sec)	PDP (J)
Using XOR gates	2.0×10^{-4}	4.78×10^{-9}
Using 4-2 Compressors	3.704×10^{-9}	3.046×10^{-13}

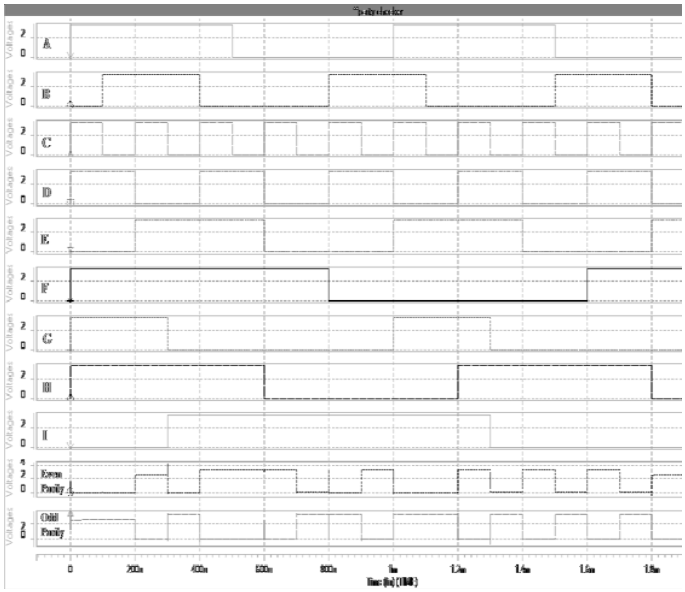

Fig. 6: Simulation results of the proposed parity checker using 4-2 Compressors

VI. CONCLUSION

An efficient 9-bit Parity Checker has been presented, with only 4-2 Compressors as its building blocks, to produce faster even and odd parity bits which further has lesser power delay product (PDP). The typical parity checker is designed with low area and low power consuming XOR modules and the 4-2 Compressors in the proposed Parity Checker is also designed with those XOR modules and transmission gates based multiplexer. The present Parity

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Checker has been showing optimal performance in terms of speed and PDP when compared to typical parity Checker when simulated using HSPICE tool at 0.18µm technology of CMOS. The Parity Generators can also be designed using 4-2 Compressors.

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