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DESIGN OF COMPACT REVERSIBLE LOW POWER n-BIT BINARY COMPARATOR USING REVERSIBLE GATES

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Abstract Reversible logic plays a very important role in recent times as reducing power consumption in digital logic design. Reversible logic contains a feature of recovering bit loss from unique input-output mapping where conventional logic has failed. Here, the reversible low power n-bit binary comparator has been designed. The two new reversible gates namely BJS and HLN gates are used to design an n-bit binary comparator. In addition, several theorems on the number of gates, garbage outputs, constant input, quantum cost, delay, power, area of n-bit binary comparator have been presented. The simulation results of the planned comparator show that the design works properly and offers higher performances than existing ones. Area and power analysis also show that the proposed design is the compact as well as a low power circuit.

1 Introduction

In 1960 landauer [1] shows that losing bit of information causes loss of energy. The loss of each bit of information causes loses of KT×ln2 joules of energy, where K is the Boltzmann constant and T is the temperature at which the system is operating. Reversible has an unique feature to generate one to one correspondence between input and output mapping [2,3] where it can generate output vector from input vector and vice versa. Reversible logic has been used in numerous applications in emerging nanotechnologies such as quantum dot cellular automata, optical computing, etc [4]. Reversible gates in circuits achieve no information loss and zero power dissipation [5]. Minimizing number of gates, quantum cost, garbage outputs and constant outputs are very important in reversible logic [6].

The comparison of two binary inputs numbers is a major application in microprocessor, encryption device, communication systems, sorting networks e.t.c [7]. The theorems and lemmas show the efficiency of reversible logic synthesis of n-bit comparator.

2 Literature overview

The basic idea and definitions of reversible gates, garbage output, quantum cost, area and power are discussed below.

2.1 Reversible gate

A reversible gate is an n-input n-output logic (denoted by n×n) that produces a output pattern form input pattern and also the inputs can be uniquely recovered from the outputs [8]. In other words, reversible gates are circuits in which the number of outputs is equal to the number of inputs and there is a one to-one correspondence between the vectors of inputs and outputs. The simple reversible NOT gate is 1×1 gate and Toffoli is a 3×3 gate.

2.2 Quantum cost

The quantum cost of a circuit is by substituting the reversible gates of a circuit with a elementary quantum gates. Every elementary quantum gate requires a single operation of unit cost. The state of a qu bit for two pure logic states can be expressed as $|c\rangle = \alpha|0\rangle + \beta|1\rangle$, where $|0\rangle$ and $|1\rangle$ denote 0 and 1, respectively, and α and β are the complex numbers such that $|\alpha|2 + |\beta|2 = 1$.

2.3 Garbage outputs

The outputs which are not used in the reversible gates are known as garbage outputs which are needed to maintain the reversibility. For each garbage outputs heavy price is paid off [9].

2.4 Area

The area of a logic circuit is the addition of separate area of each gate of the circuit. If a reversible circuit consist of n reversible gates and the area contains (a_1, a_2, ..., a_n). The area (A) of circuit is

$$A = \sum_{i=1}^{n} (a_i)$$

The area of a circuit can be calculated easily by obtaining area of each individual gate using CMOS 35nm Cadence Design Systems.

2.5 Power

The power of a logic circuit is the addition of separate power of each gate of the circuit. If a reversible circuit consist of n reversible gates and the power contains (p_1, p_2, ..., p_n). The area (P) of circuit is

$$P = \sum_{i=1}^{n} (p_i)$$

The power of a circuit can be calculated easily by obtaining power of each individual gate using CMOS 35nm Cadence Design Systems.

3 Existing Methods

The reversible design of [10] of binary comparator is a serial architecture which has an latency of O(n). The comparator consists of a chain of comparison cell which compares the *i* th of the first number x_i with the second number y_i. The 1-bit comparator cell is designed with reversible gates which is not generalised for n-bit. The reversible design of [11, 12] of binary comparator is also an serial architecture with an latency of O(n). The comparator consists of a chain of comparison cell which compares the corresponding bits of two numbers and this also not extended to n-bit.

In [13] the reversible binary comparator is a tree based. It contains the binary tree structure where each node consist of 2-bit reversible comparator that can compare 2-bit numbers x and y and gives two bit outputs. This is designed for 8 and 64 bit reversible comparator and not extended to n-bit. The [14] is the prefix grouping based reversible binary comparator and [15] is 1-bit comparator both of them are not extended to n-bit.

The sequential and a tree-based comparator have been proposed with several new gates which is also not extended to n-bit. The garbage outputs, quantum cost, delay, area, power are not compact in this design.

4 Proposed Method

Here, we proposed compact reversible n-bit binary comparator. The

comparator compares the magnitude of two binary numbers to determine whether

they are equal, greater or less than the other. Here, the two new reversible gates namely BJS and HLN gates are used to design a comparator.

4.1 BJS and HLN gates

The BJS gate is a 4×4 reversible gate which is shown in figure 1 and the HLN gate is 3×3 reversible gate which is shown in figure 2.

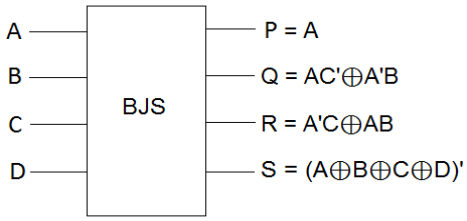

Figure1. BJS Gate

The BJS gate can implement all Boolean functions. When C=0 and D=1 then Q=A+B, R=AB and S=A⊕B.

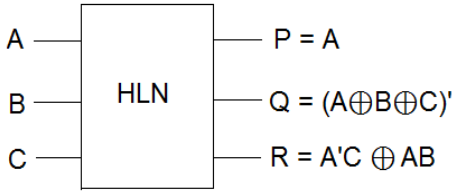

Figure 2. HLN gate

The HLN gate can implement all Boolean functions. When C=0 and C=1 then Q = A⊕B and Q=A+B. When B = 1 then R = A+B. When B = 0 and C = 0 then Q = A'.

4.2 Reversible MSB comparator

The MSB comparator circuit works with two binary inputs and sets two conatant inputs as 0. It gives three outputs based on their inputs. lb, gb and eb are the outputs from the MSB comparator. The MSB comparator circuit is derived from BJS gate. The MSB comparator circuit is shown below in figure 3. These MSB comparator output is fed into the next level, where (n-1)th bits have also compared.

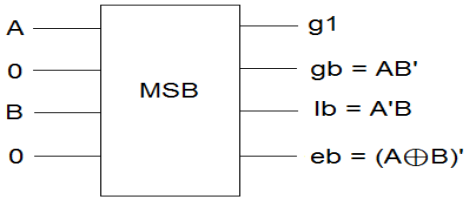

Figure 3. MSB Comparator

4.3 Reversible single-bit greater or equal comparator cell

The design of single bit comparator cell consists of HLN and two PG gates. It compares (n-1)th bit of A and B with previous MSB comparison result gb and eb. They produce the two outputs of P_{n-1} and Q_{n-1} which indicates the given number A and B are equal to each other or greater than the other. The g1 to g4 are garbage outputs.

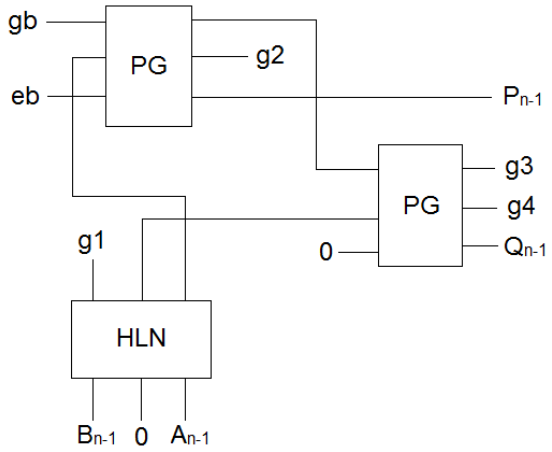

Figure 4. GE comparator

4.4Reversible single-bit less than comparator cell

A design of single bit comparator cell consists of two FG gates. The outputs of LT comparator cell shows that P represents the comparison are equal, Q represents the comparison are greater and R represents the comparison are lower.

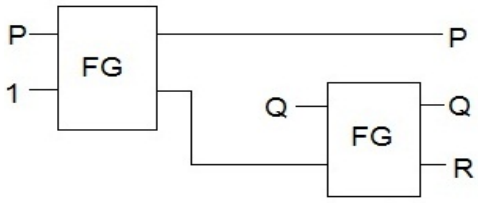

Figure 5. LT comparator

5 n-bit Reversible comparator design

The reversible 2-bit comparator consist of MSB comparator, GE comparator cell and LT comparator cell whic is shown in figure 6

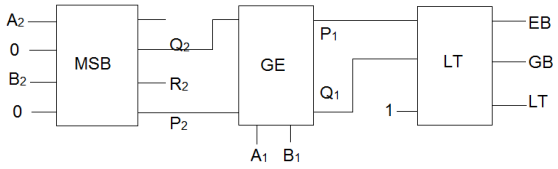

Figure 6. 2-bit comparator

The reversible n-bit comparator consist of MSB comparator, (n-1) GE comparator cell and LT comparator cell which is shown below

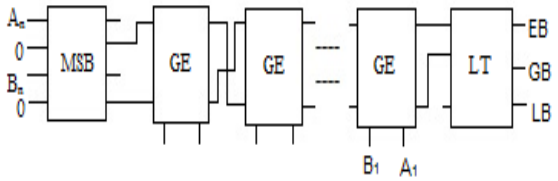

Figure 7. n-bit comparator

6 Simulation and discussion

The simulation of two bit binary comparator is shown below and the analysis of number of gates, garbage outputs, quantum cost, delay, area and power is discussed below.

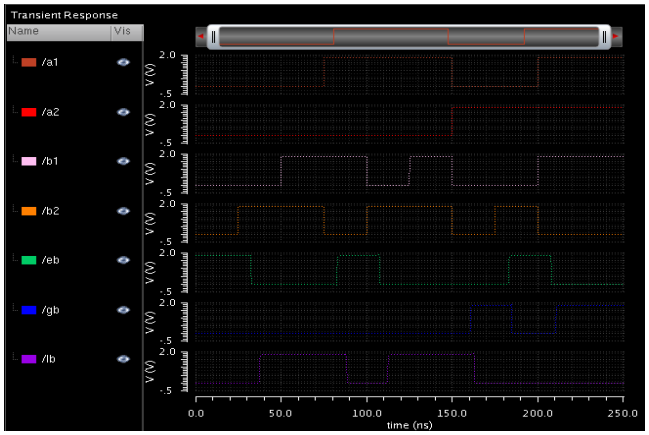

Figure 8. Simulation results

The below equations are used to calculate the n-bit reversible comparator where the number of gates, garbage outputs, quantum cost and constant inputs are

$NOG_{2\text{-bits}}$ = MSB + GE + LT
= 1 + (1+2) + 2
= 6
= 3 × 2 => 3n.

$GO_{2\text{-bits}}$ = MSB + GE + LT
= 1 + 4 + 0
= 5 => 4n-3

$QC_{2\text{-bits}}$ = MSB + GE +LT
= 6 + (5 + 4 × 2) + 2
= 21 => 13n -5

$CI_{2\text{-bits}}$ = MSB + GE +LT
= 2 + 0 + 1
= 3

Where n is the number of bits used to compare. By means of n the appropriate value can be developed by these equations. The comparison chart of these parameters are shown in the Table 1

Table 1. Comparison of Quantum cost, Garbage outputs and Number of gates.

No. of bits	Quantum cost					Garbage output					No. of gates			
	[14]	[11,12]	[13]	[15]	ours	[14]	[11,12]	[13]	[15]	Ours	[14]	[11,12]	[13]	ours
2	28	22	27	22	21	6	6	6	9	5	6	10	18	6
4	56	54	83	56	47	16	16	18	19	13	14	24	36	12
8	112	118	135	124	99	36	36	42	39	29	30	52	72	24
16	224	246	279	260	203	76	76	90	79	61	62	108	144	48
32	448	502	567	532	411	156	156	186	159	125	126	220	288	96
64	896	1014	1143	1076	827	316	316	378	319	253	256	444	576	192

Table 2. Comparison of Delay, Area and Power

No. of bits	Delay(ns)				`Area(μm^2)				Power(µw)			
	[14]	[11,12]	[13]	ours	[21]	[11,12]	[13]	Ours	[21]	[11,12]	[13]	ours
2	0.29	0.24	0.33	0.21	80	80	102.5	57.5	184.36	441.61	297.26	179.5
4	0.38	0.64	0.56	0.47	195	195	282.5	130.5	429.08	806.61	833.72	366.92
8	0.47	1.44	0.79	0.99	425	425	642.5	276.5	918.52	1536.79	1906.640	741.76
16	0.56	3.04	1.02	2.03	885	885	1362.5	568.5	1897.4	2997.03	4052.48	1491.44
32	0.65	6.24	1.25	4.11	1805	1805	2802.5	1152.5	3855.16	5917.51	8344.16	2990.8
64	0.74	12.64	1.48	8.27	3645	3645	5682.5	2320.5	7770.68	11758.41	16927.52	5989.52

Area = MSB + (n-1) GE +LT
= 16 + 36.5 (n-1) + 5
= 36.5n – 15.5

Delay = MSB + (n-1) GE +LT
= 0.05 + 0.13 (n-1) + 0.03
= 0.13n – 0.05

Power = MSB + (n-1) GE +LT
= 57.97 + 93.71 (n-1) + 27.82
= 93.71n – 7.92

7 Conclusion

This paper has presented the design of compact low power reversible n-bit binary comparator. The two new gates namely BJS and HLN gates are used to design a comparator. The proposed circuit has been constructed with 3n number of gates compared with 7n-4 [11, 12], 9n [13], 4n-2 [14], garbage outputs has 4n-3 compared with 5n-4 [11, 12], 6n-6 [13], 5n-4 [14], quantum cost has13n-5 compared with 16n-10 [11, 12], 18n-9 [13], 14n [14], power has 93.71n-7.92 compared with 182.53n+76.55 [11, 12], 268.23n-239.2 [13], 122.36n-60.36 [14], area has 36.5n-15.5 compared with 57.5n-35 [11, 12], 90n-77.5 [13], 57.5n-35 [14] and delay has 0.13n-0.05 compared with 0.2n-0.16 [11, 12], $0.23*\log_2(n)+0.1$ [13], $0.09*\log_2(n)+0.2$ [14]. Simulation of the circuit shows the design works properly. Since the comparison of two numbers are useful in numerous applications like microprocessor, sorting networks e.t.c.

References

[1]Landauer, R.: ‘Irreversibility and heat generation in the computational process’, IBM J. Res. Dev., 1961, 5, pp. 183–191.

[2] Perkowski, M., Al-Rabadi, A.N., Kerntopf, P., et al. 'A general decomposition for reversible logic'. Proc. RM'2001, Starkville, 2001,pp. 119–138

[3] Perkowski, M., Kerntopf, P.: 'Reversible logic'. Invited tutorial, Proc.EURO-MICRO, Warsaw, Poland, September 2001

[4] H. Thapliyal and N. Ranganathan, "Reversible logic-based concurrently testable latches for molecular qca," *IEEE Trans. Nanotechnol.*, vol. 9,no. 1, pp. 62–69, Jan. 2010.

[5] Bennet, C.H.: 'Logical reversibility of computation', IBM J. Res. Dev.,1973, 17, pp. 525–532.

[6] Kerntopf, P., Perkowski, M., Khan, M.H.A.: 'On universality of general reversible multiple valued logic gates'. IEEE Proc. of the 34th Int. Symp.on Multiple Valued Logic (ISMVL04), 2004, pp. 68–73

[7] D.Kim, K.Kim, J.Y. Kim, S.Lee, S.J.Lee, H.J.Yoo, "81.6 gops object recognition processor based on a memory-centric noc," *IEEE Trans. OnVLSI*, vol. 17, no. 3, pp. 370–382, 2009.

[8] Babu, H.M.H., Islam, M.R., Chowdhury, A.R., Chowdhury, S.M.A.:'Synthesis of full-adder circuit using reversible logic'. 17th Int. Conf.on VLSI Design, 2004, pp. 757–760.

[9] Biswas, A.K., Hasan, M.M., Chowdhury, A.R., Babu, H.M.H.:'Efficient approaches for designing reversible binary coded decimaladders', Microelectron. J., 2008, 39, (12), pp. 1693–1703.

[10] Al-Rabadi, A.N.: 'Closed – system quantum logic network implementation of the viterbi algorithm', Facta Universitatis – Elec.Energ., 2009, 22, (1), pp. 1–33.

[11] Rangaraju, H.G., Hegde, V., Raja, K.B., Muralidhara, K.N.: 'Design ofefficient reversible binary comparator'. Int. Conf. on Communication Technology and System Design, 2012, vol. 30, pp. 897–904

[12] Rangaraju, H.G., Hegde, V., Raja, K.B., Muralidhara, K.N.: 'Design oflow power reversible binary comparator'. Proc. Engineering (ScienceDirect), 2011.

[13] Thapliyal, H., Ranganathan, N., Ferreira, R.: 'Design of a comparator tree based on reversible logic'. Proc. Tenth IEEE Int. Conf. On Nanotechnology Joint Symp. with Nano, August 2010, pp. 1113–1116.

[14] Vudadha, C., Phaneendra, P.S., Sreehari, V., Ahmed, S.E.,Muthukrishnan, N.M., Srinivas, M.B.: 'Design of prefix-based optimal reversible comparator'. IEEE Computer Society Annual Symp. on VLSI, 2012, pp. 201–206.

[15] Morrison, M., Lewandowski, M., Ranganathan, N.: 'Design of a tree-based comparator and memory unit based on a novel reversible logic structure'. IEEE Computer Society Annual Symp. on VLSI, 2012, pp. 331–336.