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Leakage Power Reduction Using Gate Replacement and Multimode Power Switches

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***Abstract*— Power consumption is one of biggest challenges in VLSI design. In the past, power has mainly been a concern for chips used in battery-powered devices. During long periods of inactivity, multi-threshold CMOS is very effective for reducing leakage power. There are many techniques to reduce static power. However, they are very much sensitive to process variations which affect manufacturability. Reducing leakage power remains to be one of the key design goals in the mean time. So, a new multi-mode power switch architecture with gate replaced SPST adder as logic core is proposed. Here, those internal gates in their worst leakage states are being replaced by other library gates while maintaining the circuit's correct functionality during the active mode. It offers greater power reduction and delay degradation and also requires less design effort. It also assures low leakage power and high tolerance to process variations. To achieve further static power reduction benefits, it can be combined with the existing techniques. Hence it is clear that the total power consumption can be decreased to a great extend using intermediate power off modes**

***Index Terms*— Multi-threshold CMOS (MTCMOS), Threshold Voltage (V_t), Leakage Current (IL), Spurious Power Suppression Technique (SPST), Most Significant Part (MSP), Least Significant Part (LSP)**

I. INTRODUCTION

According to Moore's law, as the chip density increases, power consumption is becoming a major problem for the contemporary systems [2]. There are two types of power: static and dynamic. Dynamic power can be reduced by the reduction of supply voltage level, since it is proportional to the square of supply voltage. But the execution time is adversely affected by this reduction. So, transistor threshold voltage is reduced, to maintain system performance. When threshold voltage is decreased, sub-threshold leakage current increases exponentially. So, for technologies below 90 nm, static power is so high that it is comparable in magnitude to dynamic power consumption. A structure with intermediate power-off mode, which reduces the time required for recovering from idle mode at the expense of reduced leakage current suppression, is proposed. Similar structures were proposed by different authors. They extended this tradeoff between wake-up overhead and leakage power savings into multiple power-off modes. Hence the circuit is put into an intermediate power-off mode (i.e., low-power state), instead of consuming power by remaining in the active mode during the short periods of inactivity, which is determined by the length of the idle period and the wake-up time. The higher are the power savings achieved when the period of inactivity is longer.

As technology scales down, the supply voltage must be reduced such that dynamic power can be kept under control and power delivery remains feasible. But, in order to prevent the negative effect on performance incurred, the threshold voltage (V_t) must also be reduced such that sufficient gate overdrive is maintained. This reduction in V_t causes an increase in the leakage current (about 5 times per generation), which in turn may increase static power to unacceptable levels.

Here in this paper, we deal with the design of a new multi-mode power switch architecture with gate replaced SPST adder as the logic core.

The rest of the paper is organized as follows. Section II gives a brief background of the proposed work. Section III presents Multimode Architecture; Section IV describes the gate replacement technique; Section V provides the results and discussion obtained by designing the circuit. Finally we conclude the paper in Section VI.

II. BACKGROUND

There are many techniques evolved for reducing leakage power. MTCMOS technology is effective for reducing the same. It is a variation of CMOS chip technology which has transistors with multiple threshold voltage to reduce delay and power. An approach is to use dual V_t libraries [1]. It suppresses leakage current, but reduces the performance.

Use of high V_t power switches between the circuit and power supply or ground rail can be used to decrease power [3], [6], [5]. During idle mode, these switches are turned off, there by suppressing leakage current. Its drawback is the large current rush during core reactivation and wakeup time. This limitation of power switches can be overcome by using intermediate power of modes. Wakeup time is the time required for recovering from idle mode. So, the circuit is put into a low power state or appropriate power of mode, instead of consuming power by remaining in the active mode [4]. Higher power savings can be achieved when the period of inactivity is longer, by using most aggressive power-off modes. The previous architectures have several drawbacks. First, it cannot be easily extended to support more than two intermediate power-off modes and thus it cannot be used for high-performance circuits since the power reduction potential

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cannot be fully exploited. Next, a significant amount of power is consumed by the architecture and this reduces the advantages offered by the power switches. They are also very sensitive to process variations, which can affect its manufacturability and predictability adversely. Also, as it consists of analog components, it is not easily testable.

In this paper, we present an effective and robust multimode power-gating architecture that has none of the above drawbacks of the previous architectures. The proposed structure requires minimal design effort since it is very simple. It is considerably smaller and offers greater power savings for similar wake-up times.

III. MULTIMODE ARCHITECTURE

Standby power reduction is important in implementing low power systems. Static power becomes more prominent with device scaling.

Fig. 1 presents the multimode power switch architecture. It consists of three transistors M_P, M_0 and M_1. M_P is the main power switch transistor with high threshold voltage and remains on only during active mode. Transistors M_0 and M_1 are low threshold voltage transistors and corresponds to intermediate power of modes i.e., dream and sleep modes respectively. They are turned on only during the corresponding power of modes.

1. Active Mode: All transistors are on.

2. Snore Mode: All transistors are off. The leakage current of core is equal to total leakage current flowing though each transistor, which is very small..

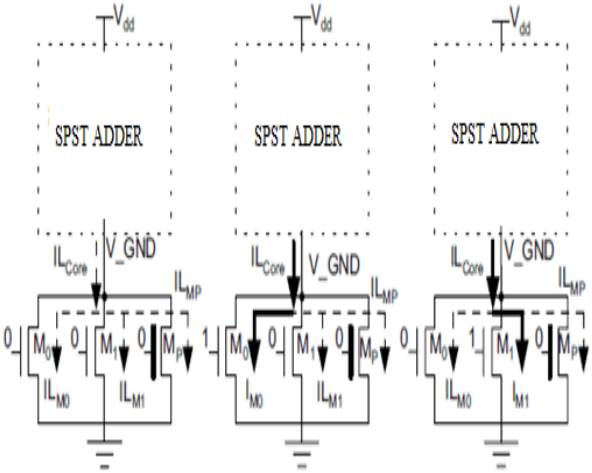

Fig.1 Multimode architecture: (a) snore mode (b) dream mode (c) sleep mode

3. Dream Mode: M_0 is on and others are off as in Fig 1(b).Since M_0 is on, the current flowing through it increases.($I_{MO} > I_{LMO}$) and hence the total current increases. The exact value of I_{MO} depends on M_0 transistor's size. The voltage level at $V_{\_GND}$ is now lower than V_{dd} ($V_{\_GND} < V_{dd}$).Compared to snore mode, static power is higher, but less wakeup time.

4. Sleep Mode: M_P, M_0 are off and M_1 is on, as in Fig 1(c).When M_1 is on, the total current again increases. Thus, voltage at V_{GND} node is further reduced compared to dream mode and thus wakeup time decreases.

The core part is implemented using SPST (Spurious Power Suppression Technique) adder which reduces power dissipation of combinational VLSI designs. It separates the design into two parts: most significant part(MSP) and least significant part(LSP). The main advantage of using SPST adder is that it turns off the MSP when it does not affect the computation results to save power.

Fig.2 shows an SPST adder. Between the eighth and ninth bits, the 16 bit adder is divided into MSP and LSP [2]. The input data of MSP remain unchanged when MSP is necessary. But it becomes zeros when MSP is negligible. This is to avoid glitching power consumption. The effective data range of arithmetic units is detected by the detection logic. The data controlling circuits of SPST latch a portion of data when it does not affect the computation results to avoid useless data transition occurring inside the arithmetic units. This data controlling unit brings evident power reduction.

The detection logic unit decides whether to turn off MSP or not. The two operands of MSP enter the detection logic unit and based on some Boolean equations, this unit determine whether the input data of MSP should be latched or not. SPST adder will avoid the unwanted addition and thus minimize power dissipation. Eliminating the spurious computations will not only save the power consumed inside the SPST adder but also reduce the glitching noises.

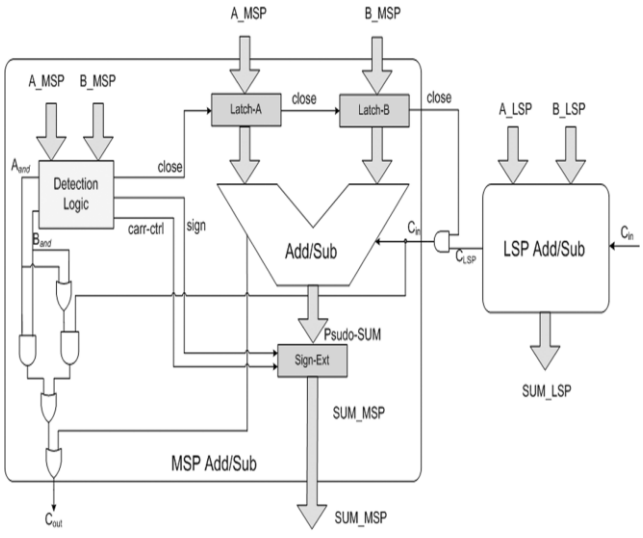

Fig.2 SPST Adder

1) When the detection-logic unit turns off the MSP: At this moment, the outputs of the MSP are directly compensated by the SE unit; therefore, the time saved from skipping the computations in the MSP circuits shall cancel out the delay caused by the detection-logic unit.

2) *When the detection-logic unit turns on the MSP:* The MSP circuits must wait for the notification of the detection-logic unit to turn on the data latches to let the data in. Hence, the

delay caused by the detection-logic unit will contribute to the delay of the whole combinational circuitry.

3) *When the detection-logic unit remains its decision:* No matter whether the last decision is turning on or turning off the MSP, the delay of the detection logic is negligible because the path of the combinational circuitry remains the same.

IV. GATE REPLACEMENT

The gate replacement technique is to replace a gate G(x) by another gate G (x, Sleep) where x is the input vector at G, such that:

1. G(x, 0) = G(x) when the circuit is active (Sleep = 0);
2. G(x, 1) has less leakage than G(x) when the circuit is in the standby mode (Sleep = 1).

Fig. 3 shows how to replace a NAND2 gate by a NAND3 gate. According to the leakage data, the leakage of NAND2 with the vector 11 is 454.50nA, and it is reduced to 94.87nA after the NAND2 gate is replaced by an NAND3 gate.

Fig.3. Gate replacement example for leakage reduction.

Using gate replacement technique, the logic gate at WLS is replaced by another gate containing an extra sleep signal. When the circuit is in active mode, i.e. SLEEP=0, this condition exhibits the correct functionality of the circuit. On the other hand, when the circuit is in standby mode, i.e. SLEEP=1, this condition reduces the leakage current of the replaced gate.

Direct Gate Replacement based on the optimal input vector is used here and we first arrange all the gates in the circuit into a topological order. The topological order guarantees that when we find a gate at its WLS, all its predecessors have already been considered. Then all the gates are evaluated one by one according to this order to further reduce the leakage power.

Fig. 4 shows the typical block diagram of the multimode architecture with the gate replaced SPST adder in the logic core. The structure operates in four different modes: active, sleep, dream and snore. The adder mainly works in the active mode. The power analysis of both with and without gate replacement is done and found that the power is very much reduced with replacement.

A novel approach of reduction in leakage current is proposed which is primarily based on the conventional gate replacement technique.

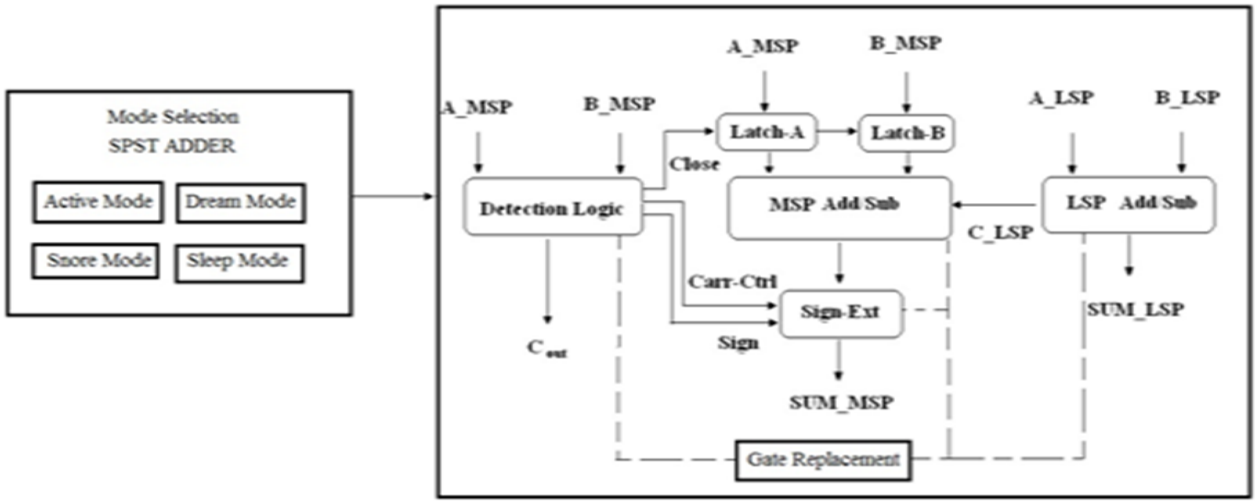

Fig.4. Block diagram including the gate replaced SPST adder in the core part

This paper focuses on the reduction of leakage current by applying gate replacement technique. Here, the gates of the SPST adder, having higher leakage current are being replaced with gates incorporating an extra sleep signal. Using this extra signal, it is observed that the functionality of the VLSI circuit is maintained in the active mode while the leakage is reduced both in the active and standby mode.

A logic gate can be considered at its worst leakage state when its input state yields higher leakage current.

V. RESULTS AND DISCUSSION

The multi-mode power switch architecture is synthesized in Spartan 2E starter board as the evaluation development board. The family is Spartan 2E, the device used is XC2S600E, the package is FG676 and the speed is -7. The top level source type is HDL, the synthesis tool is XST (VHDL/Verilog), and the simulator is ISE Simulator (VHDL/Verilog). The power analysis is done using XPower. The power analysis of active, sleep, dream and snore modes are obtained as follows:

The HTML Power Report of active mode without replacement is shown in Fig.5. The current is given in mA and the power in mW. The current from the inputs is 29mA and the power is 52mW. The Vccint is 1.8V and the total estimated power consumption is 121 mW.

The HTML Power Report of active mode with replacement is shown in Fig.6. The current from the inputs is 22mA and the power is 39mW. The Vccint is 1.8V and the total estimated power consumption is 90 mW.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		121
Vccint 1.80V:	63	114
Vcco33 3.30V:	2	7
Inputs:	29	52
Logic:	16	29
Outputs:		
Vcco33	0	0
Signals:	4	7
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Fig.5. HTML power report of active mode without replacement

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		90
Vccint 1.80V:	46	83
Vcco33 3.30V:	2	7
Inputs:	22	39
Logic:	8	14
Outputs:		
Vcco33	0	0
Signals:	2	3
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Fig.6. HTML power report of active mode with replacement

The HTML Power Report of sleep mode is shown in Fig.7. The current from the inputs is 22mA and the power is 39mW. The Vccint is 1.8V and the total estimated power consumption is 83 mW.

From the above two reports it can be viewed that the power consumption started decreasing gradually. The inputs, logic and the signals are also changing. The total current and the power for Vccint 1.80V have also been reduced and hence the total estimated power is also reduced. This also happens for the other two modes. The wake up time decreases to a great extend in the sleep mode. Sleep mode is the mode with largest energy saving capability and it operates with lowest functionality.

The HTML Power Report of dream mode is shown in Fig.8.The current from the inputs is 14mA and the power is 26mW. The Vccint is 1.8V and the total estimated power consumption is 60mW.

The HTML Power Report of snore mode is shown in Fig.9. The current from the inputs is 7mA and the power is 13mW. The Vccint is 1.8V and the total estimated power consumption is 50mW.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		83
Vccint 1.80V:	43	77
Vcco33 3.30V:	2	7
Inputs:	22	39
Logic:	4	7
Outputs:		
Vcco33	0	0
Signals:	2	4
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Fig.7. HTML power report of sleep mode

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		60
Vccint 1.80V:	30	54
Vcco33 3.30V:	2	7
Inputs:	14	26
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	1	1
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Fig.8. HTML power report of dream mode

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		50
Vccint 1.80V:	24	44
Vcco33 3.30V:	2	7
Inputs:	7	13
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	2	4
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Fig.9. HTML power report of snore mode

Snore mode is the last mode. Here, all transistors are off and the leakage current of core is equal to total leakage current flowing though each transistor, which is very small. The total current and the power for Vccint 1.80V have also been reduced to 24mA and 44mW respectively. The current at the inputs is 7mA and the power is 13mW which is again lower than the other three modes. Thus the total estimated power is reduced to 50mW which is again better than that of the previous three modes.

VI. CONCLUSION

In this work, a new power-gating scheme that provides multiple power-off modes is designed. The design offers the advantage of simplicity and required minimum design effort. It is very much tolerant to process variations and is scalable to more than two power off modes. The design requires significantly less area and consumes much less power than the previous design. The multi-mode power switch architecture is synthesized in Spartan 2E starter board. The power analysis is done using XPower. The power analysis of various modes i.e., active, sleep, dream and snore modes are obtained. From the power analysis it can be viewed that the power consumption of active mode without gate replacement of SPST adder is 121mW and when the gates that are at the worst leakage states are being replaced, the power consumption is reduced to 90Mw. Sleep mode consumes a power of 83mW. The total estimated power consumption of dream and snore modes are 60mW and 50mW respectively. Hence it is clear that the total power consumption can be decreased to a great extend using intermediate power off modes and also with the gate replacement technique.

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