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Power Optimization In Digital Circuits Using Modified Ultra Low Power NAND Gates

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***Abstract*— The design of CMOS VLSI circuits is becoming more complex as the leakage power consumption is posing a serious issue nowadays. Technological modification, reduction of threshold voltage and device geometry contributes to leakage power. The demand for electronic devices that are battery powered are increasing day by day. So the portable devices like notebooks, hearing aids ,personal communication devices need to be realized with low power consumption. In the proposed approach three digital circuits have been designed. A JK Master-Slave Flip-flop,4*1 MUX and a comparator is designed using 2 Input NAND Gate combining sleepy stack and sleepy keeper with RBB and Dual Threshold CMOS(DTCMOS)and static power consumption has been measured by switching off the sleep switches. The sleepy keeper approach has a combination of PMOS and NMOS transistor connected in parallel and will be inserted between pull up network and Vdd and pull down and GND. The sleepy keeper approach when combined with sleepy stack approach solves the area penalty with the stack approach. The keeper approach is the most efficient method for leakage reduction and maintains the logic of the circuit with lesser area. The digital circuits using the proposed NAND Gate achieves high leakage power reduction, lesser area and lesser delay when compared with the existing design.**

***Index Terms*— Reverse Body Bias(RBB),Dual Threshold Transistors, Sleepy Stack, Sleepy keeper, Multiplexer**

I. INTRODUCTION

Power dissipation in CMOS digital circuits are of three types. Static ,dynamic and short-circuit power. The dynamic power dissipation is caused due to switching activities. The dynamic power can be reduced by reducing the load capacitance as it forms the clocking network. The short-circuit power dissipation is caused due to the short-circuit between Vdd and ground. Designing the circuit to have equal input and output rise and fall time the short circuit power consumption can be reduced.. The Leakage(Static) power[1] is now forming a major threat as there is increase in the reduction of channel length, threshold voltage and gate oxide thickness. In near future power consumption due to leakage will domain over dynamic power consumption.

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This technique include controlling the substrate bias voltage applied. Stacking is a method used with sleep transistors to control leakage. In stacking first the transistors will be broken without effecting its W/L ratio and then sleep transistors will be added. With the use of Sleepy Keeper approach a combination of PMOS and NMOS will be inserted parallel between Pull Up network and Vdd and pull Down network and ground.

The Dual Threshold CMOS transistors will have input transistors for receiving input and output transistors for receiving outputs. The body contacts of one transistor which will be connected to body of another gate and thus the threshold is reduced. By reducing the threshold leakage can be controlled.

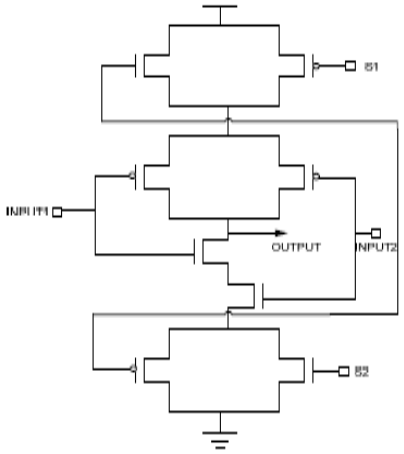

Fig 1.NAND Gate using Sleepy Keeper Approach

II.EXISTING WORK

Various techniques for leakage reduction[9] for multiplexers and JK Flip Flop includes modifying the clock pulses by applying either edge triggered or level triggered clock pulses[2]. The Gate Diffusion Input method has been used for the design of various digital circuits where power consumption and area is reduced by less complexity of the design.

The edge triggered flip flops change state at rising or falling edge of clock pulses depending upon control input. . There is double edge triggered flip- flops where the width of the pulses is made thrice that of an inverter at rising and falling edges. This is a method used to control leakage in various digital circuits.

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The design of Multiplexer and JK Flip-flop with NAND gate designed with Sleepy Stack technique combining with RBB and DTCMOS[7]. This design achieved leakage power reduction [3] with area and delay penalty. The main reason for this is stacking technique consumes much greater area and incurs greater delay.

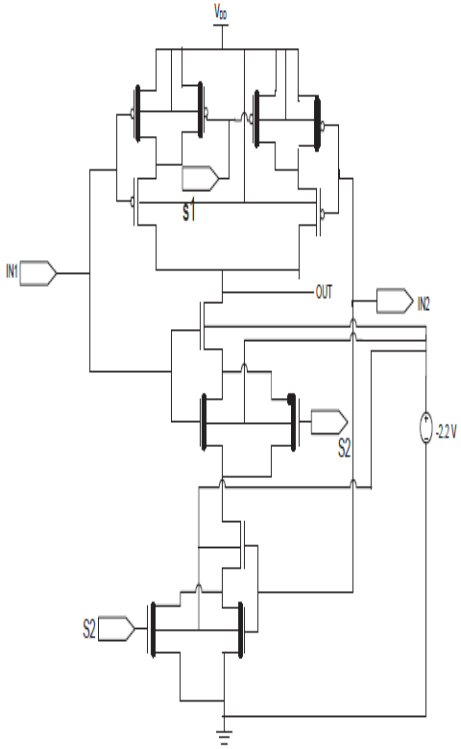

Fig 2.Existing NAND Gate using Sleepy stack with RBB and DTCMOS

III.PROPOSED WORK

The existing NAND Gate is modified by combining with Sleepy Keeper approach. The Sleepy Keeper technique has a combination of PMOS and NMOS transistors connected in parallel and placed between the pull up network and Vdd and pull down network and ground. The NMOS transistor of pull up sleep transistor is connected to PMOS pull down sleep transistor. As NMOS sleep transistor which rail off the path from Vdd to GND is connected to GND and PMOS transistor is connected to Vdd, NMOS transistor is not turn ON that's why it will not efficiently pass Vdd, this problem can be overcome by maintaining output value "1" in sleep mode by connecting NMOS to Vdd. PMOS transistor which is connected to the pull up NMOS transistor and GND which is parallel to NMOS sleep transistor, thus maintains output value equal to "0" in sleep mode.

The proposed NAND Gate combined with DTCMOS and Reverse Body Bias technique is used for ultra low power applications. With the NAND Gate designed various digital circuits like Multiplexer, JK Master-Slave Flip-Flop[10] and Comparator is designed and leakage, area and delay is analyzed.

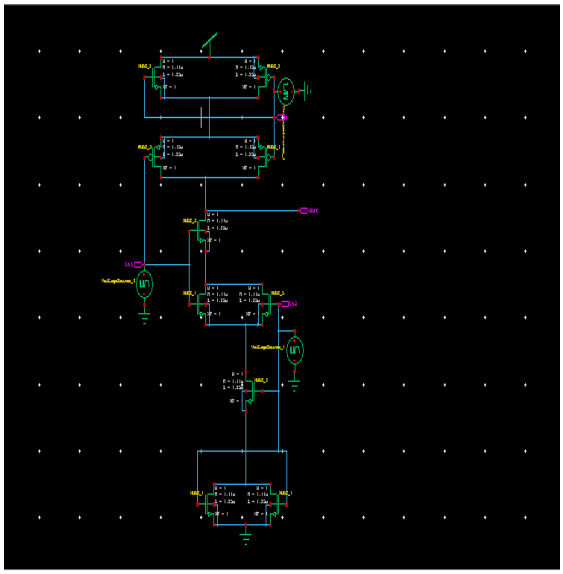

Fig 3.Schamatic Of Proposed NAND Gate using Sleepy Stack and Sleepy Keeper with RBB and DTCMOS

Multiplexer is mostly used to select from a set of signals. A Multiplexer (MUX) selects the analog or digital signals and then passes it to the output section to get a single output[4]. In a 2^n Multiplexer which inputs line has to be sent to output will be decided by the n selection lines. The amount of data that can be sent over an network can be increased.

I0, I1, I2, 13 are the inputs of the 4*1 Multiplexer. A and B act as selector inputs. Two inverters are also placed along with the selector inputs. There are two and three input NAND gates. These NAND Gates are designed using the proposed approach by combining Sleepy Stack with Sleepy Keeper with RBB and DTCMOS[5]. By using the proposed design the power consumption is reduced .

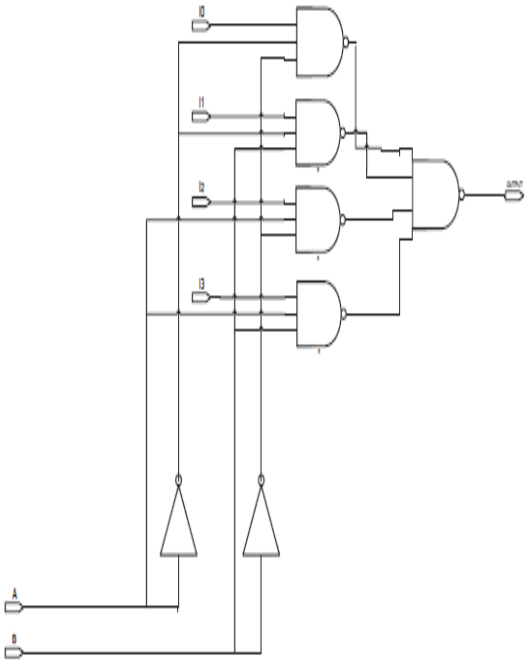

Fig 4.4*1 Multiplexer Based on Proposed NAND Gate

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A Master-Slave JK Flip-Flop is designed using the proposed NAND Gate combining Sleepy Stack with Sleepy Keeper approach.. The NAND Gate is designed by combining Sleepy Stack[6] and Sleepy Keeper with DTCMOS and RBB. The JK Master Slave flip flop comprises of a master and a slave that are two discrete clocked flip flops. When there is transition to disable level by the clock the flip flop responds. The inputs to the gates at the master is Clock C and the inputs to the gate at the Slave is clock complement. When Clock (C=1) then Clock Complement (C^{-}) and vice versa. Gates 3A and 3B are disabled when gates 1A and 1B are enabled and vice-versa.

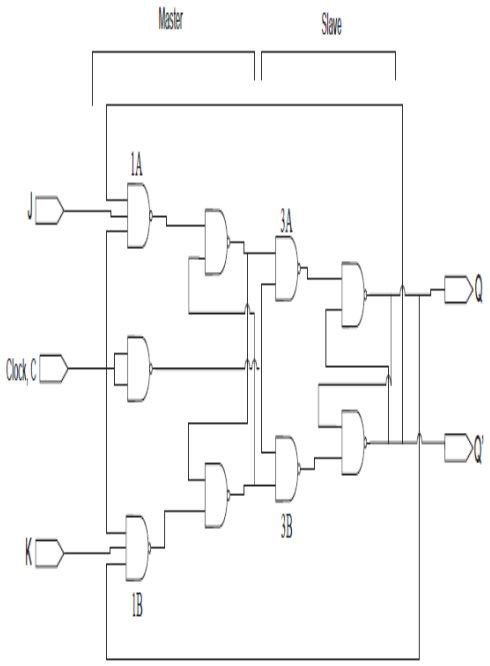

Fig 5. JK Master Slave flip flop using Proposed NAND gate

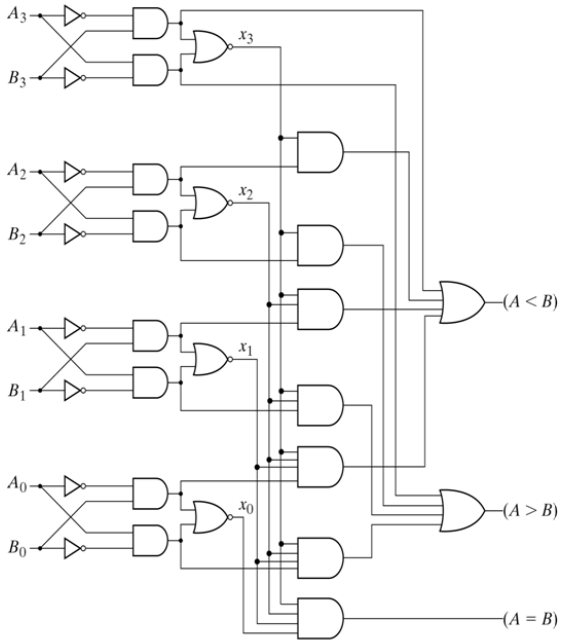

Fig 6. 4 Bit Magnitude Comparator Using NAND Gate

A 4 bit comparator is the designed using the proposed NAND Gate combining Sleepy Stack and Sleepy Keeper approach. A Comparator compares two voltages or currents and produces a digital signal as output that indicates which one is greater, which one is lesser or whether both are equal. They are commonly used in devices that monitor analog signals[8].

IV.SIMULATION RESULTS

Simulations has been done using Tanner S-Edit EDA tool. Tanner EDA's design entry and simulation system includes S-Edit for schematic capture, T-Spice for circuit simulation and W-Edit for waveform probing. Power consumption , delay and Device Count for JK master slave flip flop multiplexer and Comparator has been recorded. The tanner has dual threshold PMOS and NMOS and with reverse body biasing techniques. All simulations are done using 130nm technology.

The power Delay and Area for JK Master-Slave Flip-Flop, Multiplexer and 4 bit magnitude Comparator has been compared with the existing design and has been tabulated.

TABLE I
Power, Delay, Area Comparison for JK Master Slave FF

130nm	Power Consumption	No. Of Counts	Delay (ns)
JK Flip Flop Using Existing NAND Gate	6.99E-005W	122	3.192
JK Flip Flop Using proposed NAND Gate	5.89E-005W	73	2.18

TABLE II
Power, Delay, Area Comparison for 4*1 Multiplexer

130nm	Power Consumption	No. Of Counts	Delay (ns)
4*1 Mux Using Existing NAND Gate	7.87E-005W	163	3.91
4*1 Mux Using Proposed NAND Gate	6.60E-005W	100	3.53

TABLE III
Power, Delay, Area Comparison For 4 Bit Comparator

130nm	Power Consumption	No. Of Counts	Delay (ns)
4Bit Comparator Using Existing NAND Gate	3.96E-004W	858	4.42
4Bit Comparator Using Proposed NAND Gate	3.34E-004W	514	3.23

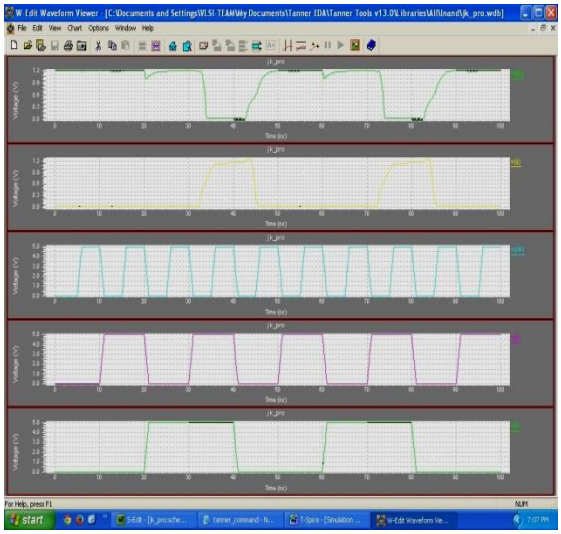

Fig7.Outputwaveform of JK Master Slave FF

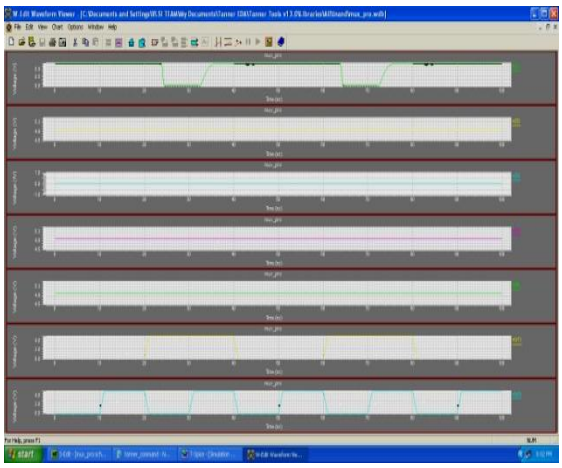

Fig8.Outputwaveform of 4*1 Multiplexer

Fig 9.Outputwaveform of 4 bit magnitude Comparator

V.CONCLUSION

A gate level power reduction technique for static and dynamic power consumption for digital CMOS circuits based on NAND gate like flip-flop and multiplexer is presented in this paper. When considering the gate current and sub threshold current there is a wide range of leakage for all input combinations of NAND. If the concentration is focused on increasing the speed of CMOS VLSI circuits then body biasing technique that use single power supply is enough.. The employment of RBB and high threshold transistors has resulted in achieving static power consumption. With the employment of Sleepy-Keeper technique the area is highly reduced. The trade-off is between area, delay and static power consumption.

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