

Impulsive Noise Removal in a Digital Image Using Reconfigurable Processor

Santosh Kumar.B¹, Divya.M.N²

¹PG Student, Reva Institute of Technology and Management (affiliated to VTU), Belagavi

²Assistant Professor, Department of ECE, Reva Institute of Technology and Management (affiliated to VTU), Belagavi

Abstract— In the field of digital image processing, two concepts are of great importance image enhancement and image noise filtering. Images are often corrupted by impulse noise in the process of signal acquisition and transmission. To avoid the damage to noise-free pixels, median filters are used for impulse detection and noise filtering. For the median filter, the concept of mean deviation parameter is added which estimate the noise in the images is proposed in this paper and is applied to gray scale image. Reconfigurable Processor based impulsive noise detection technique is implemented using 32-bit RISC processor core and XILINX ISE Design suite. The algorithm is written in system C Language and tested in DIGILENT FPGA board by interfacing with the PC.

Keywords: Impulsive noise, Median filter, Mean deviation, Reconfigurable Processor

I. INTRODUCTION

Digital image processing is a subfield of digital signal processing. Digital image processing has many advantages over analog image processing; it allows a much wider range of algorithms to be applied to the input data and can avoid problems such as the build-up of noise and signal distortion during processing [1]. Image filtering is a necessary step in image processing. In most of the cases captured photographic images from image sensors are affected by noise. The impulse noise is the most frequently referred type of noise. This noise, commonly also known as salt and pepper noise, is caused by malfunctioning pixels in camera sensors, faulty memory locations in hardware, or errors in the data transmission [2].

The median filter is an ideal filtering technique since it produces fine details, sharp corners and skinny lines but it destroys structural and neighborhood information [3]. To overcome such issues several modifications were applied to median filters that resulted in new filters for example increasing window size resulted in blurring of pictures [4]. Switched median filters [5], [6] were developed however these filters do not admit the native statistics. To overcome the flaw, totally filter [7] was developed. This filter identifies the element as pattern, if that element value is either zero or 255 it is retained otherwise is removed. This resulted in streaks in image. To avoid streaks, improved DBA [8] was developed with replacement of cut median which resulted in high noise densities i.e., the entire window within this may take all zero's or all 255's or combination of each zero and 255. Replacement of cut median did not fare well for the on high of case. So, totally asymmetrical cut median filter was developed [9]. If the chosen window contains salt or pepper noise as an element (i.e., 255/0 per value) and neighboring part values area is either zero or 255, then the median of the centre element will be either zero or

255. To overcome this draw back the some authors have taken the mean of the chosen window and replaced the centre element with the mean value but this result in certain math parameters for high salt and pepper noises. Also, some authors [10] proposed that, if the median of the chosen window is either zero or 255, the centre element is to be replaced by the absolute best neighbor element value. But, here there is no convincing reason for this proposition. So to address this drawback, I have used the statistics of the window elements, Rather than considering the mean an effort is made to cipher the deviation from the mean of the window and the central element is replaced by mean deviation.

FPGA has been chosen for this project because of its various properties. FPGAs are reconfigurable devices, which enables rapid prototyping, simplifies debugging and verification. Its parallel processing characteristic increases the speed of implementation [11]. Soft processor core is a microprocessor core that can be wholly implemented using logic synthesis. It can be implemented via FPGA. Custom peripheral blocks are interfaced with a soft processor (e.g. Xilinx's Microblaze) on FPGA fabric. Processor Local Bus (PLB) is used for this interfacing. In the proposed implementation, the input image stored in DDR2 memory is converted to HEX data format by the soft processor. The filtered image is converted back to its ASCII form again by the soft processor [12].

II. PROPOSED METHODOLOGY

The following are the steps of the proposed methodology.

- Select a 2-Dimensional window of size 3x 3. Assume that the pixel being processed is P_{ij} .
- If this pixel value lies between 0 and 255, $0 < P_{ij} < 255$, that is considered as a de-noised pixel. So, no processing is required and its value is left unchanged. For instance consider a matrix,
$$\begin{pmatrix} 25 & 28 & 24 \\ 18 & 02 & 10 \\ 08 & 30 & 50 \end{pmatrix}$$
 here centre pixel P_{ij} is 02, so left unchanged.
- If $P_{ij} = 0$ or 255, it indicates that the pixel is corrupted by salt and pepper noise. Here two cases are considered
 - The selected window contains few 0's or 255's elements and other elements lie between 0 and 255. Then the 0 and 255 elements are discarded and the median of the remaining elements is found. The P_{ij} pixel is replaced with this median value. For instance consider a matrix,

$\begin{pmatrix} 255 & 28 & 24 \\ 18 & 00 & 10 \\ 00 & 30 & 255 \end{pmatrix}$ here centre pixel P_{ij} is 0, so it is replaced with median value 24.

- Suppose the selected window contains all the elements 0 or 255 then the pixel P_{ij} is replaced by mean deviation value.

For instance consider a matrix,
 $\begin{pmatrix} 00 & 255 & 00 \\ 255 & 00 & 255 \\ 00 & 255 & 00 \end{pmatrix}$ here centre pixel P_{ij} is 0, so it is replaced with mean deviation value 101.

- Apply the above steps for all the pixels in the image to get de-noised image.

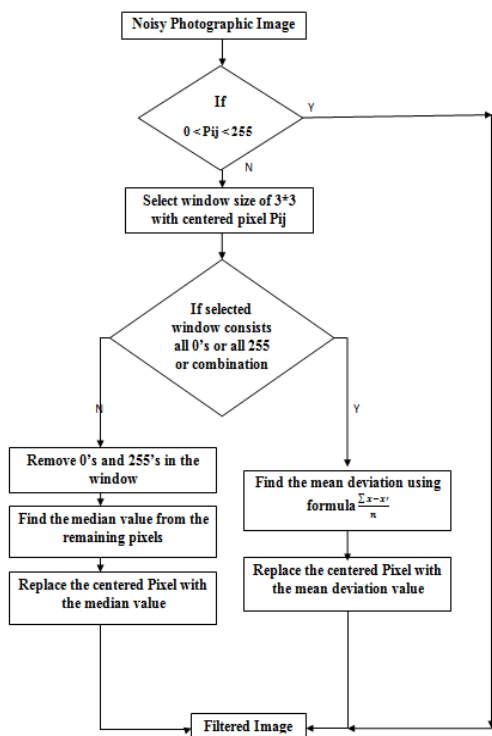


Figure1: Proposed methodology flowchart

III. PROPOSED IMPLEMENTATION

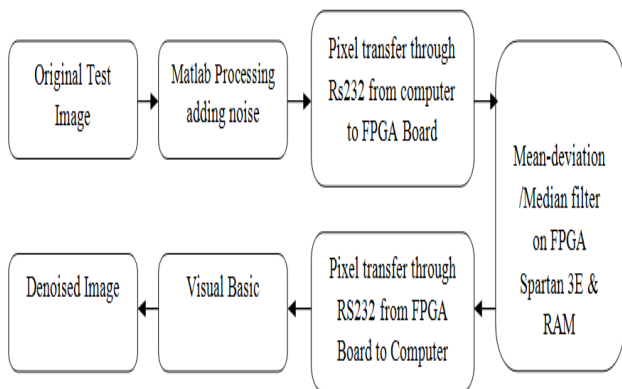


Figure2: Block diagram of the proposed system

The above is the block diagram for the proposed system where the test image input are converted to gray scale image with added noise using MATLAB. These images are represented by 8 bits/pixel and size is 128 x 128. Pixels are transferred through Rs232 cable from computer to FPGA Board. The Xilinx Platform Studio (XPS) is the development environment or GUI used for designing the hardware portion of this embedded processor system. Xilinx Embedded Development Kit (EDK) is an integrated software tool which has been used to develop an embedded system right from the hardware creation to final implementation of the system on an FPGA. Xilinx Platform Studio Software Development Kit (SDK) is an integrated development environment, that is used for C/C++ embedded software application creation and verification. The software application is written in C, debugged & downloads the bit file into FPGA. Then FPGA behaves like processor implemented on it.

IV. RESULTS

The proposed algorithm is implemented in the RISC processor on a FPGA Kit. It is implemented on 128x128 8-bit gray scale test image of a flower. The results are shown in following figures.

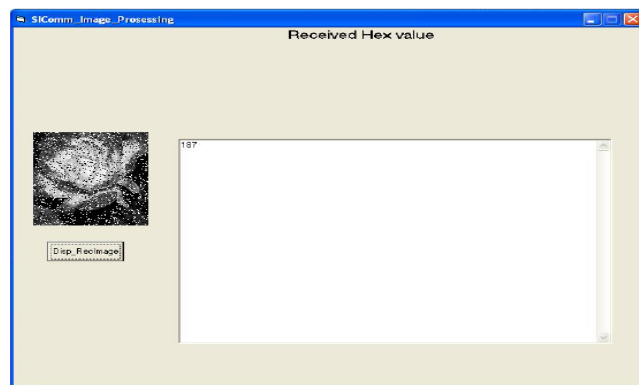


Figure 3: (a) Noisy Image Send to FPGA Kit

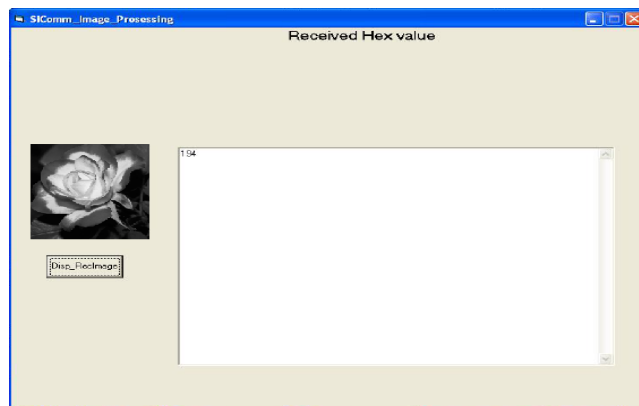


Figure 3: (b) Received Restored image from FPGA Kit

V. CONCLUSION

The proposed algorithm is tested using the MATLAB and FPGA hardware. From the observation of

figure 3(a) and 3(b), one can come to the conclusion that the present method is showing reasonably good performance at high noise density levels. Also it is clear that the fine details of the image and the contrast levels are much better in the case of the proposed algorithm. This confirms the validity of the proposed algorithm for de-noising the high density salt and pepper noise from the images. The VLSI architecture of our design requires only low computational complexity and two line memory buffers hence making it suitable for real-time applications. The architectures work with monochromatic images, but they can be extended for working with RGB color images and videos.

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BIOGRAPHY

Mr. Santosh Kumar.B., presently pursuing M-Tech (VLSI System Design and Embedded System) in Reva Institute of Technology and Management, Bangalore, Karnataka, India. He has received his B.E degree from VTU Belgaum. He is working as Assistant Professor in the Department of Electronics and Communication Engineering, East Point College of Engineering and Technology, Bangalore, Karnataka, India. His areas of interests are VLSI, Digital Image Processing, Microprocessor, Microcontroller and Communication Systems.

Mrs. Divya.M.N., presently pursuing PhD (VTU Belgaum). She is working as Associate Professor in the Department of Electronics & Communication Engineering, Reva Institute of Technology and Management, Bangalore, Karnataka, India. Her areas of interests are VLSI, Digital Image Processing, Control System and Communication Systems.