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Improvement of the Performance of DPLL Based FM Demodulator by using of Variable Gain Control in the Positive Region of the Input Signal

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***Abstract*— A dynamic structure modification algorithm of the conventional digital phase locked loop (CDPLL) design parameters has been proposed to get a variable gain DPLL (VGDPLL_UP) which has nearly symmetric two-sided acquisition range. The proposed variable gain control circuit has been allowed to function only at the positive region of the input signal (i.e. UP-side of the input signal). With the help of extensive simulation results, it has been established that in comparison to a CDPLL, the VGDPLL_UP has better FM demodulation capability.**

***Index Terms*— FM demodulator; Variable Gain DPLL (VGDPLL_UP); Acquisition Range; Tracking Response.**

I. INTRODUCTION

In coherent communication system DPLLs are used mostly [1,2,3,4,5,6]. DPLLs are often used as FM demodulator [7,8]. The present paper reports the effect of variable loop gain of conventional DPLL (CDPLL) in the performance of DPLL based FM demodulator and measures the improvements of the loop performance. In the case of fixed loop gain the demodulated output is not symmetric about the loop nominal frequency [8]. A way to remove this asymmetry is to vary the loop gain in accordance with the loop phase error only above the loop nominal frequency. The effect of variable loop gain may be utilized to improve the performance of CDPLL based FM demodulator. Here we have proposed a variable gain DPLL (VGDPLL_UP) in which loop gain is varied in accordance with the change of input frequency or loop phase error above loop nominal frequency. The present paper contains the performance of CDPLL as a FM demodulator with fixed loop gain and its system dynamics and its modification to improve the performance. The system equations of CDPLL and VGDPLL_UP, analytical results, simulation results and conclusion are stated in the section II, III, IV and V respectively.

II. CONVENTIONAL DPLL

The functional block diagram of DPLL has been shown in Fig.1. Considering the input signal as $A\sin\omega_i t_k$ the system equation for DPLL can be written as [9]

$$\varphi(t_{k+1}) = \varphi(t_k) + 2\pi(z-1) - K_0 z \sin\varphi(t_k) \quad \ldots(1)$$

where, $\varphi(t_{k+1})$ and $\varphi(t_k)$ are loop phase error at $(k+1)^{th}$ and k^{th} instances respectively, z is the ratio of input frequency and DCO nominal frequency (ω_0) and K_0 is the overall loop gain.

The system would achieve the steady state if the following conditions are satisfied [10].

$0 < K_0 < 2$ …….. (2a) for phase step input (z=1)

$0 < (K_0 z)^2 - \Lambda_0{}^2 < 4$ ………… (2b) for frequency step input $(z \neq 1)$, where $\Lambda_0 = 2\pi(z-1)$

Here we consider a tone modulated FM signal as input with carrier frequency ω (= ω_0, DCO nominal frequency), modulation index m_f and modulating signal frequency $\omega_m (\omega_m << \omega_0)$, $A\sin(\omega_0 t - m_f \cos\omega_m t)$ as the input of the FM demodulator. So in this case the value of z will be a slowly varying function of time, given as, $(1 + \frac{\omega_m}{\omega_0} m_f \sin\omega_m t)$. So for DPLL with FM input signal equation (1) may be written as

$$\varphi(t_{k+1}) = \varphi(t_k) + 2\pi k_f \sin\omega_m t_k - K_0(1 + k_f \sin\omega_m t_k)\sin\varphi(t_k) \quad \ldots(3)$$

Here t_k is the time of the k^{th} instant of the input signal, $k_f = \frac{\omega_m}{\omega_0} m_f$. When the loop will follow the input signal, the sampler output can be obtained as proportional to,

$$\sin\varphi(t_k) = \frac{2\pi k_f \sin\omega_m t_k}{K_0(1 + k_f \sin\omega_m t_k)} \quad \ldots\ldots\ldots\ldots\ldots(4)$$

Now if we consider the maximum frequency deviation of the FM signal of intune carrier $(\omega = \omega_0)$ lies within the tracking-range of a DPLL, then the DPLL will track the FM input signal and the sampler output drawn can be treated as demodulated output.

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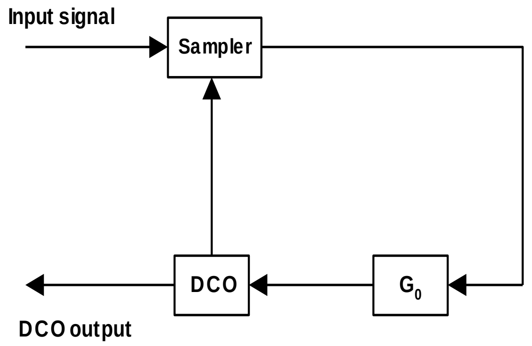

Fig. 1. Functional block diagram of CDPLL

III. VARIABLE GAIN DPLL (VGDPLL_UP)

A. *Formation of system equation*

The functional block diagram of VGDPLL_UP has been shown in Fig.2. To derive the system equation let us consider the incoming signal to the loop as $A\sin\omega_i t$. The DCO pulses sample this incoming signal. Let us consider the loop gain of at $(k+1)^{th}$ instant is $G_x(t_{k+1})$ and the same for DPLL is G_0 . So we can write $G_x(t_{k+1})$ as follows

$$G_x(t_{k+1}) = G_0(1+K_1\sin\varphi(t_k)) \quad \text{............... (5a)}$$

Again overall loop gain K_0 is related to loop gain G_0 as $K_0 = A\omega_0 G_0$. So the instantaneous overall loop gain can be written as

$$K_x(t_{k+1}) = K_0(1+K_1\sin\varphi(t_k)) \quad \text{............. (5b)}$$

So in that case we can write the equation (3) replacing K_0 by K_x as

$$\varphi(t_{k+1}) = \varphi(t_k) + 2\pi(z-1) - K_0 z(1+K_1\sin\varphi(t_k))\sin\varphi(t_k) \quad \text{................ (6)}$$

So for VGDPLL_UP with FM input signal equation (6) may be written as

$$\varphi(t_{k+1}) = \varphi(t_k) + 2\pi k_f \sin\omega_m t_k - K_0(1+k_f\sin\omega_m t_k)(1+K_1\sin\varphi(t_k))\sin\varphi(t_k) \quad \text{............... (7)}$$

Here t_k is the time of the k^{th} instant of the input signal and $k_f = \frac{\omega_m}{\omega_0} m_f$. The steady state sampler output will be

$$\sin\varphi(t_k) = \frac{2\pi}{K_0} m(t_k)\left(1 - \frac{4\pi K_1}{K_0} m(t_k)\right) \quad \text{......... (8a)}$$

for $\sin\varphi(t_k) > 0$, here, $m(t_k) = \frac{k_f \sin\omega_m t_k}{1+k_f\sin\omega_m t_k}$ and

$$\sin\varphi(t_k) = \frac{2\pi k_f \sin\omega_m t_k}{K_0(1+k_f\sin\omega_m t_k)} \quad \text{.............. (8b)}$$

for $\sin\varphi(t_k) < 0$.

B. *Acquisition performance of CDPLL and VGDPLL_UP with noise free input signal*

The acquisition properties of the VGDPLL_UP can be studied using the graphical analysis technique [11]. Using equation (7) for steady state solution one can derive the normalized input frequency $\left(\frac{\omega_{in}(t_k)}{\omega_0}\right)$ as given below,

$$\frac{\omega_{in}(t_k)}{\omega_0} = \frac{2\pi}{2\pi - K_0\sin(\varphi(t_k))(1+K_1\sin(\varphi(t_k)))} \quad \text{........(9)}$$

for $\sin\varphi(t_k) > 0$ and

$$\frac{\omega_{in}(t_k)}{\omega_0} = \frac{2\pi}{2\pi - K_0\sin(\varphi(t_k))} \quad \text{............... (10)}$$

for $\sin\varphi(t_k) < 0$

Fig.(3) shows the variation of normalized input frequency with respect to over all loop gain (K_0) and it has been shown in this figure that with $K_0 = 1.8$ and $K_1 = -0.365$, the acquisition range (AR) for CDPLL and VGDPLL_UP can be given in terms of the normalized input signal frequency

$$0.777 \le \frac{\omega_{in}}{\omega_0} \le 1.402 \quad \text{... (11)} \quad \text{for CDPLL and}$$

$$0.777 \le \frac{\omega_{in}}{\omega_0} \le 1.223 \quad \text{...(12)} \quad \text{for VGDPLL\_UP}$$

The significance of this observation is that the AR is symmetrical about the DCO nominal frequency for VGDPLL_UP and which is very much asymmetric for CDPLL.

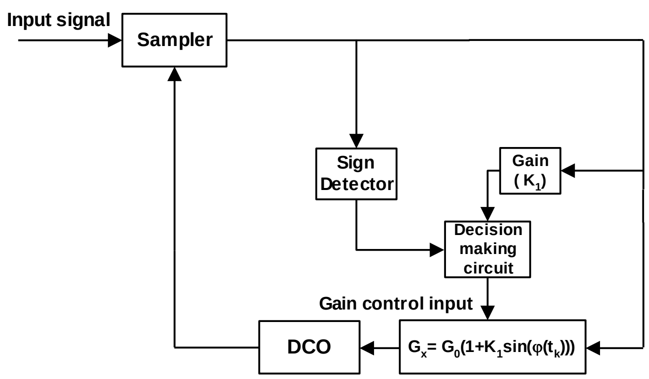

Fig. 2. Functional block diagram of VGDPLL_UP

C. *Analytical calculation of stability zone of VGDPLL_UP*

The stability criterion of CDPLL with finite width of DCO pulses can be obtained using the following iteration. Let us consider

$$X(t_{k+1}) = G(X(t_k))$$

$X(t_k)$ is a state vector defined as $X(t_k) = (\alpha(t_k), \beta(t_k))$, where $\alpha(t_k)$ and $\beta(t_k)$ are defined as $\alpha(t_k) = \varphi(t_{k+1})$ and $\beta(t_k) = \varphi(t_{k+2})$ If X^* is a value of X such that $X^* = G(X^*)$. Then X^* is called fixed point. Now Eqn.(6) can be written as

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$$\begin{pmatrix}\alpha(t_{k+1})\\ \beta(t_{k+1})\end{pmatrix}=\begin{pmatrix}\beta(t_k)\\ \beta(t_k)+2\pi k_f\sin\omega_m t_k-K_0(1+K_1\sin\varphi(t_k))(1+k_f\sin\omega_m t_k)\sin\beta(t_k)\end{pmatrix}$$

……….. (13)

So, we can write

$$G(X(t_k))=\begin{pmatrix}\beta(t_k)\\ \beta(t_k)+2\pi k_f\sin\omega_m t_k-K_0(1+K_1\sin\beta(t_k))(1+k_f\sin\omega_m t_k)\sin\beta(t_k)\end{pmatrix}$$

………… (14)

The Jacobian of the matrix is given by

$$G'(X(t_k))=\begin{pmatrix}0 & 1\\ 0 & 1-K_0(1+K_1\sin\beta(t_k))(1+k_f\sin\omega_m t_k)\cos\beta(t_k)-K_0K_1\cos\beta(t_k)(1+k_f\sin\omega_m t_k)\sin\beta(t_k)\end{pmatrix}$$

or,

$$G'(X(t_k))=\begin{pmatrix}0 & 1\\ 0 & 1-K_0(1+k_f\sin\omega_m t_k)\cos\beta(t_k)-2K_0K_1(1+k_f\sin\omega_m t_k)\sin\beta(t_k)\cos\beta(t_k)\end{pmatrix}$$

……. (15)

Now according to the Ostrowski's theorem [12], the condition of convergence i.e. the system would reach a steady state if

$\rho[G'(X^*)]<1$ ………………… (16)

where ρ is the spectral radius of an n × n matrix and defined as

$\rho(A)=\max|\lambda_i|$

Here λ_i = eigen value of A and $G'(X)$ is the $n\times n$ matrix of partial derivatives. Therefore

$$G'(X^*)=\frac{\partial}{\partial x}G(X)\Big|_{X=X^*}\qquad \text{………………. (17)}$$

Fastest convergence would occur if $G'(X^*)=0$.

Now for FM input (i.e. frequency step input), $G'(X^*)$ is given by

$$G'(X^*)=\begin{pmatrix}0 & 1\\ 0 & 1-K_0(1+k_f\sin\omega_m t_k)\sqrt{1-\left(\frac{2\pi}{K_0}m(t_k)\left(1-\frac{4\pi K_1}{K_0}m(t_k)\right)\right)^2}\left(1+2K_1\frac{2\pi}{K_0}m(t_k)\left(1-\frac{4\pi K_1}{K_0}m(t_k)\right)\right)\end{pmatrix}$$

… (18)

Determining the eigen values of the matrix (14) and applying the convergence condition (16), one gets the condition of convergence

$$0<\left(\left(K_0(1+k_f\sin\omega_m t_k)\right)^2\left(1-\left(\frac{2\pi}{K_0}m(t_k)\left(1-\frac{4\pi K_1}{K_0}m(t_k)\right)\right)^2\right)\right)\left(1+2K_1\frac{2\pi}{K_0}m(t_k)\left(1-\frac{4\pi K_1}{K_0}m(t_k)\right)\right)^2<4$$

….. (19)

The condition of convergence for CDPLL can be written from equation (19) by putting $K_1=0$. So the condition of convergence for CDPLL will be

$0<\left(K_0(1+k_f\sin\omega_m t_k)\right)^2-(2\pi k_f\sin\omega_m t_k)^2<4$ …… (20)

It can be shown that the stability zone using equation (19) and (20) for VGDPLL_UP and CDPLL respectively remain almost equal, i.e. VGDPLL_UP has no demerits in view of stability zone.

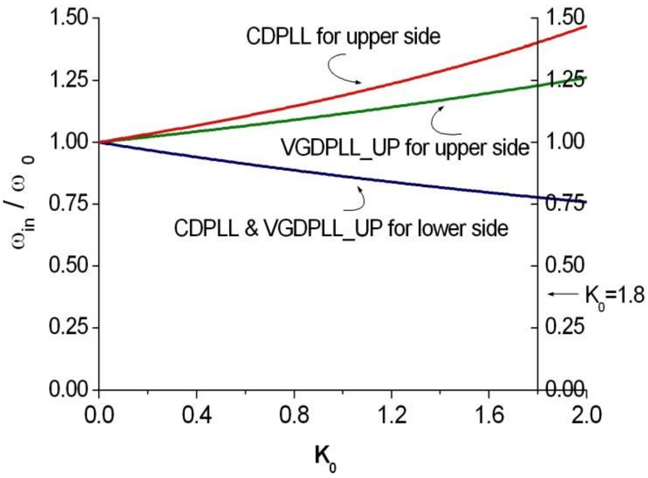

Fig. 3. Variation of normalized input frequency with respect to over all loop gain (K_0), with $K_1=-0.365$

IV. Numerical Simulation Results

The behaviors of the DPLL and MDPLL have been studied using the system equations (3) and (6) respectively. Fig.(4a) and Fig.(4b) show the analytical result of FM demodulated signal using CDPLL and VGDPLL_UP with $K_1=-0.35$ and $K_1=-0.4$ respectively and the same result using simulation shown in Fig.(5a) and Fig.(5b) respectively. It is observed from both analytical and simulation result that the output of VGDPLL_UP quite similar to the modulating signals, whereas that of the CDPLL much more differs from modulating signal. It can be easily shown that the amplitudes of the higher harmonics are proportional to the difference in maximum amplitudes in the positive and negative region. Therefore the output of the CDPLL will contain higher harmonic terms and which are very small in the VGDPLL_UP. So using VGDPLL_UP asymmetry of CDPLL can be removed and it gives much more better result when it is used as a FM demodulator.

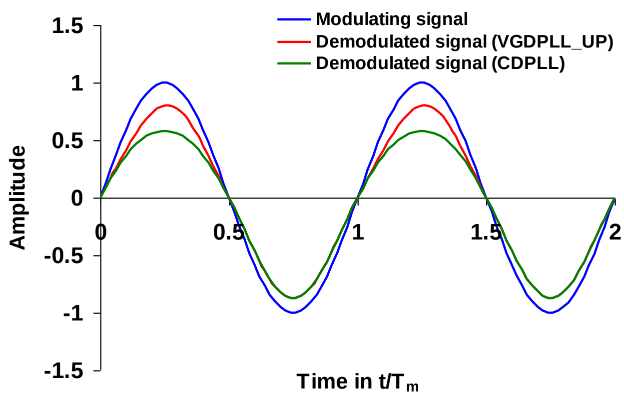

Fig. 4a. Plotting of FM demodulated signal using CDPLL and VGDPLL_UP. (With $K_0=1.8$, $\omega_0/\omega_m=50$, $K_1=-0.35$ and $m_f=10$) (Analytical Result)

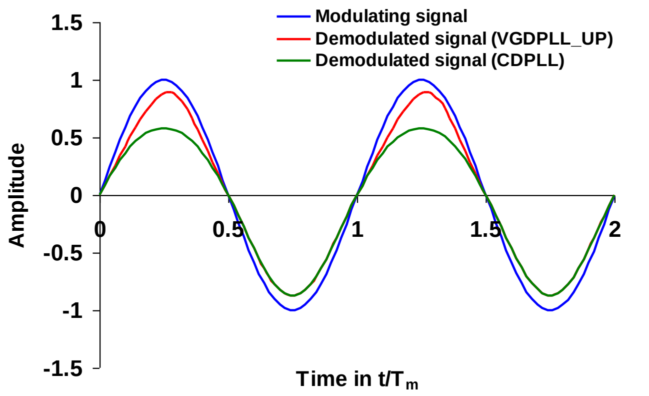

Fig. 4b. Plotting of FM demodulated signal using CDPLL and VGDPLL_UP. (With $K_0 = 1.8$, $\omega_0/\omega_m = 50$, $K_1 = -0.4$ and $m_f = 10$) (Analytical Result)

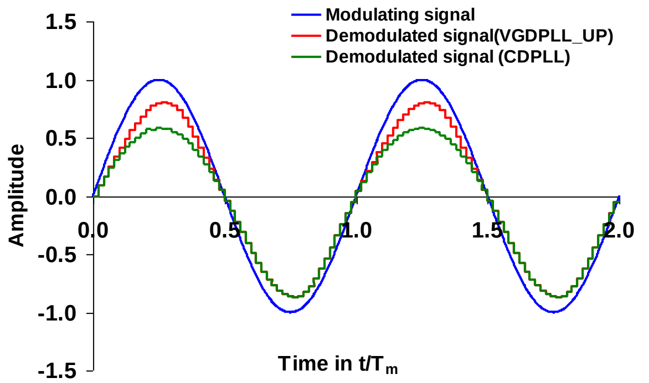

Fig. 5a. Plotting of FM demodulated signal using CDPLL and VGDPLL_UP. (With $K_0 = 1.8$, $\omega_0/\omega_m = 50$, $K_1 = -0.35$ and $m_f = 10$) (Simulation Result)

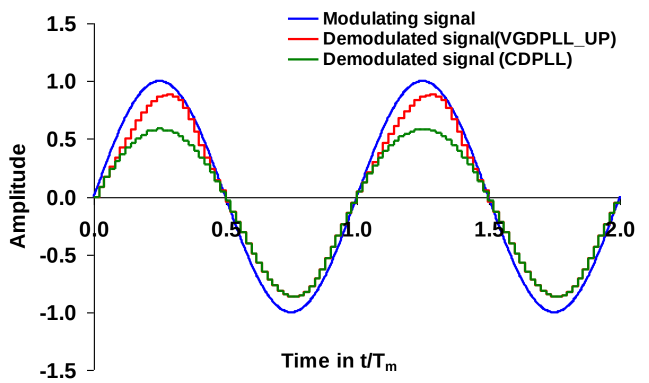

Fig. 5b. Plotting of FM demodulated signal using CDPLL and VGDPLL_UP. (With $K_0 = 1.8$, $\omega_0/\omega_m = 50$, $K_1 = -0.4$ and $m_f = 10$) (Simulation Result)

V. Conclusion

An algorithm of variable loop gain of a CDPLL has been proposed to get a VGDPLL_UP structure, which have symmetrical acquisition range. The VGDPLL_UP thus obtained have better performance as FM demodulator, as far as the distortion of the demodulated output is concerned. A detailed simulation study of the proposed system has been carried out to arrive at these conclusions.

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