

CNTFET based low noise amplifier (LNA) for BLUETOOTH applications

Roohi Fatima, Mr. AmitGangopadhyay

Department of Electronics Engineering, Manalayatana University, Beswan, Aligarh

E-mail:- ecroohi786@gmail.com

Abstract-Low noise amplifiers (LNAs) for wireless PAN has been implemented using carbon nano-tube FET (CNTFET) as the device technology. This project focuses on the development of LNA for BLUETOOTH application (2.4 GHz). The designed circuit uses inductors to implement the matching networks. The performance investigation is done for the two LNAs using only one CNTFET and using two CNTFET2 in this project. The LNA transfer gain (S_{21}) were found ~ 19.85 dB in single CNTFET but in double CNTFET2 it is found to be 24.95 dB and noise figure(NF) were 0.016 dB for single and 0.024 dB for double. An excellent simultaneous matching is provided at both input ($S_{11} \leq -19$ dB) and output ($S_{22} \leq -24$ dB) in case of double CNTFET2 as well as stability factor (K) >1 has been achieved. With $\frac{?}{?}$ V supply, this LNA consumes only ~ 30 μ W power only. The LNA performances like transfer gain(S_{21}), Noise figure(NF) and power consumption (P_{DC}) were investigated by key process parameters such as dielectric constant of gate oxide (k_{ox}), diameter of CNTs (D_{CNT}), thickness of gate oxide (t_{ox}) and gate length (L_{gate}).

I. INTRODUCTION

Today nanotechnology is a technological field of paramount importance, covering all aspects of nano-scale science and technology from multidisciplinary perspective. Downsizing the dimension from 100 nm to 1 nm, nanotechnology not only yields miniaturization of devices and enhancement of integration density but also features unusual physical, chemical and biological device properties. Driven by technology and market requirements, semiconductor electronics already has found its way into nano-scale dimensions[1,2].

Beyond this, novel nano-electronics materials and devices such as CNTs (Carbon Nano-Tubes) and GNRs (Graphene Nano-Ribbons) are forth coming on a medium scale (in 10-20 years). These developments are based not only on new technologies but also on novel theoretical concepts. CNTs have demonstrated outstanding potential for a wide range of applications, including field effect transistors (FETs) and high frequency electronics, thin film transistors and display electronic. Their small size, high mobility (near-ballistic electron transport), high intrinsic cut-off frequency, mechanical and thermal stability, high current carrying

density and their capability of having both semiconducting and metallic tubes make carbon based devices promising candidate to replace silicon-based devices in some applications. Single walled CNTs exhibits linearity properties far superior to Si or III – V based devices[2].

Secondly, most important issue is design of transceiver blocks in high GHz frequency range [1]. Interest has been shown in wireless bands around 2.4 GHz for high data rate wireless personal area network (WPANs). This band have been used worldwide and are well suited for applications such as WPANs and point-to-point links and are expected to allow a data rate of about 1.5 to 54 Mbps. The most important block in wireless receiver is LNA. Since designing of LNA is itself an issue and of single band LNA is also an issue of great importance.

II. PROPOSED CIRCUIT

The circuit presented in this paper has used inductively degenerated common-source topology and a buffer using CNTFET, as shown in figure 1(single CNTFET model) and figure 2(double CNTFET2 model). An important advantage of degenerated common-source topology is that one has control over the value of the real part of the impedance through choice of inductance L_s . Since, in common source topology source is grounded, hence grounding the major part of the noise that could have been contributed by source noise current.

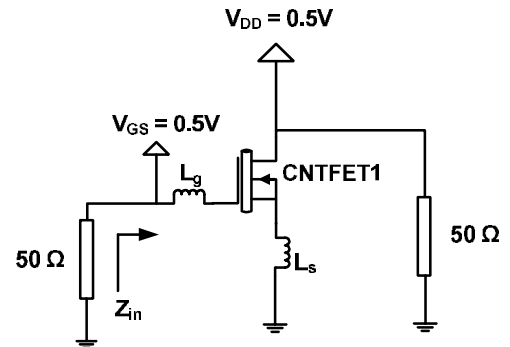


Figure 1: Proposed LNA circuit(Single CNTFET)

Second CNTFET (CNTFET2) as shown in figure 2, which is acting as buffer, is added in order to provide

isolation between input and output, so that input and output matching is achieved simultaneously. Using CNTFETs there is an effect of multiple gate fingers so there is lower value of parasitic capacitances and thus higher bandwidth is achieved.

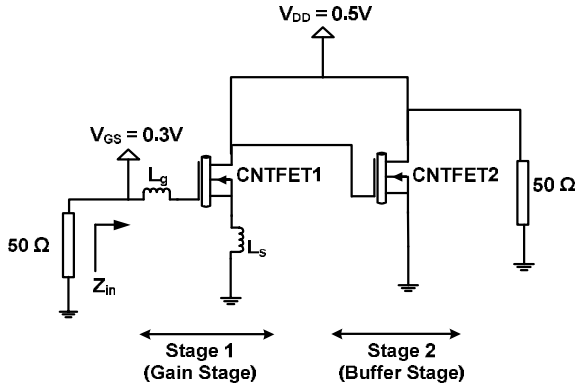


Figure 2: Proposed LNA circuit (Double CNTFET2)

The CNTFET in this circuit is described using Stanford University CNTFET model, as shown in figure. Every CNT can be characterized by a pair of indices (n,m) that define the chiral vector:

$$C = n.a_1 + m.a_2$$

Where a_1 and a_2 are the unit vectors of graphene in configuration space, as in figure. The chiral vector describes how the graphene sheet is wrapped around while the translation vector T is in the direction of the CNT axis. Using the index pair (n,m).

Due to the chirality, an energy gap that is only dependent on the geometry of the CNT varies between 0 and 1 eV. CNTs with vanishing energy gap are denoted as metallic or zero-gap nanotubes and the others are semiconducting nanotubes. The diameter of single-walled CNT (SWCNT) is given as:

$$D_{CNT} = \frac{a \sqrt{n^2 + m^2}}{\pi}$$

Where, a (lattice constant) = 2.49 Å, and (n,m) are the chiralities of SWCNT. The CNTs are taken with chirality (19,0) and thus the $D_{CNT} = 1.5$ nm. So the approximate width of CNTFET with 4000 tubes is found to be 85 μm. The L_{gate} of 32 nm and 2 nm thick (t_{ox}) Hafnium Oxide (HfO_2), having high dielectric constant (K_{ox}) of 25 was taken for CNTFET. With only single CNTFET in the circuit of figure, it was difficult to achieve input and output matching simultaneously. So second CNTFET (CNTFET2), is added. The designed LNA takes about 30.5 mA of current in single CNTFET when operated with V_{DD} equals 0.5 V. This leads to low power (15 μW) design but in parallel CNTFET2 61.1 mA of current is required which leads to high power (30 μW) design. With these design values the simulation result shows that this circuit is good for operation in higher GHz range.

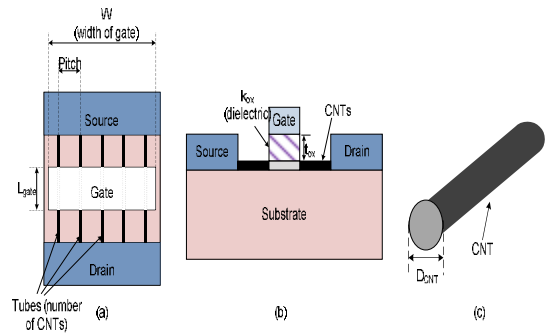


Figure 3: Process Parameters of CNTFET

III. CIRCUIT ANALYSIS

The CNTFET model used for analysis is the simplified model of figure 5. The input impedance of the LNA circuit of figure 1 is given as,

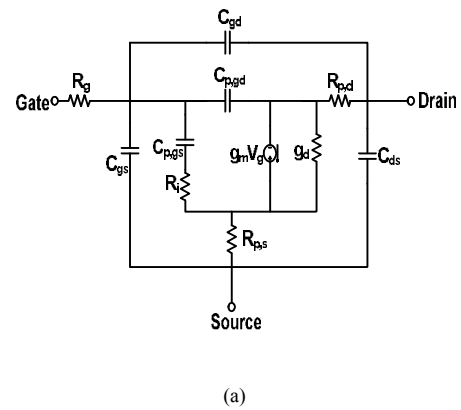
$$Z_{in} = j[\omega(L_g + L_s) - \frac{1}{\omega C_{gs}}] + \omega_T L_s \quad (1)$$

where Z_{in} is the input impedance of the first part of the circuit, L_g & L_s are inductors at gate and source terminals respectively, ω_T ($=g_m/C_{gs}$) is the cut-off frequency and ω is operating frequency. In order to match this LNA to a 50 Ω impedance we need to fulfill following conditions,

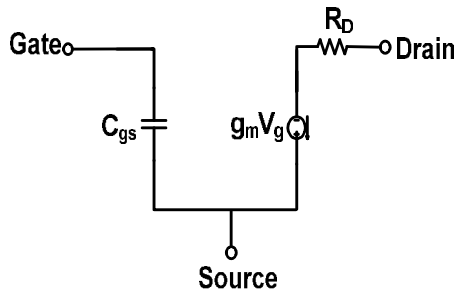
$$\text{Imaginary}(Z_{in}) = \omega(L_g + L_s) - \frac{1}{\omega C_{gs}} = 0 \quad (2)$$

$$\text{Real}(Z_{in}) = \omega_T L_s = 50 \quad (3)$$

C_{gs} in the small-signal model of CNFET (see figure 5), contributes to the imaginary part of the input impedance of the LNA circuit of figure . In order to cancel this part there should be a suitable value of L_g . In this topology, the real part is controlled by L_s and imaginary part by L_g , as evident from the equations (2) and (3).



(a)



(b)
Figure 5: Equivalent small-signal model circuit of CNTFET (a) including the parasitic component (b) Simplified model.

The V_{GS} is taken to be 0.5 V ($>V_1$ of CNTFET i.e. 0.25 V). And after various simulations and iterations it has been found that V_{DD} of 0.5 V is sufficient for the working of the circuit to achieve required performance. This leads us to low power design. On considering the circuit of figure 5, then it will give results for single-band CNTFET LNA.

IV. SIMULATION RESULTS

The circuit implementation in ADS is shown in figure 6 for single CNTFET model and figure 7 for double CNTFET2 model.

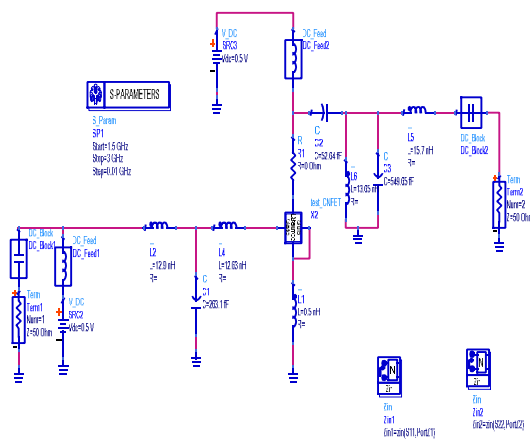


Figure 6: Single band LNA (2.4 GHz) implementation in ADS of single CNTFET

The performance of circuit of figure 6 and figure 7 is investigated at the 32 nm node (i.e. L_{gate}) with 0.5 V power supply and 4000 tubes. With these numbers of tubes width (W) of CNTFET is found to be around 85 μm . All the CNTs are taken with (19,0) chirality which are semiconducting and diameter (D_{CNT}) is 1.5 nm. The gate dielectric is taken to be 2 nm thick (t_{OX}) Hafnium Oxide (HfO_2) having high-K of 25.

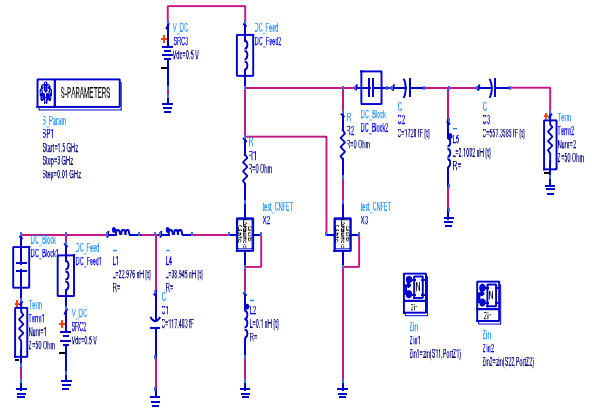
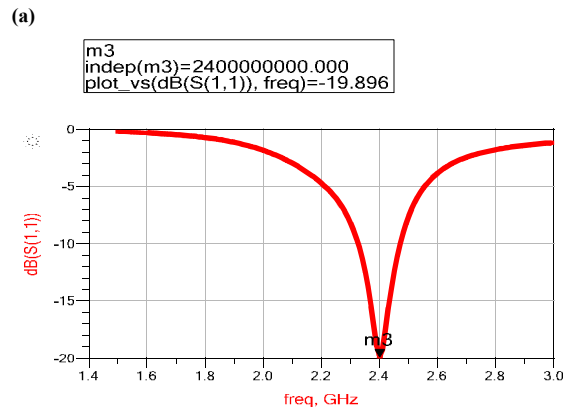
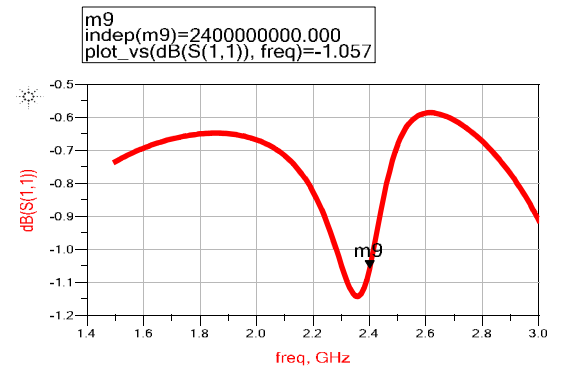


Figure 7: Single band LNA (2.4 GHz) implementation in ADS of double CNTFET2

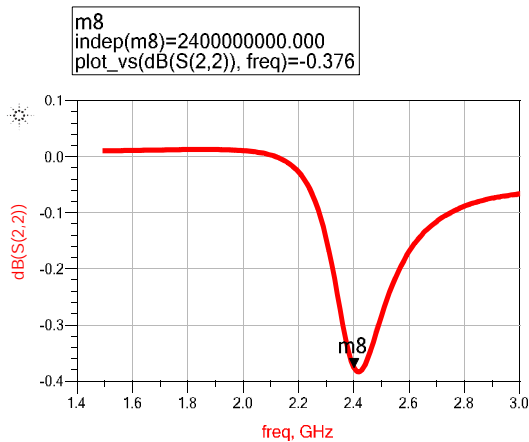
S-parameters:-Scattering parameters or S-parameters are extracted using ADS simulations which are shown in figure.

Input reflection coefficient (S_{11}):-At 2.4 GHz, S_{11} is -1.057 dB in case of single CNTFET but in double CNTFET2, S_{11} is -19.896 dB this value give good impedance matching as we observe from figure 8 (a) and (b).

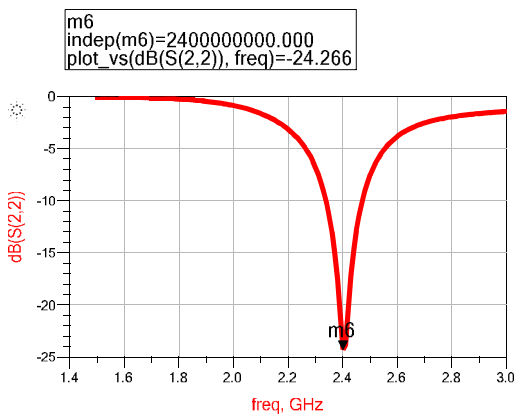


(a)
 (b)
Figure 8: Input matching coefficients (a) Single CNTFET (b) Double CNTFET2

Output reflection coefficient (S_{22}):- The S_{22} is find to be -0.376 dB in single CNTFET and -24.266 dB in double CNTFET2 at 2.4 GHz (see figure 9(a) and (b)).



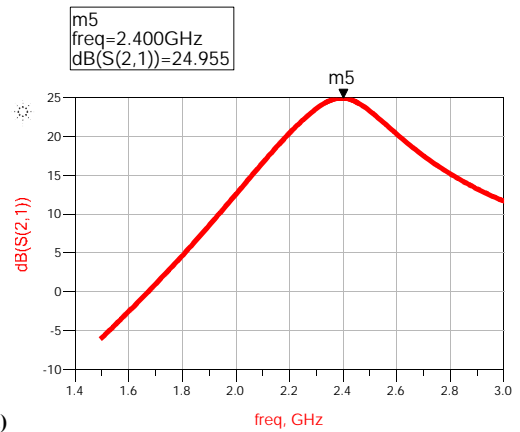
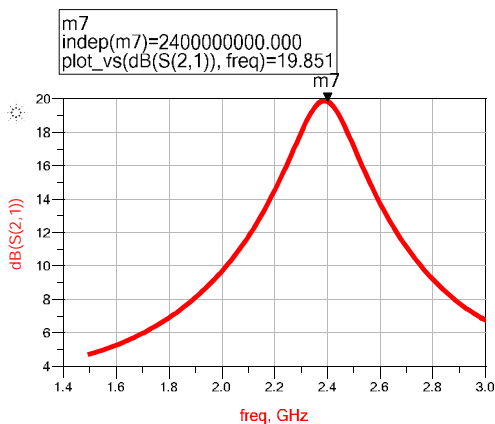
(a)



(b)

Figure 9: Output matching coefficient (a) Single CNTFET (b) Double CNTFET2

Transfer gain (S_{21}):- The S_{21} is 19.851 dB in single CNTFET and 24.955 dB in CNTFET2 as shown in figure 10(a) and (b).

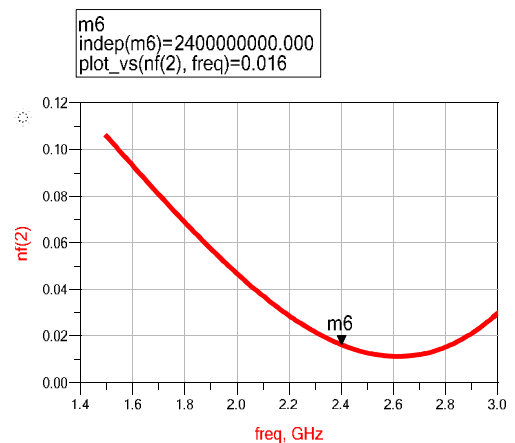


(a)

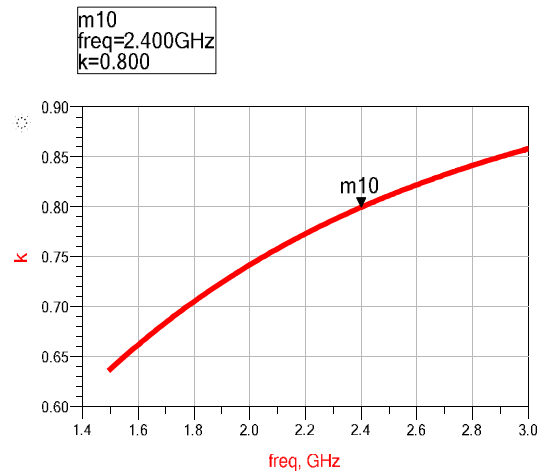
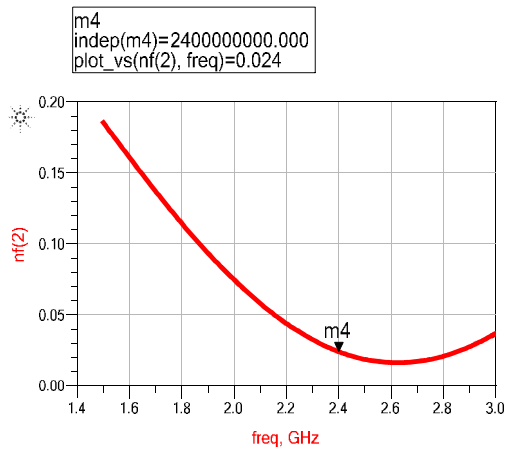
(b)

Figure 10: Transfer gain (a) Single CNTFET (b) Double CNTFET2

Noise Figure (NF):- The noise performance of an RF amplifier is represented by its noise figure or noise factor. It gives the measure of degradation of information signal due to noise in the device or circuit concerned. The plot for NF is shown in figure 11(a) and (b). The NF has such a low value required for LNA.



(a)



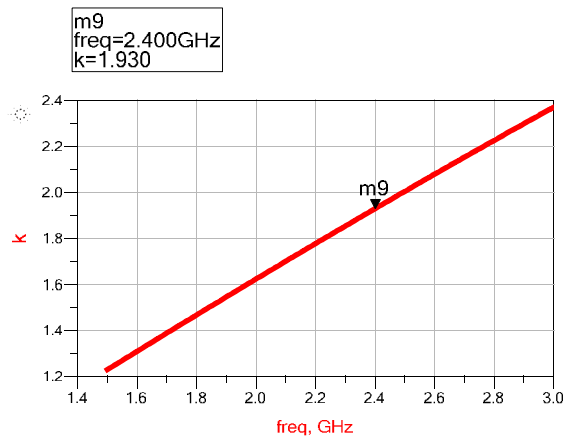
(b)

(a)

Figure 11: Noise Figure (a) Single CNTFET (b) CNTFET2

Stability Factor (K):-The stability factor at 2.4 GHz is found to be 0.8 in single CNTFET and 1.9 in CNTFET2 (see figure 12). In double CNTFET2 stages $K > 1$ that means the LNA circuit design is stable as compare to single stage.

Parameters	Single CNTFET	Double CNTFET2
Input reflection coefficient (S_{11} , dB)	-1.057	-19.896
Output reflection coefficient (S_{22} , dB)	-0.376	-24.266
Transfer gain (S_{21} , dB)	19.85	24.95
Noise Figure (NF, dB)	0.016	0.024
Stability Factor (K, dB)	0.8	1.9
Power consumption (μ W)	15.0	30.0



(b)

Figure 12: Stability Factor (a) Single CNTFET (b) Double CNTFET2

Power Consumption:-The power consumption of LNA for single CNTFET is 15μ W at the current of 30.5 mA at 0.5 V supply which is much lower than double CNTFET2 i.e 30μ W at the current of 61.1 mA at 0.5 V supply.

Table 1: Comparison of single CNTFET model parameters to the double CNTFET2 model

From the above table 1, The designed LNAs performance has been investigated and it has been found that double CNTFET2 model as compare to single CNTFET model gives very good results that are required i.e. high gain, low noise figure, low power consumption, excellent matching and good stability.

REFERENCES

- [1] A. Saleem, M.S. Alam and A.A. Moinuddin, "Carbon nanotube field effect transistor for Dual Band Low Noise Amplifier", IEEE Impact Magazine, June 2013, pp. 978-1205.
- [2] P. Russer and N. Fichtner, "Nanoelectronics in Radio-Frequency Technology", IEEE Microwave Magazine, May 2010, pp. 119-135.
- [3] N. Rouhi, D. Jain, and P. J. Burke, "Nanoscale Devices for Large-Scale Applications", IEEE Microwave Magazine, December 2010, pp. 72-80.
- [4] B. Razavi, "Design of Millimeter-Wave CMOS Radios: A Tutorial", IEEE Transactions On Circuits And Systems—I: Regular Papers, vol. 56, no. 1, January 2009, pp. 4-16.
- [5] C. Kocabas, H.-S. Kim, T. Banks, J. A. Rogers, A. A. Pesetski, J. E. Baumgardner, S. V. Krishnaswamy, and H. Zhang, "Radio frequency analog electronics based on carbon nanotube transistors", PNAS, vol. 105, no. 5, February 2008, pp. 1405–1409.
- [6] R. Chau, J. Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, "Emerging Silicon and Non-Silicon Nanoelectronic Devices: Emerging Silicon and Non-Silicon Nanoelectronic Devices: Opportunities and Challenges for Future High-Performance and Low-Power Computational Applications ", Invited Paper, Components Research, Logic Technology Development, Intel Corporation.
- [7] T.H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, second edition, 2004.
- [8] S. Ehrampoosh and A. Hakimi, "High Gain CMOS Low Noise Amplifier with 2.6 GHz Bandwidth", 1st International Conference on Communication Engineering, University of Sistan&Baluchestan, December 2010, pp. 72-76.
- [9] M. El-Nozahi, E.S. Sinencio, and K. Entesari, "A CMOS low-noise amplifier with reconfigurable input matching network", IEEE transactions on microwave theory and techniques, vol. 57, no. 5, May 2009, pp. 1054-1062.
- [10] J. Deng, and H.-S. Philip Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Non

idealities and Its Application—Part I: Model of the Intrinsic Channel Region", IEEE Transactions on Electron Devices, vol. 54, no. 12, December 2007, pp. 3186-31

- [11] A. Lin, G. Wan, J. Deng, and H.S. Philip Wong, "A Quick User Guide on Stanford University Carbon Nanotube Field Effect Transistors (CNFET) HSPICE Model v. 2.2.1", Stanford University, September 9, 2008.