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An Efficient Design of Full Subtractor Cell and its Application in Ripple Borrow Subtractor

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***Abstract*—This paper proposes a novel design of full subtractor. The design is intended to minimize leakage power and circuit area. Proposed full subtractor is designed by using three transistor x-or gate to generate difference and a Differential Cascade Voltage Switch Logic (DCVSL) multiplexer to generate borrow. The design technique ensures lesser circuit area and lesser power dissipation in nano scale very large scale integration (VLSI) systems for a wide range of power supply voltages. Simulations were carried out by using Tanner EDA tool, Dsch2, Microwind and LT Spice at 35nm technology. Percentage reduction obtained in power is 62%, in area is 41.98% and percentage reduction in noise is 50.4% compared to the existing MTCMOS technology. Using the full subtractor circuit a ripple borrow subtractor is also designed.**

***Index Terms*—CMOS circuit, DCVSL circuit, full subtractor, leakage current, low power design, ripple borrow subtractor.**

I. INTRODUCTION

Main strategy of VLSI design engineers was performance and miniaturization at the early days. But today most of the portable devices demand higher battery life time. While the non-portable devices also demands low power designs to avoid the burden of heat removal and cooling techniques. Hence to reduce package cost. For these reasons power dissipation becomes a challenge for circuit designers and a critical factor in the future of nano scale designs. Power consumption in CMOS circuits can be categorised into three: short-circuit power, switching power and static power or leakage power [7].

Short-circuit power arises when a conducting path is formed between power supply and ground. To eliminate this short circuit power dissipation the rise time and fall time of the transistors must be equal. This can be achieved by proper sizing of both the pull-up and pull-down circuits. This component of power consumption can be significant especially in dynamic circuits. Switching power is a result of the power consumed due to charging and discharging of internal capacitances in the circuit. Leakage power is the power dissipation due to all the leakage currents present in the device.

Different levels of optimization are carrying out to reduce power consumption. They are mainly in logic style adapted, in technology used, in algorithm used if any, and inthe circuit architecture.

In this paper a full subtractor circuit is designed to reduce the static power dissipation. The major techniques involved in this design are Pass Transistor Logic and DCVSL based multiplexer. By using this method low power area efficient full subtractor can be designed.

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II. FULL SUBTRACTOR CIRCUITS

A. Conventional Full Subtractor Circuit

A full subtractor is a combinational circuit specially designed in arithmetic unit to perform subtraction. It takes three inputs and gives difference and borrow as outputs. The inputs are minuend, subtrahend and borrow. In the subtraction operation subtrahend is subtracted from minuend by considering a 1 may have been borrowed by a lower significant stage [4]. The truth table of the full subtractor is shown in Table 1. The inputs are A, B and C and outputs are Difference and Borrow.

TABLE I TRUTHTABLE OF FULLSUBTRACTOR

A	*B*	*C*	*Difference*	*Borrow*
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The outputs of the full subtractor can be expressed in Boolean logic expressions as:

Difference = A ^ B ^ C
Borrow = C (A'B' + A B) + A'B

The CMOS level circuit diagram of full subtractor is shown in Fig.1.

B. MTCMOS Full Subtractor Circuit

MTCMOS technique is a variation of CMOS chip technology. MTCMOS stands for multi threshold CMOS technique. The technique is designed with transistors having multiple threshold voltages. That is it uses low, normal and high threshold voltage transistors to design the circuit [3] [4]. Low threshold voltage transistors have high performance but have significant power consumption. Hence low threshold voltage transistors can be used in critical path. High threshold transistors have less power consumption with a compromise in performance. Hence high threshold voltage transistors can be used in shortest path to reduce power consumption.

MTCMOS circuit has two modes of operation. One is active mode and other is the sleep mode. The modes of operations are determined by sleep signal. When the sleep

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signal is logic low the high Vth transistors turn ON and circuit enters to the active mode of operation. Circuit performs the full subtractor operation designed by using low threshold voltage transistors. However when sleep signal is logic high, the high Vth transistors turn OFF causing the circuit to enter to the sleep mode. At the sleep mode the leakage current is eliminated effectively.

The CMOS level circuit diagram of MTCMOS full subtractor is shown in Fig.2.

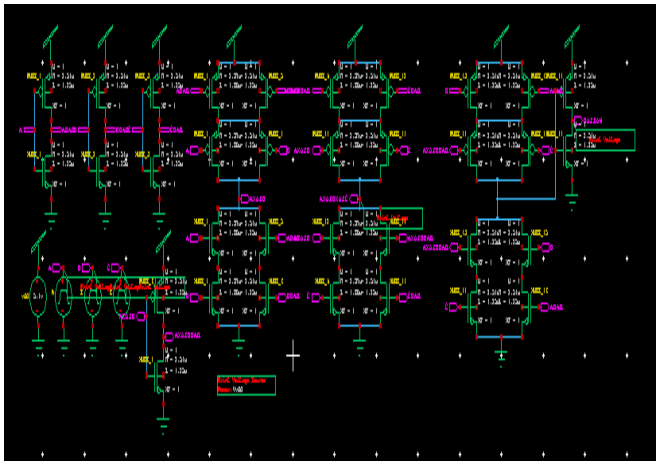

Fig.1. Circuit diagram of a conventional full subtractor.

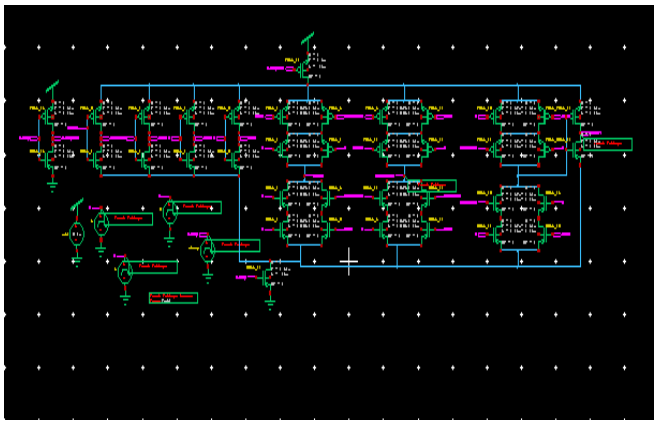

Fig 2. Circuit diagram of MTCMOS full subtractor.

III. Proposed Full Subtractor

The proposed full subtractor can be explained by considering both the difference and borrow circuit part separately. Basic block of difference circuit is a xor gate. The xor gate is designed in this paper by using three transistors.That is by using an inverter and pass transistor. Cascaded circuit of two such xor gates gives difference. Major purpose of this design is to reduce area and power significantly. Borrow circuit part is designed by using a multiplexer. From table1 it is clear that when A ^ B = 1 borrow is same as that of input B and if A ^ B=0 borrow is same as that of C. Hence a mux can be designed to choose between B and C depending on select signal A ^ B which is the output of first xor gate in difference circuit part. The multiplexer is designed by using DCVSL technique. DCVSL technique offers outputs in both the true and complementary form.The main advantage of DCVSL is its high logic density since the logic requires lesser number of PMOS transistors [2].

Circuit diagram of proposed full subtractor circuit and its timing diagram is shown in fig.3 and fig.4 respectively.

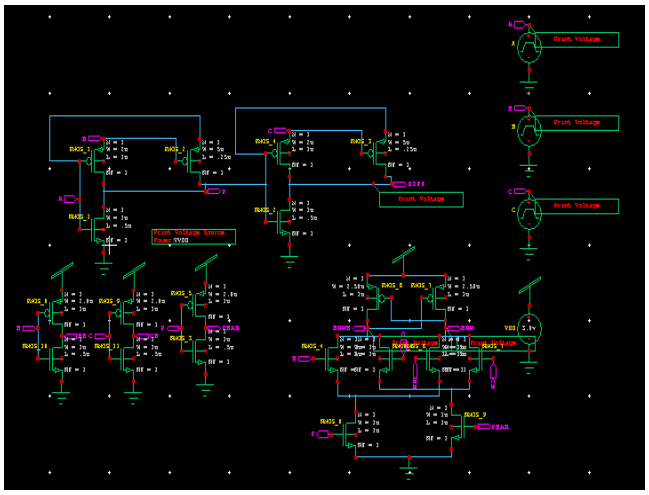

Fig 3. Circuit diagram of proposed full subtractor.

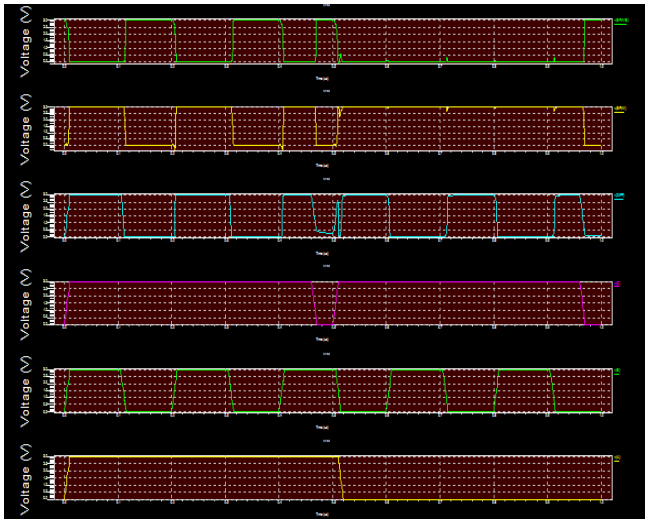

Fig.4. Waveform of proposed full subtractor.

IV. Simulations and Comparisons

Power simulation is carried out using tanner EDA tool. While noise and area simulations were done using LT Spice and microwind tools. All the simulation results are given in table 2. Fig.5,fig.6 and fig.7 shows the power simulation of the full subtractors discussed earlier.

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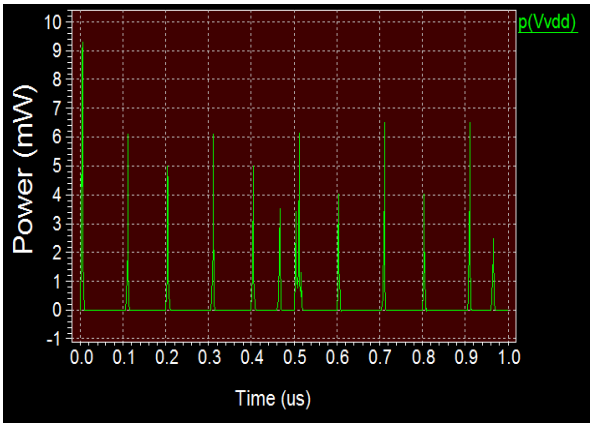

Fig.5. Power dissipation of conventional full subtractor.

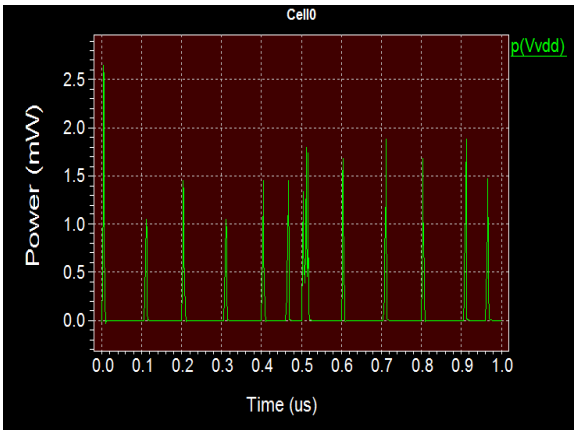

Fig.6. Power dissipation of MTCMOS full subtractor.

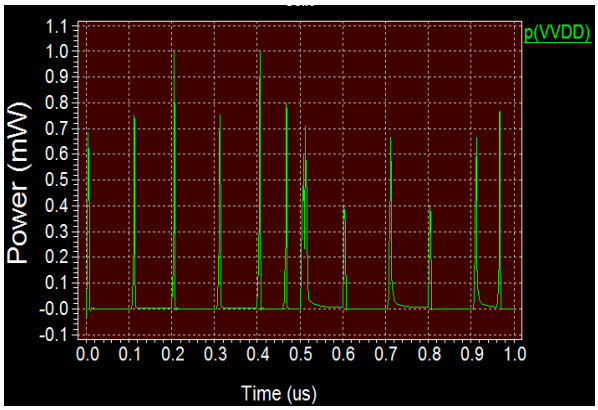

Fig.7. Power dissipation of proposed full subtractor.

While comparing with existing MTCMOS technique it is obvious that the proposed full subtractor has reduced area, power and noise and the percentage reduction in area, power and noise is 41%, 62%and 94% respectively.

TABLE IICOMPARISON OF VARIOUS FULLSUBTRACTORS

Circuit Parameter	Circuit Structure		
	Conventional FS	*MTCMOS FS*	*DCVSL FS*
Transistor count	34	38	20
Layout area (μm^2)	472.8	633.1	367.3
Power dissipation (mW)	9.25	2.65	1
Noise (pV)	17.52	33.89	16.782

V. APPLICATION OF PROPOSED FULL SUBTRACTOR IN RIPPLE BORROW SUBTRACTOR

It is possible to create a logical circuit using multiple full subtractors to subtract N-bit numbers. Each full subtractor stage takes an input a $Borrow_{in}$, which is the output $Borrow_{out}$ of the previous subtractor. Subtractor of this kind is called ripple-borrow subtractor, since each borrow bit "ripples" to the next full subtractor. The layout of a ripple-borrow subtractor is simple, which allows for fast design time.

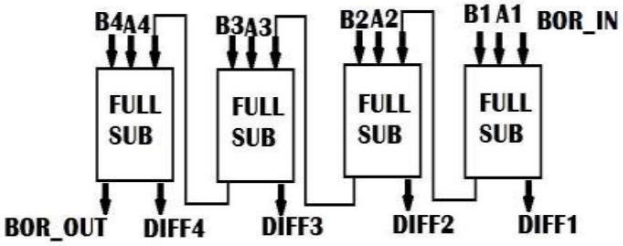

Fig.8. Block diagram of ripple borrow subtractor.

A ripple borrow subtractor is proposing here by taking the proposed full subtractor as the basic block. Since the proposed full subtractor gives complement of borrow part, the proposed full subtractor can be reduced as shown in fig.9. Need to provide an inverter at the initial stage and the reduced block can be used as such in successive blocks since it provides complementary borrow signal as well.

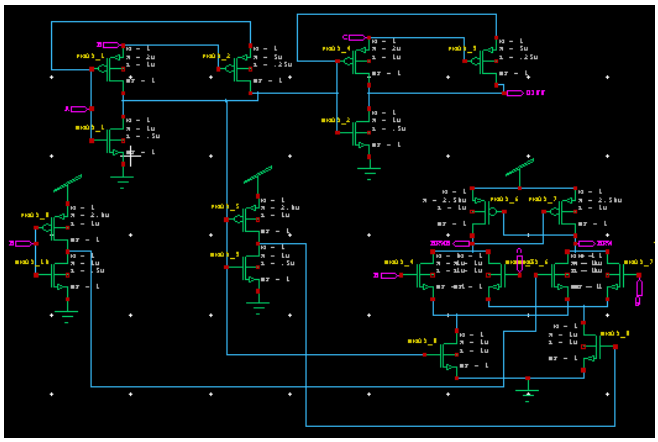

Fig.9. Single block of ripple borrow subtractor.

Fig.10 shows the ripple borrow subtractor using the circuit in fig.9.

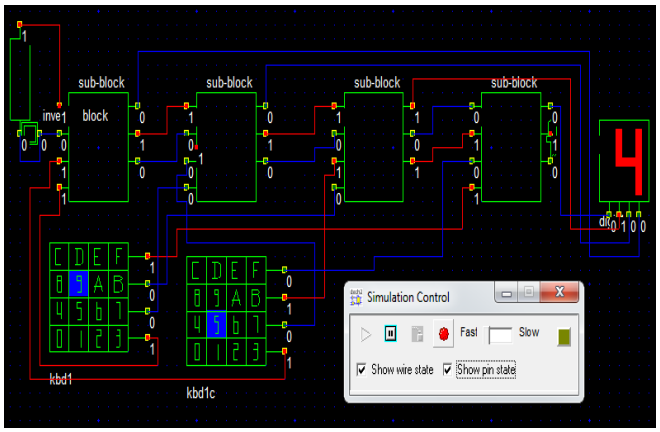

Fig.10. Proposed ripple borrow subtractor

VI. CONCLUSION

Using pass transistor logic, CMOS logic and DCVSL logic a novel full subtractor circuit has designed. It gives reduction in area, power and noise by 41%, 62% and 94% respectively. The tools used are Tanner EDA tool, Micro wind and LT Spice to find out power dissipation, layout area and noise respectively. All the simulations are carried out in 35nm technology. A four bit ripple borrow subtractor has designed using the proposed full subtractor for lesser area and power compared to the conventional ripple borrow subtractor circuit.

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