ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 3, March 2015

# ANALYSIS OF LOW POWER 32-BIT BRENT KUNG ADDER WITH GROUND BOUNCEING NOISE OPTIMIZATION

**Nisha, Asst.Prof. Anup Kumar**

*Abstract*— **Reducing power dissipation is one of the most important issues in deeply scaled technology. Sub-threshold leakage currents to become a large component of total power dissipation with the scaling of technology. Multi–Threshold (MTCMOS) technique is a promising way to reduce leakage power consumption of the circuits but it gives a problem called ground bouncing noise which reduces the reliability of the circuit. Ground bouncing noise produced during sleep to active mode transitions is an important challenge in Multi-Threshold CMOS circuits. The noise aware techniques Trimode, Stacking and Gated ground with variable Sleep transistor size MTCMOS circuit are applies to a prototype 32 bit Brent Kung adder to optimize the ground bouncing noise, Current surges and power consumption is presented in this paper. Simulate and analyze the results by using Cadence Virtuoso at 90nm technology node and comparative analysis of their performance is done with variation in supply voltage (VDD).**

***Index Terms*—Active mode, *Battery lifetime, Leakage power consumption, power gating, SLEEP mode.***

## I. INTRODUCTION

In high performance battery operated portable devices such as laptop, mobile phones and notebook power dissipation has become a very important design constraint. Shortening of battery life and additional packaging and cooling requirements are associated with high power consumption [1][2]. With the continued scaling of MOS devices, a theatrical enhancement in the performance of MOS devices has been achieved. However the sub-threshold leakage current is produced as the technology scaled [3]. Static power dissipation due to standby leakage currents is an important component of total power dissipation [4].The minimization of this leakage component is essential for effective power management [5].

Multi-threshold (MTCMOS) is the most commonly used leakage optimization technique and also called power gating [6]. In an MTCMOS circuits a high threshold voltage (High-Vt) sleep transistors are connected in the header and footer of the low threshold voltage (Low-Vt) logic blocks [7]. The sleep transistor can be a high –Vt PMOS transistor or a high-Vt NMOS .Header is a PMOS transistor connected between the real power line and a virtual power line and Footer is a NMOS transistor connected between the real ground line and a virtual ground line. These sleep transistors are cut off to reduce the sub-threshold leakage current in idle circuits [8]. MTCMOS circuits are operated in three different modes. Active mode, in which the sleep transistor is on and the circuit function normally. Sleep mode, in which the sleep transistor is shut-off and the leakage current of entire circuit is suppressed. The sleep transistor is switched 'off' to block leakage paths between the power and ground rails which could otherwise steadily draw power even during standby. Transition mode, is the operating mode at which the sleep transistor is turned on and the circuit goes from sleep to active. During the transition mode the high instantaneous current flow through the sleep transistor to the inductor of package parasitic will induced the voltage fluctuation on the real ground line. These voltage fluctuations on the ground line are known as ground bouncing noise [9]. Ground bouncing effect usually occurs in transition mode which is a very important issue in deeply scaled technology [10].

This paper is organized as. Ground bouncing noise is described in Section 2.32-bit Brent Kung adder design is explain in Section 3.Different noise optimization techniques are introduced in Section 4. Simulation results and analysis are presented in Section 5. Paper is concluded in Section 6.

## II. GROUND BOUNCING NOISE

Ground bouncing noise is the serious issue in a deeply scaled technology in MTCMOS circuits. It causes the false switching and poor signal quality in high speed circuits. Ground bouncing noise is a voltage fluctuation between the component package ground pin and reference ground level on component die. Basically it is caused by instantaneous current surge passing through the lead inductance of the package [10]. In MTCMOS circuits when low threshold logic block transition from sleep to active mode voltage fluctuation arise in ground distribution network as shown in Fig.1.If the amplitude of ground bouncing noise is more significant which will flipped the internal states of logic blocks causes malfunctioning the integrated circuits. The delay and dynamic switching power is increase as the voltage fluctuation increases. The ground bouncing noise is also reduced the noise margin of the circuit. The effect of ground bounce is more pronounced when all input and output switch simultaneously, so it is also known as switching noise.

***Manuscript received Aug 15, 2012***.
***Nisha,*** *Deptt. of E.C.E, A.K.G. Engineering College. Uttar Pradesh Technical University Ghaziabad, India, Phone/ Mobile No - +919891117442 Email- nisha_05ec29@rediffmail.com*
***Anup Kumar,*** *Deptt. of E.C.E, A.K.G. Engineering College. Uttar Pradesh Technical University, Ghaziabad, India.*
*Email- et_anup@yahoo.co.in*

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 3, March 2015

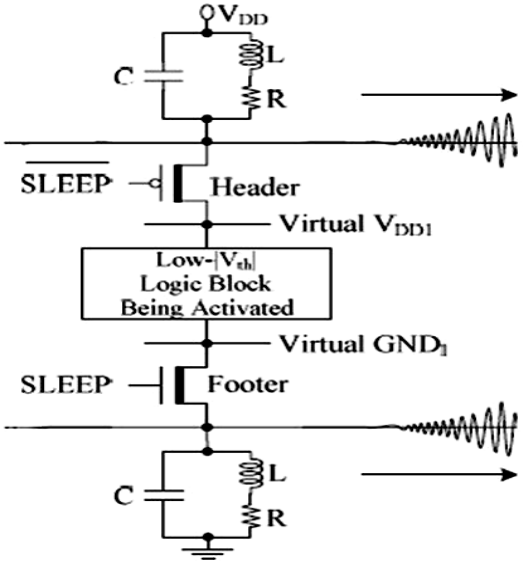


**Fig 1: Ground Bounce due to power gating**

$$g_i = a_i + b_i \quad (1)$$

$$p_i = a_i \oplus b_i \quad (2)$$

$$c_i = \begin{cases} g_i \\ g_i + p_i c_{i-1} \end{cases} \quad (3)$$

$$s_i = p_i \oplus c_{i-1} \quad (4)$$

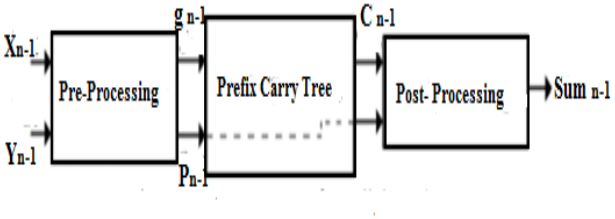


**Fig 2 : Block Diagram of Brent Kung Adder**

The amplitude of ground bouncing noise is due to parasitic impedance of on chip bonding wires pins of package, package lead frame and off chip distribution network. The package parasitic impedance plays a very important role in the generation of ground bouncing noise. R, L and C are the package parasitic resistor, the package parasitic inductance and package parasitic inductance. Inductance is the major component of generation of ground bouncing noise. The rate of change of instantaneous current in the sleep transistor during transition mode is related to the intensity of ground bouncing noise. The peak amplitude of ground bouncing noise is decreased as supply voltage decreases. Large sleep transistor is desirable for higher speed of operation but it will increase the ground bouncing noise [11]. The temperature and Supply voltage are another parameter on which the ground bounce depends at higher temperature, the saturation current of sleep transistor is reduced due to lower carrier mobility. At higher simulation temperature and supply voltage the power consumption and ground bounce is increased.

## III. 32-Bit Brent Kung Adder

Adder is the basic building block of any computational circuit. Brent Kung adder is the parallel prefix adder .In current technology it is the best adder with respect to area, time and good for high speed addition of large number of bits [12]. It is very efficient in terms of power consumption .Parallel prefix is a terminology described as parallel in this is define as the execution of operation in parallel i.e concurrent operation. Prefix describe as the outcome of the operation depends on initial value of inputs. This adder is considered as one of the best tree adders for minimizing gate count, wiring tracks and fan out used as a basis for many other networks. it computes the sum in three stages as shown as the block diagram in Fig 2. The binary addition usually expresses in terms of carry generation signal , carry propagation signal , carry signal , and sum signal , at each bit position ($1 \leq i \leq n$) where n is the number of bits , all these signals can be acquire by regard to the equation below:

Pre- Processing stage is the first stage in the Brent Kung adder design. It is used for the generation of carry generate signal $g_i$ and carry propagate signal $p_i$ as in equation (1) and (2). The first stage signal will proceed with the Second stage (prefix carry tree stage) to obtain all carry signals. This stage consists of three complex logic cells. it follow the equation (3) to produced carry bits. Carry bits that obtain from the prefix carry stage will pass through the last stage called post processing stage [13]. This stage generates the final sum of the adder following the equation (4).

## IV. Ground Bounce Optimization Techniques

As the technology is scaling down, the noise margins are also becoming very small. So optimize the ground bouncing noise to the least possible amplitude is very much essential. The primary factors which affect the amplitude of the ground bouncing noise are Supply voltage, Magnitude of current surge, Rate of change of current through sleep device (di/dt), Inductance value and size of sleep transistor. The peak amplitude of the ground bouncing noise increases with increase in any of the above parameter. Supply voltage and the inductance are fixed for a particular technology. So by manipulating the other three parameter current surge, dI/dt, and voltage swing values are able to minimize the ground bouncing [14]. The two parameter dI/dt and current surge value depend on the size of the sleep transistor. We can reduce them by decreasing the size of the sleep device but reducing the size of the affects the performance of the circuits. So the ground bouncing optimization techniques are focused on alternative method of reducing the current surge and dI/dt with size fixed and also the control of voltage swing taken care of while applying these techniques. The following section describes different techniques used to control the ground bouncing by controlling the different parameter like current surge, dI/dt, and voltage swing. The current surge value depends on the size of the sleep transistor. We can reduce them by decreasing the size of the sleep device.

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 3, March 2015

### A. *Gated ground MTCMOS with variable $W_{SLEEP}$*

In Gated ground power gating structure the high threshold NMOS transistor (SLEEP Transistor) is connected in the footer of low Vth logic block to optimize the power consumption of the circuit. Power consumption and Amplitude of Ground bouncing noise can be further reduced by resizing the SLEEP transistor. The Gated Ground Power gating structure is shown in Fig 3. In the conventional power gating circuits, the virtual ground is charged to $V_{DD}$ during sleep mode and discharge from $V_{DD}$ to $V_{GND}$ during wakeup. Thus there is a voltage swing of approximately $V_{DD}$ while transitioning from sleep to active mode. This causes a high peak value of the ground bouncing noise [11]. This amplitude of this noise is reduced by dividing the voltage swing in to two stage, i.e. from $V_{DD}$ to intermediate voltage $V_{PARKER}$ and then from $V_{PARKER}$ to $V_{GND}$. The following techniques use this principle for minimizing the noise is described in next section.

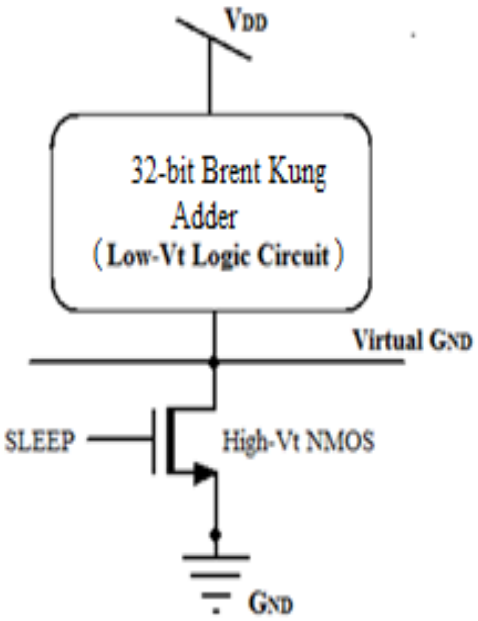


**Fig 3: Gated Ground power gating structure**

### B. *Tri-mode Technique*

In Trimode technique, an intermediate relaxation mode is created between sleep and active mode to gradually dump the charge stored on virtual ground line to real ground distribution network during the sleep to active mode transitions. The tri-mode power gating structure used to lower the ground bouncing noise is shown in Fig 4. High -Vt| sleep transistor are represented with a thick line in the channel region. A High-Vt PMOS transistor (Parker) is connected in parallel with the footer transistor (SLEEP) to implement an additional PARK mode [14] (utilized as an intermediate step between the sleep and the active modes) as illustrated in Fig.4. The Parker is activated while Sleep is maintained cut-off during PARK mode. Both Sleep and the Parker are turned off to reduce the sub-threshold leakage currents of an idle circuit.

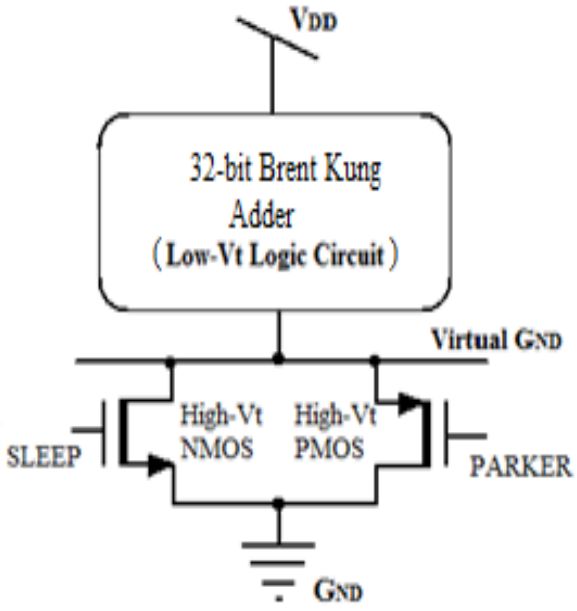


**Fig 4: Tri-mode power gating structure**

The voltage of the virtual ground line is maintained at ~$V_{DD}$ during the SLEEP mode. Prior to the activation of the circuit, the Parker is turned on while Sleep transistor is maintained at cut-off. The circuit transitions to the intermediate PARK mode. The virtual ground line is discharged to the threshold voltage of the Parker high-Vt, The first wave of activation noise is produced during the transition from SLEEP mode to PARK mode. High-Vt NMOS subsequently turned on to complete the activation process. The virtual ground line is discharged to ~$V_{GND}$. The second wave of activation noise is produced during the transition from PARK mode to ACTIVE mode. The activation noise is reduced due to the lower range of voltage swing on the virtual ground line with a two-step transition from SLEEP mode to ACTIVE mode through PARK mode Alternatively, the virtual ground line is discharged to the threshold voltage of the Parker (|Vtp |) [15]. The ground bouncing noise is reduced due to lower range of the voltage swing on the virtual ground line with a two step transition from the sleep mode to the active mode through the PARK mode. No complex circuitry is needed for the controlling the operation of the sleep transistor with this technique.

### C. *Stacking Technique*

In Stacking technique, stack of two Sleep transistors are use in place of single Sleep transistor. Two Sleep transistors are High-Vt NMOS1 and High-Vt NMOS2 as shown in Fig 5. This technique will reduces the leakage power consumption and peak amplitude of ground bouncing noise by suppressing the current surge on the virtual ground line. The voltage on the node ($G_{ND}1$) between the two Sleep transistors can be controlled by proper selection of delay $\Delta T$ and discharging capacitance $C_D$.

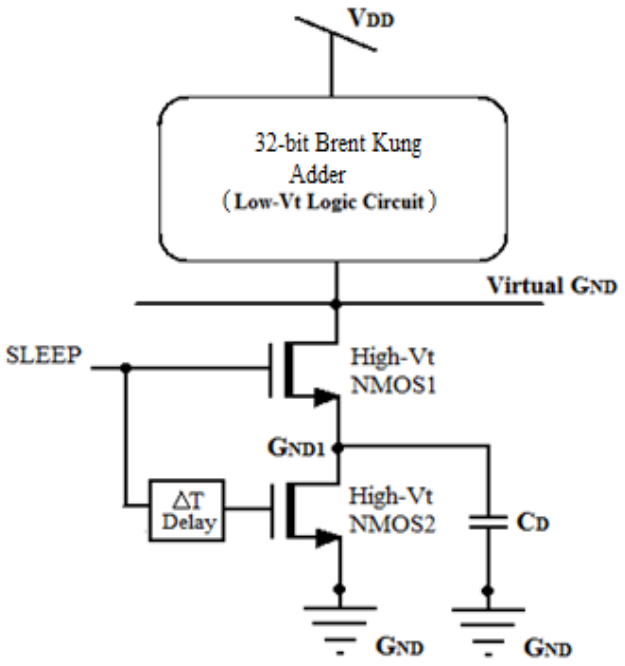


**Fig 5: Stacking Technique**

There are three operating modes of Stacking technique. In SLEEP mode both NMOS1 and NMOS2 Sleep transistors are in cut-off. This saves the leakage current and hence reduces the power consumption of the circuit. The virtual ground line is maintained at ~VDD. In ACTIVE mode both Sleep Transistors NMOS1 and NMOS2 are turned on. NMOS2 operate in linear region to reduce the current surges. The virtual ground line discharged to ~Vgnd. In TRANSITION mode High-Vt NMOS1 is turned on firstly after the delay Δ*T* High-Vt NMOS2 is turned on. During the duration at which NMOS2 is off, logic circuit is isolated from the ground. The peak amplitude of ground bounce is suppressed greatly in this duration, by operating NMOS2 in triode region and controlling the voltage at $G_{ND}1$ node. Δ*T* and $C_D$ are selected in such a way which will give minimum ground bouncing noise and walk up delay.

## V. SIMULATED RESULTS AND ANALYSIS

### *A. Simulation Setup*

The simulations are carried out in "Cadence Virtuoso" at 90nm CMOS Technology. The Brent Kung Adder is design with Low Threshold Voltage NMOS and PMOS FETs. This is used as low Vth circuit block which is connected in series with high Vth sleep transistor to minimize the leakage in sleep. The threshold value of low and high Vt NMOS and PMOS (Low-Vt NMOS=169mV, Low-Vt PMOS=-135mV, High-Vt NMOS=274mV, High-Vt PMOS=-244mV). The parasitic inductance, capacitance and resistance are taken from the dual in line package (DIP-40) package model. The simulation parameters are: Supply voltage VDD = 1V, the input string A0 – A31(0) and B0 –B31(FFFFFFFF) are added with carry input $C_{in}(0)$ and analyse the results at three different value of supply Voltage (VDD). DIP 40 packages parasitic are: Inductance L = 8.18 nH, Resistance R = 0.217 Ω and Capacitance C = 5.32 pF. Four 32-bit Brent Kung adders are designed based on four different techniques, CMOS adder, Gated ground adder design, Trimode adder design and Stacking method. In Gated ground simulation are performed at three different size of sleep transistor ($W_{SLEEP}$ = 5um, 4um and 3um).In Trimode and Stacking width of Sleep transistor is fixed i.e $W_{SLEEP}$ = 5um, with variable parker transistor size.

### *B. Simulation Results*

All techniques are implemented by using the centralized sleep transistor method. Gated ground MTCMOS is the best method to reduce the power consumption in the CMOS circuits but ground bounce is the big problem in these circuits. To minimize the ground bouncing noise width of the sleep transistor is reduced. Small size of sleep transistor will reduce the current surge through the Sleep transistor, which will reduce the voltage fluctuations. Simulation results of gated ground MTCMOS adder at 110˚C simulation temperature with $W_{SLEEP}$= 5µ is shown in Fig.6.The peak amplitude of ground bouncing noise is 43.35mV and virtual ground node is discharges from $V_{DD}$ to $G_{ND}$ as shown in Fig.6.

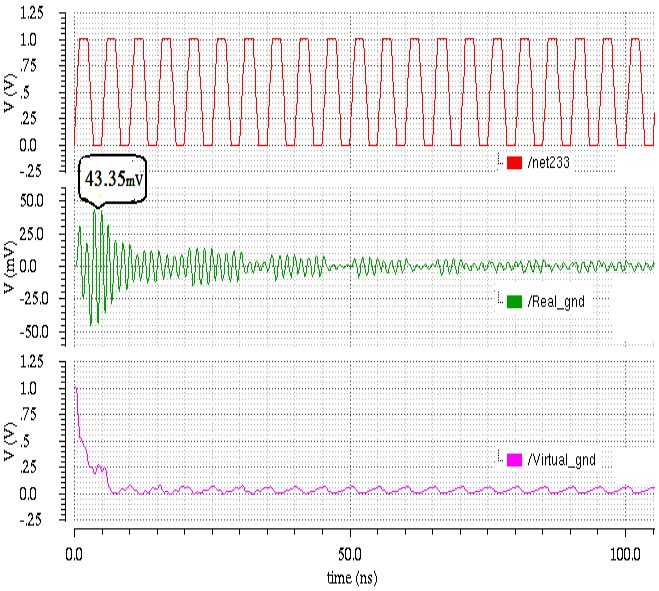


**Fig. 6 Peak amplitude of ground bounce in Gated ground MTCMOS Technique**

Trimode is the noise aware technique in which High-Vt PMOS (PARKER) is connected in parallel with High-Vt NMOS (SLEEP) transistor. Parker introduce the intermediate mode which reduces the peak amplitude of ground bounce at real ground.

Simulation results of Trimode adder at 110˚C simulation temperature with $W_{SLEEP}$= 5µ and $W_{PARKER}$=10µ is shown in Fig.7.The peak amplitude of ground bouncing noise in this case is 19.90 mV which is less in comparison to gated ground technique.

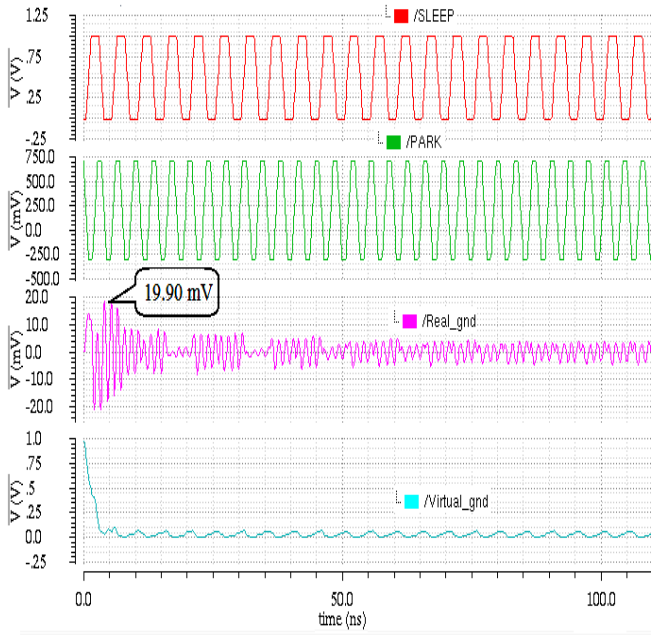


**Fig. 7 Peak amplitude of ground bounce in Tri-mode Technique with $W_{PARKER}$=10µ, $W_{SLEEP}$=5µ**

In Stacking technique two Sleep transistors are connected in series. Stack effect reduces the power consumption to the large extent. With the reduction of power consumption it will also suppress the ground bouncing noise more than the tri-mode technique. The peak amplitude of ground bounce in stacking method is 19.80 mV as shown in Fig.8.

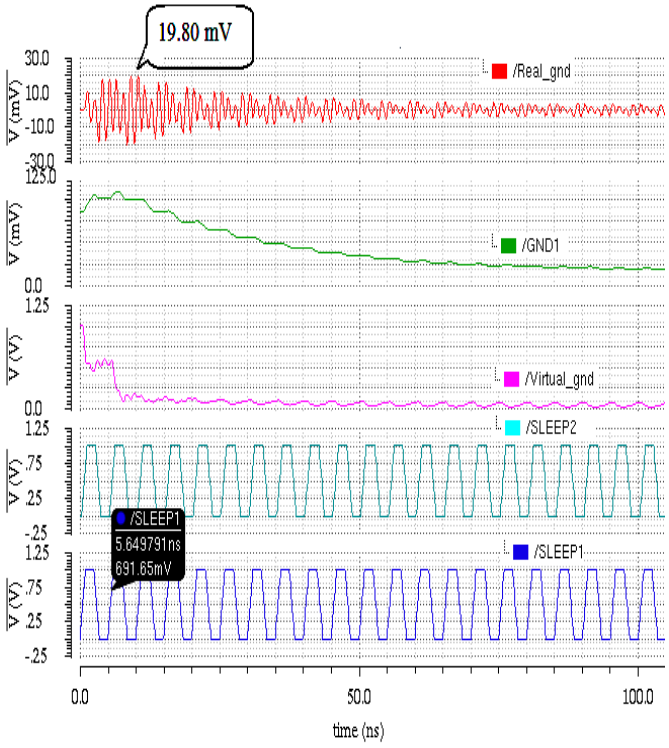


**Fig. 8 Peak amplitude of ground bounce in Stacking Technique with $W_{SLEEP1}$=5µ, $W_{SLEEP2}$=5µ**

### C. Results Analysis

The dependency of ground bouncing noise, power consumption and peak current surges with the different transistor size and supply voltage is analyzed in different noise aware techniques. The peak amplitude of Ground bouncing noise is analyzed at three different size of sleep transistor in gated ground technique and at five different size of Parker transistor with $W_{SLEEP}$=5u in Trimode. The peak amplitude of ground bouncing noise on the basis of simulation results in Gated ground MTCMOS, Trimode and stacking technique at three different value of supply voltage is tabulated in Table 1 and its corresponding graph is shown in Fig.9 and Fig.10.The graph in Fig.9 shows the ground bouncing noise w.r.t transistor size. As the size of Parker increases and supply voltage decreases the amplitude of ground bounce suppressed. Fig.10 shows the ground bouncing noise in different techniques. At the same transistor size that is 5µ Stacking technique gives the minimum amplitude of ground bouncing noise.

**Table 1: Peak amplitude of Ground Bouncing Noise (mV)**

| TECHNIQUES | | VDD | | |
|---|---|---|---|---|
| | | **0.6 V** | **0.9 V** | **1V** |
| **GATED GROUND MTCMOS** | **5µ** | 23.92 | 41.13 | 43.35 |
| | **4µ** | 23.43 | 36.99 | 39.19 |
| | **3µ** | 22.90 | 34.40 | 35.82 |
| **TRIMODE** $W_{SLEEP}$= **5µ** | **0.12µ** | 21.81 | 27.98 | 29.03 |
| | **5µ** | 14.60 | 18.44 | 19.90 |
| | **10µ** | 13.30 | 17.09 | 18.17 |
| | **12µ** | 12.98 | 16.76 | 17.90 |
| | **15µ** | 12.62 | 16.32 | 17.47 |
| **STACKING** | | 12.37 | 18.33 | 19.80 |

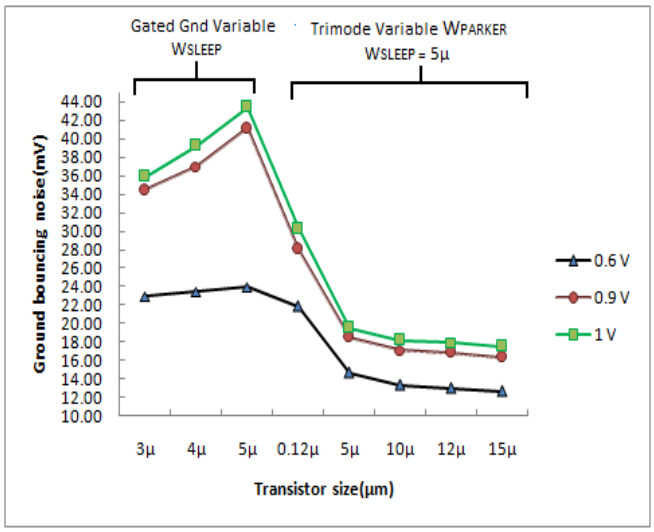


**Fig 9: Graph of peak amplitude of GBN w.r.t Transistor size at different VDD**

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 3, March 2015

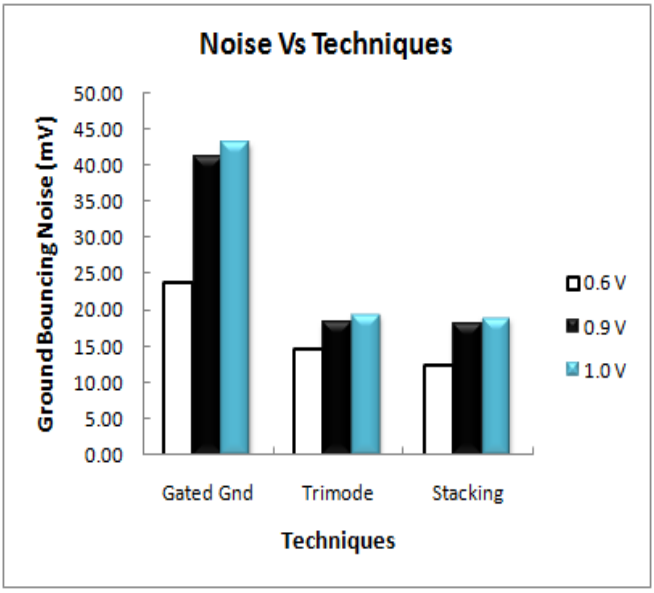


**Fig. 10: Comparison of different Technique for GBN at different VDD**

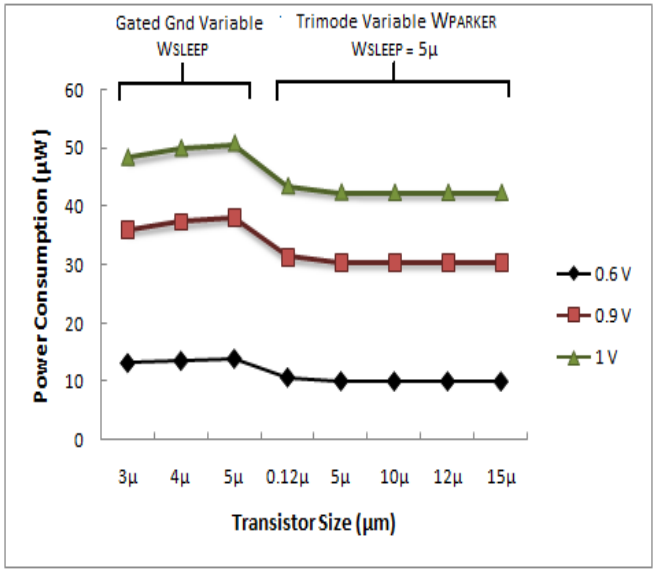


**Fig 11: Graph of Power consumption w.r.t Transistor size at different VDD**

The power consumption in CMOS adder is very large. Gated ground MTCMOS is reduces the power consumption approximately half in comparison to CMOS adder. The power consumption is maintained in all the noise aware techniques i.e Gated ground with variable $W_{SLEEP}$, Trimode and Stacking. The simulation results of power consumption in Gated ground MTCMOS, Trimode and stacking technique at three different supply voltage is tabulated in Table 2 and its corresponding graph is shown in Fig.11 and Fig.12. The graph in Fig.11 shows the power consumption at three different size of sleep transistor in gated ground technique and at five different size of Parker transistor with $W_{SLEEP}$=5u in Trimode. As the size of Parker increases the power consumption is reduced as compare to gated ground technique. Fig.12 shows the power consumption in different techniques. Trimode technique gives the minimum power consumption compare to other techniques.

**Table 2: Power Consumption (µW)**

| TECHNIQUES | | VDD | | |
|---|---|---|---|---|
| | | **0.6 V** | **0.9 V** | **1 V** |
| **CMOS ADDER** | | 40.63 | 56.92 | 77.79 |
| **GATED GROUND MTCMOS** | **5µ** | 13.81 | 38.08 | 50.80 |
| | **4µ** | 13.49 | 37.25 | 49.98 |
| | **3µ** | 13.11 | 35.94 | 48.43 |
| **TRIMODE** $W_{SLEEP}$= **5µ** | **0.12µ** | 10.70 | 31.34 | 43.55 |
| | **5µ** | 10.10 | 30.43 | 42.52 |
| | **10µ** | 10.06 | 30.39 | 42.47 |
| | **12µ** | 10.51 | 30.38 | 42.46 |
| | **15µ** | 10.05 | 30.37 | 42.45 |
| **STACKING** | | 13.19 | 35.43 | 47.01 |

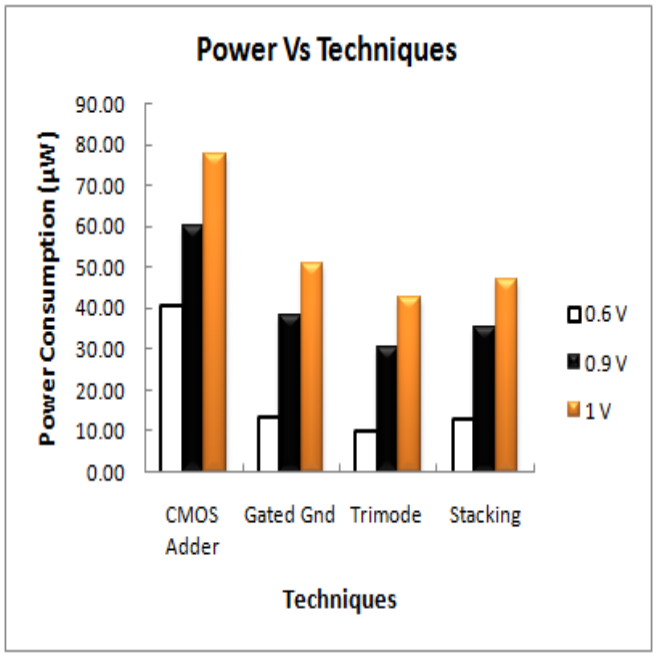


**Fig.12: Power Consumption Vs Techniques at different VDD**

Current surge is one of the important factor on which ground bouncing noise depend. It is the amount of current flow across the Sleep transistor pass through the parasitic inductor. The rate of change of current with inductor will produces the voltage fluctuation on the real ground line. The peak current surges in Gated ground MTCMOS, Trimode and stacking technique at three VDD Table 3 and its corresponding graph is shown in Fig.13.The current surges is decreases with the decrease in the VDD and increase in the size of the Parker transistor. Stacking technique has less current surges than other technique. Therefore, stacking technique reduces the ground bouncing noise.

**Table 3: Peak Current Surges (mA)**

| TECHNIQUES | | VDD | | |
|---|---|---|---|---|
| | | **0.6 V** | **0.9 V** | **1V** |
| **GATED GROUND MTCMOS** | **5µ** | 1.281 | 1.826 | 1.932 |
| | **4µ** | 1.120 | 1.522 | 1.602 |
| | **3µ** | 0.985 | 1.434 | 1.516 |
| **TRIMODE** $W_{SLEEP}$= **5µ** | **0.12µ** | 1.233 | 1.602 | 1.680 |
| | **5µ** | 0.775 | 0.983 | 1.049 |
| | **10µ** | 0.705 | 0.911 | 0.975 |
| | **12µ** | 0.691 | 0.892 | 0.959 |
| | **15µ** | 0.670 | 0.869 | 0.935 |
| **STACKING** | | 0.762 | 0.905 | 0.964 |

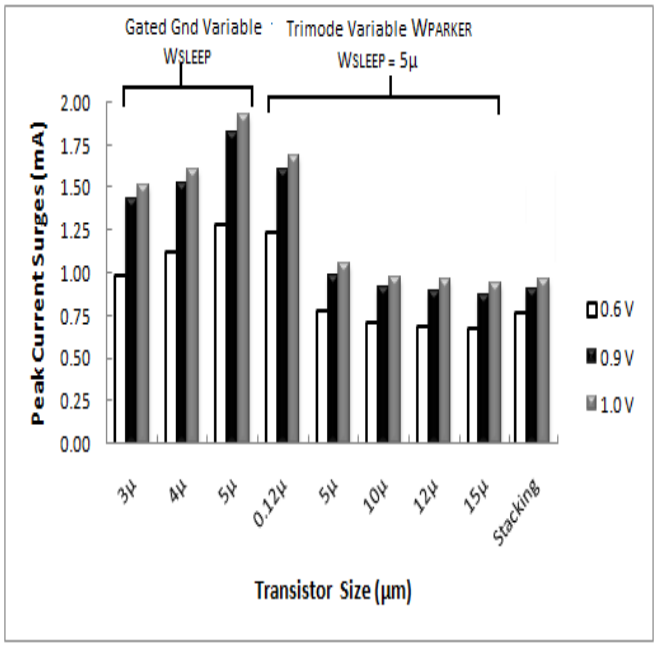


**Fig.13: Current surges Vs Techniques at different VDD**

## VI. CONCLUSION

Stacking and Trimode technique shows the highest reduction in the Leakage power consumption in sleep mode and ground bouncing noise during transition mode as compare to other technique with same Sleep transistor size.

It has been observed that Stacking technique reduces the ground bounce and current surge up to 54.32% and 50.10% in comparison to gated ground technique. Average power of 32 bit Brent Kung Adder can be reduces up to 40 % by using Stacking technique and 44% by using Trimode. Increase in supply voltage increase the power consumption and decrease the ground bouncing noise amplitude. By increasing sleep transistor size in Trimode the ground bounce reduces with the saving of the power consumption.

## ACKNOWLEDGMENT

I would like to thank Ajay Kumar Garg Engineering College for providing all the resources required for this work and their faculty member guidance.

## REFERENCES

[1] V.Kursun and E. G. Friedman , *Multi-Voltage CMOS Circuit Design. New York: Wiley*, 2006.

[2] S. Mukhopadhyay, H. Mahmoodi-Meimand, and C. Neau, Leakage in Nanometer Scale CMOS Circuits, *in Proc. International Symposium on Low Power Electronics and Design, pp. 307-312*, August 2003

[3] S. G. Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies, *New York: Springer-verlag*, 2006

[4] C. Piguet, Low power Electronics Design, *CRC press*, 2005.

[5] J.M. Rabaey,"*Digital Integrated Circuits: A Design Perspective"* Prentice-Hall 1996.

[6] S.Kim, S.V. Kosonocky, D. R. Knebel, and K. Stawiasz," Experimental Measurement of a Novel Power Gating Structure with Intermediate Power Saving Mode," in *Proc. the International Symposium on Low Power Electronics and Design*, pp. 20- 25, 2004.

[7] K. Shi and D. Howard Challenges in sleep transistor design and implementation in low-power designs, in *Proc. ACM/IEEE Des. Autom. Conf*, pp. 113–116., Jun. 2006

[8] Z.Liu and V.Kursun. "Leakage power characteristics of dynamic circuits in nanometer CMOS technologies," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 8, pp. 692–696, 2006.

[9] S. Kim, S. V. Kosonocky, and D. R. Knebel, "Understanding and Minimizing Ground Bounce During Mode Transition of Power Gating Structures*" IEEE International Symposiumon on Low Power Electronics Designs*, pp. 22-25, 2003.

[10] P. Heydari and M. Pedram, "Ground Bounce in Digital VLSI circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 11, No. 2, pp. 180-185, 2003.

[11] S. Kim, S. V. Kosonocky, D. R. Knebel, K. Stawiasz, D. Heidel, and M. Immediato, Minimizing Inductive Noise in System-on-a-chip with Multiple Power Gating Structures, in *Proc. European Solid- State Circuits*, pp. 16-18, 2003

[12] Kostas Vitoroulis, "Parallel Prefix Adders", Concordia University,2006

[13] Anas Zainal Abidin, Syed Abdul Mutalib Al Junid, Khairul Khaizi Mohd Sharif, Zulkifli Othman, "4-bit Brent Kung Parallel Prefix Adder Simulation Study Using Silvaco EDA Tools*", IJSSST*, Vol. 13, pp. 51-59, 2012.

[14] H.Jiao and V. Kursun "Ground-Bouncing-Noise-Aware Combinational MTCMOS Circuits," IEEE *Transaction on Circuits and System*, VOL. 57, NO. 8, pp. 2053-2065, 2010.

[15] H. Jiao and V. Kursun "Threshold voltage tunning for faster Activation with Lower Noise in trimode MTCMOS Circuits*" IEEE*

*1st International Symposium on Quality Electronic Design-Asia*, pp. 64-70, 2012.

[16] H. Jiao and V. Kursun, Noise-aware data preserving sequential MTCMOS circuits with dynamic forward body bias, *J. Circuits,Syst., Comput.*, vol. 20, no. 1, pp. 125–145, Feb. 2011.

**Nisha** received her B.E degree in Electronics and Communication Engineering from Institute of Engineering and Technology, Agra. She is pursuing M.Tech in VLSI design from A.K.G. Engineering College, Ghaziabad, and Uttar Pradesh, India. Her major areas of research work include Low power Circuit Design.

**Anup Kumar** is Asst. Prof. at A.K.G. Engineering College, Ghaziabad, Uttar Pradesh. He received his M.Tech degree in VLSI Design from Thapar University, Punjab, India.