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Carbon Nanotube Prospects as On Chip VLSI Interconnects

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***Abstract*— within the confines of the topic we aim to acquaint the need, present trend and viability of the research in CNT as on-chip VLSI interconnects. The need to discuss the topic arises from the fact that the conventional materials used as interconnects like Cu/Al are subjected to many glitches like high electromigration resistance, surface roughness, grain boundary scattering, interconnect scaling, multiple interconnect stacks, leakage power, support to FinFET etc. in nanometer regime. This in turn raises the need to explore new materials which are able to withstand the above limitations and suitable for signal transmission in THz range. Carbon nanotubes in different configurations such as SWCNT, DWCNT, MWCNT, GNR propose to be a viable supplement for conventional Cu/Al as interconnect material. This paper describes techniques followed by researchers to predict various design strategies to withstand the ever increasing demand of interconnects compatible with nanometer and sub-nanometer device scaling. The paper also aims to investigate the application of CNT as interconnect to specific technological nodes. It is realized in the process that CNT indeed satisfies to be the interconnect material if the mentioned strategies and cogitations are followed.**

***Index Terms*—TLM Interconnects, CNT, SWCNT bundles, Crosstalk, RLC interconnect, Simulation, MWCNT, MLGNR, MCB**

I. INTRODUCTION

The present scenario of modern high speed, high density CMOS VLSI circuits aim at decreasing feature size along with increasing chip dimensions which results in increased complexity and the problem cannot be ignored as we aim at faster, dynamic and minimal circuits which consume least of power without compromising on their functionality.

As we move towards deep submicron regime more no of interconnections are used to connect millions of devices. Thus resistance of wire increase significantly giving rise to propagation delay. Earlier Al & Cu interconnects were viable enough, but the shrinking of device dimensions caused these conventional interconnects to suffer from problems like high electromigration resistance, surface roughness, grain boundary scattering, interconnect scaling, multiple interconnect stacks, leakage power, support to FinFET and Tri-gate transistors. Tang et al. [1] found that the continuous decrement in the feature size has brought to the arrival of certain problems like signal integrity, delay, crosstalk, rise time, high contact resistance and high processing temperature at a much significant level in comparison with the past.

The sub100 nm regime subjects increasing challenges for both active and passive components on the chip. The continuous scaling of the feature sizes of transistors and interconnects, increase in transistor speed, propagation delays, increment in contact resistance etc. have become the dominant chip performance limiting factor [2]. Consequently, materials such as carbon nanotubes (CNTs), graphene, nanoribbons, and Ag nanowires are being considered as potential replacements for Cu in interconnects, due to their better electrical and mechanical properties [2]. CNT appears to be the most promising to replace Cu due to its ultrahigh current capacity and it's filling ability in high aspect ratio structures.

The present paper aims to find the various strategies followed to overcome problems with respect to the use of Carbon nanotubes as On-chip VLSI interconnects.

II. MODELS AND THEORIES FORMULATED

Hong Li et al. [3] reviewed CNT and GNR interconnects with respect to fabrication and modeling perspectives. It is found that Cu is inferior to SWCNT, DWCNT and MWCNT interconnects for delay performance as far as long global wires are concerned. MWCNT-based vertical interconnects (vias) being always metallic are preferred for interconnects. Electrothermal analysis of CNT vias concluded that they are both electrically and thermally ballistic proving their suitability for TSVs in 3-D IC integration as well as for various chip-to-packaging interconnect applications. A comparative study realized that taller CNT vias have better advantages than shorter CNT vias and the presence of large kinetic inductance, the skin effect is reduced by integrating them as CNT bundle, a promising prospect for future high frequency circuit applications.

Alessandro Giustiniani et al. [4] analyzed the performances of a semiglobal interconnect based on a densely packed SWCNT bundle. Valuable consequences related to nonlinear distributed parameters that exist in TLM were realized. It was concluded that unknown distribution of metallic CNTs on the bundle cross section affects the high frequency behavior of the interconnects due to capacitive effect while the presence of kinetic inductance forbids the insertion of equi-spaced repeaters which results in reduced time delay. The effect of high parasitic contact resistance between the CNT bundle and lumped circuit elements results in bandwidth decrease, thus constituting a bottleneck for the high speed application of CNT-based interconnects. All these resulted considering Multiconductor transmission line model matrices for

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Equivalent Single-Conductor TL Model parameters, avoiding arbitrary assumptions on the ESC location in the transverse plane.

P. Murugeswari et al. [5] compared the performance of carbon nano structures of SWCNT and SLGNR with Cu interconnect for on-chip interconnects applications and found that Carbon nano structures provide a justified replacement to copper on-chip interconnect to hold the Moore's law for future technology nodes as CNT structures have less delay and more bandwidth when compared to Cu. SLGNR and SWCNT produces only 0.5% and 0.7% of copper delay in global interconnect level and have 1000 times better energy efficiency than copper due to its ballistic transport and excellent thermal and electrical conductivity thereby has less power dissipation compared than Cu.

Fabrication and modelling perspectives are considered for SWCNT and MWCNT by Kaustav Banerjee et al. [6] The performance analysis concluded that dense and high metallic-fraction SWCNT may subdue MWCNT interconnects but they are easier to fabricate ignoring the chirality and density for horizontal wires including local, intermediate and global level interconnects. At higher frequency the presence of large kinetic inductance allows to ignore the current redistribution in a CNT bundle even at large cross-sections. As a result, CNT bundles exhibit unique characteristic for HF interconnect applications such as inductor in high-performance analog/RF circuits. The promising electrical and thermal properties of CNTs permits their application for chip-to-packaging interconnects.

Another scientific approach has been propose by Hong Li et al. [7] to find the applicability of MWCNTs as an interconnect candidate in future design of integrated circuits. The factors like diameter dependent MFP, technology scaling, chirality, signal delay were considered to validate their performance in comparison with SWCNT bundles and Cu as interconnect. It is concluded that MWCNTs are easier to fabricate with less concern about chirality, have long MFP and contributes to the conductance, even if the shell is of semiconducting chirality, signal delay is as low as 15% of Cu delay which has further scope of improvement with technology scaling. Hence, MWCNTs are viable to be used as horizontal wires in VLSI, including local, intermediate, and global level interconnects.

The present scenario of modern high speed, high density circuit aim at decreasing feature size along with increasing chip dimensions resulting in need of highly compatible interconnects. Kaustav Banerjee et al. [8] aimed at discussing various aspects of the same in context to CNT bundle interconnects. Nano metric dimensional issues like scaling of metal resistivity, surface and grain boundary scattering of electrons, small cross-sectional dimensions of local tier wires and vias that have the smallest cross-sectional dimensions among all on-chip interconnects were considered in specific. Extensive performance analysis of CNT bundle and comparison with same dimensional Cu interconnect suggested the CNT's winning edge over contemporary Cu interconnects. However, issues like process integration, lowering of nanotube's contact resistance for local interconnects and via, process integration, modelling of: electromagnetic interactions in CNT bundles, 3-D (metal) to 1-D (CNT) contact resistance, impact of defects on electrical and thermal transport and high-frequency effects need to be addressed.

Navin Srivastava et.al. [9] exclusively compared the performance of CNT bundle interconnects and Cu for thermal management, reliability, performance and, power dissipation as practical limitations of the technology. The expressions conclude that CNT bundles can significantly improve the performance of long global interconnects by as much as 80% with minimal additional power dissipation for maximum metallic CNT density. The extracted parameters match to different technologies to be preferred over as VLSI interconnect material and additional improvement may be attained with power-optimal repeater insertion and constructive usage of CNT bundle vias.

Kailiang Zhang1et. al. [10] presented a novel expression to analyze crosstalk in SWCNT bundle as an interconnect candidate. Based on ITRS scheme equivalent distributed circuit parameter models of SWCNT bundle are obtained and analyzed resulting in significant reduction in crosstalk noise on reduction in line length , appropriate positioning at determined length , space increment between adjacent lines, increasing the diameter of SWCNT and selecting the appropriate frequency.

The paper [11] utilizes an accurate model to discuss the crosstalk effects in coupled MWCNT interconnect lines applying FDTD method. The model emphasized both functional and dynamic crosstalk effects in coupled two and three interconnect lines extensible up-to n-coupled lines. The results obtained are in lue with HSPICE simulations suggesting the average error in the propagation delay measurement less than 1%.

A. M. Attiya [12] devised the relation between the resonance mechanism and the surface wave propagation expression for CNT bundle antenna. The frequency dependent attenuation coefficient of complex surface wave propagation has been evaluated which introduces highly damping effect reducing the active part of the dipole length. The dipole would be always below resonance resulting capacitive input impedance which limits the lowest frequency suitable for a CNT antenna to nearly 100 GHz for resonance and size reduction. And there exists no relation between the resonant length and the approximate RLC representation of parallel wire CNT transmission line. Based on the conclusions more accuracy may be achieved while selecting CNT interconnects for specific frequency application.

Nisha Kuruvilla1et. al. [13] devised a new model for calculation of characteristic impedance of SWCNT/bundled SWCNTs interconnects as a function of physical parameters such as length, diameter and frequency. The same was simulated in SPICE and compared with other published results. The dependence of characteristic impedance as a function of frequency and length of interconnects is also realized. The conclusions drawn appease the resolving of appropriate loading impedance for CNT interconnects to constraint signal reflections and attenuations and limit the range of frequencies that can be transmitted through these interconnects at different lengths under critical mismatch conditions.

P. Uma Sathyakam et.al. [14] proposed a hierarchical modelling approach of MESC and MTL models for mixed CNT bundle interconnects specifically to realize the ESC model of inter-CNT capacitance and tunneling conductance. The transient analysis of the same to estimate delay predicts better performance of MCB interconnects over MWCNT and SWCNT bundle interconnects.

The transmission performance based on ESC model and closed –form equations for equivalent inductance and capacitance of MLGNR interconnects are presented by Wen-Sheng Zhao et.al. [15] catering to side and top contacts. The resistivity of a MLGNR interconnect is characterized and compared with Cu, SWCNT bundle, MWCNT, respectively. The results predict that side contacts in MLGNR interconnects can achieve smaller resistance in comparison with that of top one for short interconnect length but, the edge roughness and Fermi energy are the constraining issues. The time delay analysis of MLGNR interconnect suggest their practicality for intermediate level over global interconnects in comparison to Cu when crosstalk effects considered.

S. Haji Nasiri et.al. [16] analyze the dependence of (MLGNR) interconnects on their dimensions and contact resistances applying TLM and linear parametric expression for the TF of a driver–MLGNR interconnect–load configuration. In doing so, sixth order linear parametric approximate relation is applied to simulate the step response and Nyquist stability analysis suggests instability and delay rise with increase in lengths, widths, or contact resistances. The time domain output responses and Nyquist plots suggests reduced propagation delays for MLGNRs than SWCNT bundle interconnects of same dimensions.

Vangmayee Sharda et.al. [17] realized that there is a reduction of propagation delay of two coupled line bus architecture with increasing length of MLGNR with increment of number of fins and MLGNR layers suggesting a good combination for minimizing crosstalk induced delays at global interconnect lengths.

Sathyakam P.U.et. al. [18] proposed the configuration of Mixed CNT bundles (MCB) with DWCNTs and metallic SWCNTs at the core and semiconducting SWCNTs at the periphery Multi equivalent single conductor (MESC) analysis realized that MCBs with the proposed configuration results superior than MWCNTs and other MCB structures at local, intermediate and global interconnect applications.

Circuit-oriented modelling techniques have been proposed and modelled by Wen-Sheng Zhao et.al. [19] for both CNT and graphene interconnects. The electrical performance of the same evaluated and compared with Cu suggests the use of SWCNT and MWCNT for long interconnects while SLGNR are more suitable with width less than 8 nm. The proposed ESC circuit model of an MLGNR suggests improvement for HF application. It is also proclaimed as the beginning of "all-carbon" interconnects era for the development of new 3-D ICs.

P.S. Raja et.al. [20] concluded that minimization of length and shell spacing with maximized width and average diameter of Mixed CNT bundle is preferred to upgrade .interconnect performance.

Relative stability analysis of SWCNT used in 3D-VLSI circuits is performed using TLM and Bode stability diagrams in [21]. It is concluded that an increase in the length or diameter of each tube brings the relative stability increase due to switching delay. Consequently, the system's step response tends to damp faster.

III. Conclusion

On the basis of various models predicted, simulated and verified by various scientists it can be concluded that CNTs application as VLSI Interconnects is one of the great possibilities to meet the ever demanding challenges of modern high speed, high density CMOS VLSI circuits which aim at decreasing feature size along with increasing chip dimensions. However the limitations of crosstalk, glitches, signal integrity, spikes, logic levels, rise-time, grain boundary, MFP, electronmigration etc. which become more significant in nanometer and sub nanometer regime can be brought to limitations if the above mentioned models are properly analyzed and strategies followed.

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