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High Throughput Vedic Multiplier Using Binary To Excess-1 Code Converter

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***Abstract*— Multipliers is one of the most crucial elements for computation present in speedy arithmetic and logic unit, Multiplier and accumulate unit, microprocessors, DSP's and many more. Since, the throughput of these units is evaluated in terms of the number of multiplication performed per unit time, while meeting the time constraints. Vedic multiplier is one of the most promising solutions as it the fastest and energy efficient as well. This paper proposes a novel 8*8 bit vedic multiplier which is based on ""urdhvatriyakbhyam sutra" and uses Binary to Excess-1 code converter as its key component to increase the speed and reduce the area utilized by the multiplier. We also compare the delay, area and power results of proposed multiplier with existing topology. The proposed multiplier is coded in VHDL. Xillinx ISE 12.4 have been used for synthesis and ISIM for simulation.**

Keywords*— Vedic multiplier, carry save adder, BEC-1, 8:4 MUX

I. INTRODUCTION

Multiplication is found to be one of the most tedious and time consuming tasks to be handled by ALU, MAC, DSP's[14]. Hence, Multiplier is the key element in determining the overall performance of the system design. Since, multiplication is the major part of most of the signal processing algorithms. Therefore, its very crucial to develop and implement speedy and efficient multiplier designs. Multiplication involves the partial product generation followed by the addition of those partial products. Vedic mathematics speeds up the multiplication by parallel product generation. Hence, vedic mathematics based multipliers have been the wide area of research. Vedic multipliers handle large bit tedious multiplications of N- bit multiplicands by breaking them into N/2 bit numbers and the process continues till 2*2 bit multiplicands are left. The proposed modified vedic multiplier is based on "urdhvatriyakbhyam sutra" or vertically and crosswise algorithm" since it is identified as the fastest algorithm.

II. VEDIC SUTRAS

The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge. Vedic mathematics deals with 16 sutras [1]. Which have been alphabetically arranged with their corresponding meaning. Only "urdhvatriyakbhyam sutra" is discussed in the paper, as discussion of all sutras is beyond the scope of paper.

1. Anurupye Shunyamanyat– If one is in ratio, the other is zero

2. Chalana-Kalanabyham– Differences and Similarities

3. Ekadhikina Purvena– By one more than the previous one

4. Ekanyunena Purvena– By one less than the previous one

5. Gunakasamuchyah– The factors of the sum is equal to the sum of the factors

6. Gunitasamuchyah– The product of the sum is equal to the sum of the product

7. Nikhilam Navatashcaramam Dashatah– All from 9 and the last from 10

8. Paraavartya Yojayet– Transpose and adjust

9. Puranapuranabyham– By the completion or noncompletion.

10. Sankalana-vyavakalanabhyam– By addition and by subtraction

11. Shesanyankena Charamena– The remainders by the last digit

12. Shunyam Saamyasamuccaye– When the sum is the same that sum is zero

13. Sopaantyadvayamantyam– The ultimate and twice the penultimate

14. Urdhva Tiryakbyham– Vertically and crosswise.

15. Vyashtisamanstih– Part and Whole

16. Yaavadunam– Whatever the extent to fits deficiency

A. Urdhvatriyakbhyam Sutra

This sutra is based on "Vertically and Crosswise" technique. It makes all the numeric computations faster and simpler. The prime advantage of urdhva multiplier based over the others is that with the increase in number of bits, area and delay increase at comparatively smaller rate in comparison to others [2]. Figure 1 shows the line multiplication of two 4-bit numbers[3].

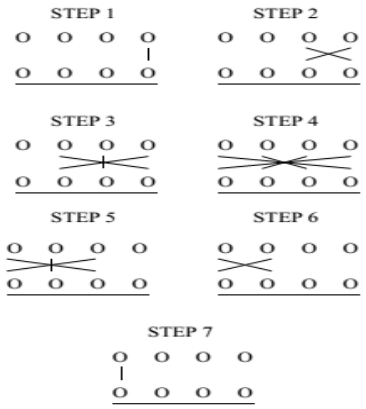

Fig. 1. Line diagram of four bit multiplication

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III. EXISTING TOPOLOGIES FOR 8*8 VEDIC MULTPLICATION.

A. *Conventional 8*8 Vedic multiplier*

The conventional architecture [7] of 8*8 bit vedic multiplier has been implemented using 4*4 vedic multiplier and three 8-bit ripple carry adders. Each ripple carry adder comprises of N-1 full adders, this adder in turn is a parallel adder as half adder and full adders are arranged in parallel way for computing result and carry. In this approach, combinational delay is found to be 21.644 ns. Results when compared with array and booth encoding multiplier shows reduced delay. The only drawback of this architecture is that each consecutive adder has to wait for the carry generated by the preceding adder. Therefore, this carry propagation restricts the performance of multiplier. Figure 2 shows the block diagram of 8*8 conventional vedic multiplier.

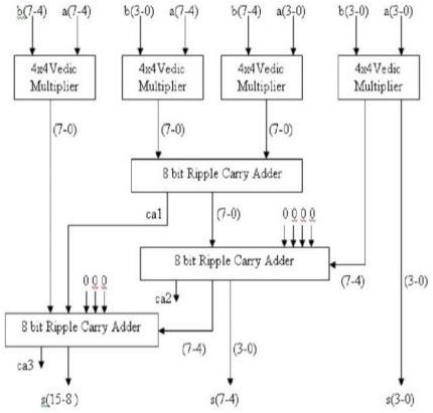

Fig. 2. Conventional 8*8 vedic multiplier

B. Modified Carry save adder based 8*8 Vedic multiplier

Modified vedic multiplier [8] uses 4*4 vedic multiplier, 2 operand 8- bit CSA and 3-operand 16-bit CSA for final product generation. CSA adders have been employed since they are fast adders and show significant decrease in routing delay as compared to RCA[10]. In this approach, combinational delay is found to be 21.608 ns which when compared with conventional architecture shows that CSA-based multipliers are faster. The main drawback of this approach is that it occupies more slices as compared to conventional multiplier.

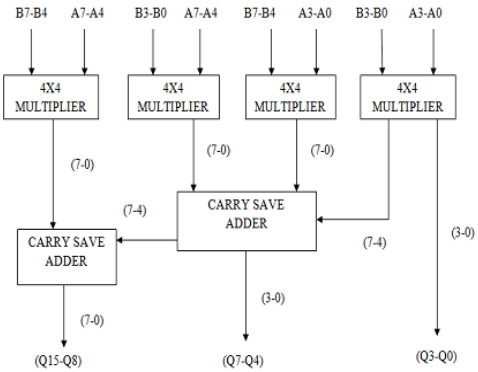

Fig. 3. Modified 8*8 bit vedic multiplier.

IV. PROPOSED BEC-1 BASED HIGH THROUGHPUT 8*8 VEDIC MULTIPLIER

The proposed Vedic multiplier architecture is divided into following blocks.

a) 4 bit vedic multiplier

b) Multioperand carry save adder

c) Binary to Excess-1 code converter

d) 8:4 MUX

Hardware implementation of BEC-1 8*8 bit vedic multiplier is shown in Figure 4.

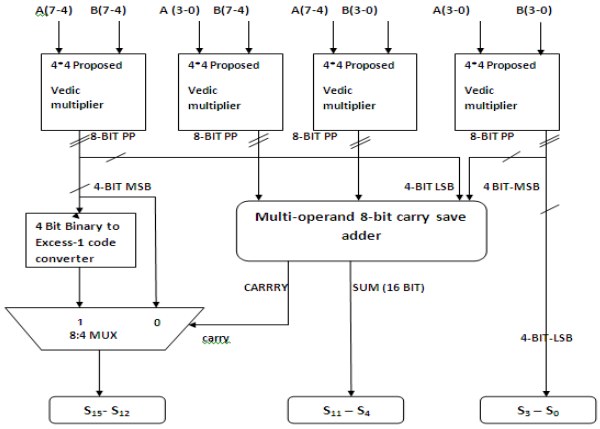

Fig. 4. Proposed BEC-1 based 8*8 vedic multiplier.

B. *4*4 bit Vedic Multiplier*

The 4*4 bit vedic multiplier structure can be decomposed into four 2*2 bit vedic multiplier entities generating partial product.

*1) 2*2 Bit vedic multiplier*

2*2 bit vedic multiplication exploits "vertically and crosswise" technique as shown in the following equations. Let X = x1x0 be the multiplicand and Y= y1y0 be the multiplier and P= p3p2p1p0 be the final partial product. Figure 5 shows 2*2 bit vedic multiplier comprising of 2 half adders, Hence, the total delay is the sum of delay of 2 half adders after partial product generation.

p0 = x0 and y0……...Vertically

c0p1 = (x0 and y1) + (y1x0)……..Crosswise

p3p2 = c0 + (x1 and y1)…….Vertically

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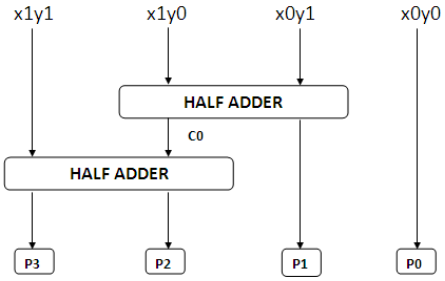

Fig. 5. 2*2 bit vedic multiplier

The "urdhvatriyakbhyam" technique can now be extended to 4*4 vedic multipliers. Let the multiplier be A= a3a2a1a0 and multiplicand B= b3b2b1b0 and the final product be S= s7s6s5s4s3s2s1s0. Figure 6 shows the 4*4 bit vedic multiplication using urdhvatriyakbhyam technique. Proposed architecture of 4*4 bit vedic multiplier consists of four 2*2 bit multipliers for generating partial products and a multi-operand fast carry save adder is used to add up the partial products and generates final product S= s7s6 s5 s4 s3 s2 s1 s0. Proposed architecture reduces the routing delay when compared to existing topologies.

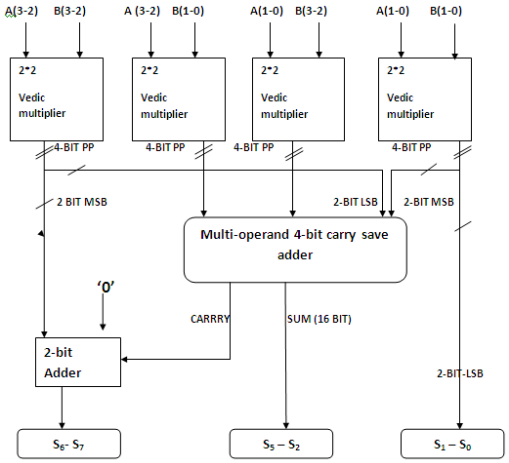

Fig. 6. Proposed 4*4 bit vedic multiplier

2) Binary to Excess-1 code converter

The proposed BEC-1 vedic multiplier architecture employs Binary to excess-1 converter is vital element. Purpose of using BEC-1 is that it reduces the delay time for addition drastically and occupies very less area as compares to full adders. As stated above the 2-operand carry save adder in the existing technology shown in Figure5 is replaced by BEC-1. It is observed from the results when compared with existing topology that proposed BEC-1 based Vedic multiplier is the fastest and most area efficient. Figure 7 [6] shows block diagram of BEC-1.

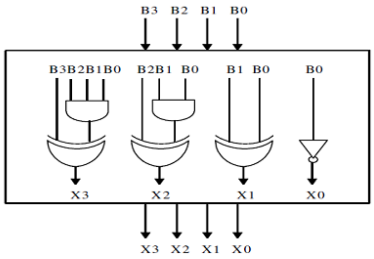

Fig. 7. 4-bit binary to excess-1 converter

3) 8:4 Multiplexer

8:4 MUX is used for conditional additional addition. If the carry obtained from multi-operand carrysave adder is '1' the, the output S(7-4) is taken from BEC-1 and if carry = 0. The output s(7-4) is directly taken from the partial products generated by the 4*4 bit proposed vedic multiplier.

4) Multioperand carry save adder

The carry-save adder [4] reduces the addition of 3 numbers to the addition of 2 numbers. The propagation delay is 3 gates regardless of the number of bits. The main application of carry save algorithm is, well known for multiplier architecture is used for efficient CMOS implementation of much wider variety of algorithms for high speed digital signal processing .CSA applied in the partial product line of array multipliers speed up the carry propagation[5].

V. SIMULATION AND RESULTS.

Simulation and synthesis is done using Xillinx ISE 12.4, and ISIM selecting device Spartan-3 FPGA (XC3S400-PQ208).

Here, the figure 9 shows RTL- schematic and figure 8 shows the test bench wave form generated by Xillinx ISE 12.4 and ISIM.

Table.1 shows the comparison of BEC-1 based vedic multiplier with Conventional vedic multiplier and modified vedic multiplier.

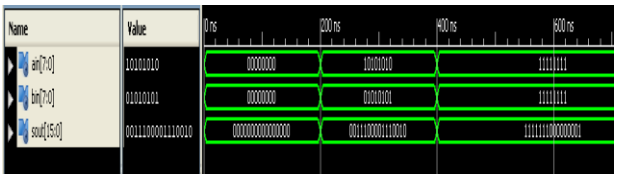

Fig. 8. ISIM waveform of BEC-1 based 8*8 vedic multiplier

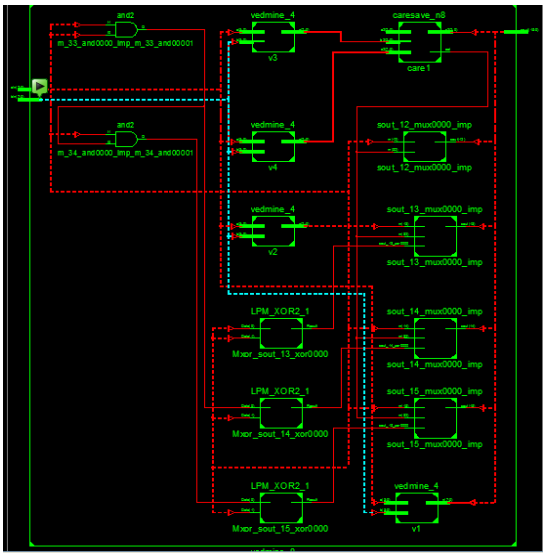

Fig. 9. RTL schemetic of BEC-1 based vedic multiplier

TABLE I: COMPARISION OF BEC-1 BASED MULTIPLIER WITH EXISTING TOPOLOGY

Vedic architecture	Delay	logic delay	Route delay	Slice utilization	4i/p LUT utilization	Logic level
Conventional architecture	21.644 ns	10.893 ns	10.751 ns	119	227	13
CSA based existing architecture	21.608 ns	11.372 ns	10.236 ns	104	204	14
Proposed BEC-1 based Architecture	**18.139 ns**	**9.996 ns**	**8.143 ns**	**100**	**196**	**11**

VI. CONCLUSION

High speed multipliers are the major requirement of DSP's and all arithmetic and signal processing units. Proposed BEC-1 based Vedic multiplier gives reduced logic and routing delay of 9.996 ns and 8.143 ns by decreasing the number of logic levels to 11 which is fastest as compared to existing topologies. Also, it utilizes least number of slices which makes it area efficient. So, it fulfills our motivation of both reduced area and reduced delay.

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