ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 6, June 2015

Review paper on Trends in Reconfigurable Computing

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Abstract- Properties such as flexibility, lifecycle upgrading, execution acceleration, and energy savings, make reconfigurable computing a foreseen solution for many applications. In this paper we introduce different trends in reconfigurable computing such as context switching configurations, partial reconfigurations. It also includes Heterogeneous Hardware computing, implementing C-programming on FPGA based systems. These trends tend to reduce the disadvantages posed by traditional reconfigurable computing. The scope of reconfigurable computing in scientific applications like embedded systems is increasing. Industries have developed C and C-like languages that are used for FPGAs. The C compilers here are different based on FPGA architecture. Reconfiguration process of the system needs a considerable amount of time. Reconfigurable aspect of FPGA is managed by internal memory. Multiple configuration bit streams stored in set of local storages in the FPGA device. Multi- context switching of configurations is internally now possible. Also enables operations of the system to continue while new configuration bit stream is loaded. The heterogeneous computing platform basically consists of different computing architectures such CPU, FPGA and highly parallel processors like Graphical Processing Unit (GPU). This leads to combining the advantages of all these Units.

Introduction

A CPU is an integrated circuit that contains many functional units used to interpret and execute program instructions. An FPGA, on the other hand, is essentially a collection of unconnected simple and complex functional units in hardware – the application programmer's code defines the connections among the functional units. The functional units are no more than simple hardware building blocks that may be interconnected to make more complex functional units. Properties such as flexibility, lifecycle upgrading, execution acceleration, and energy savings, make reconfigurable computing a foreseen solution for many applications. While ASICs take months to develop, have a substantial tooling cost, and cannot be changed, FPGA based designs take days to weeks to develop, have no tooling cost, and can easily be changed. Even better, ASIC design requires extensive hardware engineering expertise not required for reconfigurable system application development.

The CAD tools now fully support the emerging reconfigurable computing mechanisms including partial and run-time reconfiguration.

Module I:

In last couple of decades, specialized hardware description language (HDL), like Verilog or VHDL have been used in FPGA designs. With recent development in FPGA technology, it has improved the scope of reconfigurable computing in scientific applications beyond Moore's Law. Industries have developed C and C-like languages that are used for FPGAs. The C compilers here are different based on FPGA architecture, from those used in conventional CPUs. So the applications developed based on this need to follow different style of programming. One such environment is SRC Carte™ programming environment.

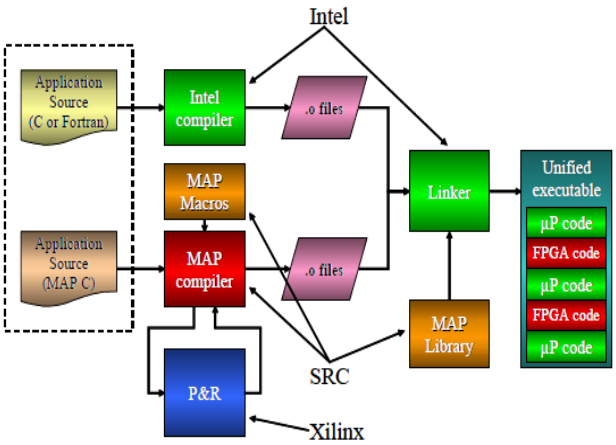

Fig1: SRC Carte™ Programming Environment[1]

The development process for FPGAs in reconfigurable systems [1]: For Programmer:

1) Outline an algorithm and identify the operand data, movement of data and result data.
2) Write a C program for the given algorithm.

- Steps by development tool:

3) This program or embodiment of algorithm is compiled and an intermediate hardware description language.
4) It is then fed to Vendor's tool.
5) The tool then performs the functional unit placement and its interconnect determination
6) Bit file is formed to be loaded on FPGA.

Module II:

One of the aspects of Reconfigurable Computing systems which makes it worth of modern application is the programmable logic resource for configuration management unit, provided by reconfigurable computing accelerators.

However reconfigurable computing presents a disadvantage that, reconfiguration process of the system needs a considerable amount of time. To overcome this, certain remedies are being implemented.

The reconfigurable aspect of FPGA is managed by internal memory, bits from which controls the connectivity and defines functionality for the units. The set of bit-streams, defining the hardware circuit, is called configuration. These configurations are created by software tools such as Computer aided design (CAD). If for certain applications the configurations for the system could change then the configuration overhead will hamper the speed performance. It is an emerging practice to provide a set of local storages in the FPGA device for holding temporary multiple configurations simultaneously [2]. Thus, the multi context switching capability can be introduced here. This kind of arrangement can now not only multi context the configurations but also enables operations of the system to continue while new configuration bit stream is loaded. And apparently, makes the switching between configurations faster, the bit streams being present with-in. Further, to reduce the configuration overheads, pipelined reconfiguration is introduced in some systems. Virtual pipeline stages are created so that during active operations of the device, they are allocated to the physical pipeline stage when one is available.

Module III:

Another way of accelerating the configuration process is to reduce the configuration overhead by reload only those streams which are new and reuse those streams which match the next incoming streams. This is partial reconfiguration [2]. Such devices have addressable configuration memory. It also permit a set of multiple independent configurations to be swapped in and swapped of the reconfigurable device quite independently. Hence one of the configurations can be selectively replaced on the device while another one is left intact [2].

An application as an illustration shows how partial reconfiguration is used. [3]Avionic systems are used in satellites. These systems are responsible for functional implementations such as orbit propagation and navigation, attitude determination and control. These systems are based on Commercial-Of-The-Shelf (COTS) components. These components make use of FPGAs. Earlier anti-fused FPGA were preferred by satellite developers due to radiation concerns in space environment. But these days reprogrammable FPGAs are found reliable too. The SRAM-based FPGAs (e.g. from Xilinx) help partial reconfiguration to be included in avionic systems. The partial reconfiguration helps to reduce threats posed in avionic systems by adaptive response to orbital changes. Thus it increases the reliability of system with affordable power consumption.

The concept of reconfiguration is realized in the Xilinx Virtex family by defining two main partitions: the fixed and reconfigurable. The fixed partition contains the static logic that should not change. The reconfigurable partition is tentative and can be loaded with partial bit streams of different designs. The fixed partition would contain the logic used to load the partial bit-streams representing there place able functions. The loading is done by accessing the external flash memory which holds the hardware design in the form of binary bit-streams. This configuration bit-stream is stored inside the FPGA in the form of frames in the FPGA SRAM. Reconfigurable FPGA can be designed in such a way that it contains multiple functions which can be swapped in and out according to the application requirements. This swapping mechanism needs all of the different functions to be available in an external flash memory that is accessible by the configuration controller as shown in Figure 7. Reconfiguration uses the Internal Configuration Access Port (ICAP).

Whenever a reconfiguration is needed, the configuration controller would load its partial bit-file, such as the partial bit-file A in Figure 7. Bit-files are loaded to specific partitions called the reconfiguration-partition which is planned on the FPGA floor using the PlanAhead tool from Xilinx. The loaded design can be overwritten by other partial bit-files whenever the FPGA needs to change its function. The fixed part of the design logic that should not be overwritten, is the configuration controller itself.

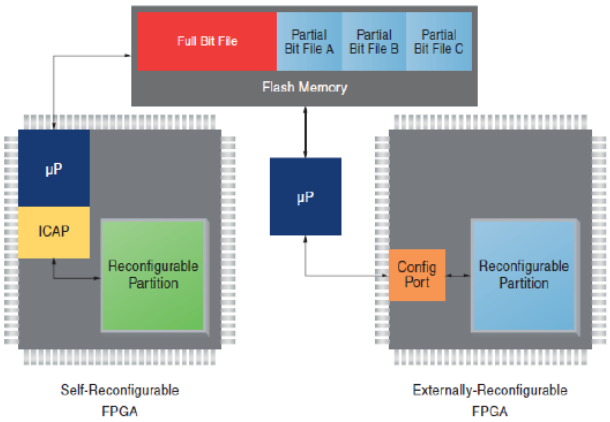

Figure 7 – Partial Reconfiguration Concept- Courtesy of Xilinx

[2]

Module IV:

These days, the actual reconfigurable logic is being implemented at different levels in a system. These levels could be categorised broadly,

a) As a functional unit:- Here FPGA is implemented as main functional unit.

b) As a Co-processor:- They perform computations without continuous supervision of host system.

c) As an external processor connected to I/O:- Connected to external I/Os and coupled to host system.

d) As a processing unit attached to memory:- They exhibit DMA-like operations.

Module V:

Heterogeneous computing is another recent trend that is being implemented in many high end applications. One such is discussed here.

[4]In today's world for fast development of science and technology people are demanding the high computational power to satisfy these demands; scientist and engineers have built super computers with hundreds and thousands of cores. As scale of supercomputer is getting large, the power consumption has increased leading to heat dissipation problems. For designing platforms specific applications using FPGA will increase the power efficiency.

Research on the brain network analysis plays a vital role in understanding the connectivity patterns of human brain and disease-related alternations. Both construction and analysis of brain networks requires tremendous computations. Here the power of heterogeneous hardware computing in the brain network research helps the research on connectivity pattern of both normal and diseased brain. The heterogeneous computing platform basically consists of CPU, FPGA and highly parallel processors like Graphical Processing Unit (GPU). This leads to combining the advantages of all these Units. The advantages of each such type would include power efficiency and space ratio performance.

The heterogeneous computation helps in brain network analysis in two situations. The first being at the Hospital end where the PCs (made up of FPGA and GPUs) promptly does the brain network analysis and give diagnostic suggestions. The second consists of research institutes where brain network is analyzed for several subjects.

The brain network analysis consists of three tasks: 1) Network Construction 2) All –pairs shortest path 3) network modularity.

In network construction takes place by acquiring data from functional Magnetic Resonance imaging (fMRI). This helps to build the voxel-based brain network. Thus these voxel pair requires parallel computation. For such computations GPUs are efficient. The shortest path computations can be resourcefully implemented using FPGA.

Thus in reconfigurable computing the heterogonous computing is becoming a new trend for applications where faster and parallel processing is required.

Conclusion:

In this paper we have introduced different trends in reconfigurable computing such as context switching configurations, partial reconfigurations. It also includes Heterogeneous Hardware computing, implementing C-programming on FPGA based systems. These trends tend to reduce the disadvantages posed by traditional reconfigurable computing.

These trends facilitate the advancement in technologies in different streams of science such as medicine, space-technology, embedded systems etc.

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