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Simulation and Verification of FPGA based Digital Modulators using MATLAB

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Abstract - Digital Modulators (i.e. BASK, BFSK, BPSK) which are implemented on FPGA are simulated and verified in this paper. By use of MATLAB software tools, the digital modulator designs are simulated and verified results are presented, which helps to obtain accurate design constraints. It includes minimum number of blocks required to achieve BASK,BFSK and BPSK modulation. The modulated signal obtained from simulations is verified with Modelsim by generating HDL code, before implementation on FPGA board.

Index Terms—BASK, BFSK, BPSK, Digital Modulator, HDL, Modelsim and FPGA

I. INTRODUCTION

Field programmable gate arrays (FPGAs) are semiconductor instruments which contain programmable logic elements and a hierarchical interconnects to realize any complex combinational or sequential logic functions. Today's FPGAs made up of configurable embedded static random access memories (SRAMs), high speed input/output (IO) elements high speed transceivers, network interface, and also hard embedded processors. But then again implementation of digital modulation and demodulation using FPGAs has received considerable attention. The digital communication system used to transport digital data between two or more nodes. We can achieve this in radio communication by doing a modification in physical characteristics of a sinusoidal carrier, the frequency, phase, amplitude or a combination.

In real world scenario radio communication can be achieved by placing a modulator at the transmitting end to impose the physical change to the carrier and a demodulator is placed at the receiving end to capture the changes in signal and detect the result of modulator on reception end.

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This is well known that digital modulation is less complex than analog one and very efficient for those system which is used in long distance transmission. It is also very efficient in noise correction/detection.

In modern communication system it has very important place. Purchasing a devices that is real network and tools which is required to build or deploy a complete system for establishing a simple or complex communication network. Notwithstanding this, it is not esay task to test a system without the real equipment viz computers, oscilloscope, switches, routers and also software required for system. To address this issue to deploy many researchers and software engineers introduced different network simulation tools that can help in designing the complete network system.

This work compares the methods and performance of digital modulation scheme and also presents the MATLAB environments which is a combination of high-level modeling environments. MATLAB provides the easy steps to generate HDL code automatically with the help of HDL coder which is a built-in tool of the MATLAB. Code generation is necessary for hardware/software co-design which present the simulation to synthesize the result of digital modulation schemes using the MATLAB program and its implementation in a FPGA Spartan-III kit using Xilinx ISE tool. In this paper three specific digital design of digital modulator scheme is analyzed and have create the simulation model of modulators for mapping the design on FPGA board. The output shows that in the designing of digital modulators minimum no of digital block is used. We have also analysed that design time, complexity and cost of the system is also reduced.

II. THEORY OF DIGITAL MODULATION

Same as analog modulation, there are basic three features is also availebel in digital modulators which can be modulated on carrier signal by the digital information. They are

(a) Amplitude-Shift Keying (ASK),
(b) Frequency-Shift Keying (FSK) and
(c) Phase-Shift Keying (PSK).

BASK can be obtained by the alteration of the amplitude of the carrier wave. This modulation has very poor bandwidth efficiency. The basic merit of this technique is its simple implementations, but is highly prone to noise.

BFSK is the procedure/technique where two different signals are presented by two different frequencies. It can be wide or narrow band digital modulation technique based upon the space between the carrier frequencies.

BPSK is obtained by the alteration of the phase of carrier wave with reference to the modulating signal. The digital modulation technique can be said to be the simplest form of phase modulation and is known as binary because the carrier phase represents only two phase states. This modulation technique is generally used for high speed data transfer application. This modulation technique gives a 3 dB pwer advantages compared to the BASK modulation technique and it is robust in nature and simple implementation technique.

III. DESIGN METHODS

The steps for designing of digital modulator on FPGA board are shown in fig. 1.

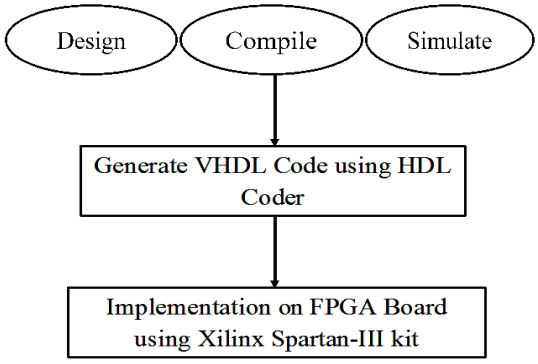

Fig. 1 Design Model of Digital Modulator

The design was first simulated using MATLAB, but this result is not directly implemented on FPGA board. In order to implement this on FPGA board VHDL code is converted using HDL coder.

IV. DESIGN OF SIMULATION TECHNIQUE

MATLAB R2013 was used for simulation, verification and for validation deployment on Hardware (Xilinx Spartan 3 FPGA). MATLAB is a new software tool of fourth-generation which is high-level programming language provides interactive or virtual environment for numerical/mathematical computation and visualization of design.

For implementing the MATLAB code on hardware board we use the syntax which supports HDL code generation. For the HDL code generation two files are needed:

(a) A function of the code that we want to convert in HDL code.
(b) A test script that calls that MATLAB function.

These are the few steps for writing a MATLAB test script:

(a) Call the design from the testbench function.
(b) Exercise the design thoroughly-This is indeed a important point while converting floating point to fixed point , where HDL Coder determines the ranges of the variableswhich are used in the design algorithm based on the values the testbench assigns to the variables.
(c) In testbench we will simulate the design before generating the code in order to ensure that there is no simulation error also we will ensure that all the required files are on the path.

The HDL coder is a built in MATLAB tool which helps in automate the steps and give way from MATLAB to hardware. The key steps in the left column of HDL coder of HDL workflow advisor which is shown in fig. 2.

I. Fixed-Point Conversion
II. HDL Code Generation
III. HDL Verification
IV. HDL code Synthesis and Analysis

A. HDL Code Generation

HDL coder provide the VHDL/Verilog code in the HDL workflow advisor which is opened after creating the project folder. In this process MATLAB code automatically converts from floating point to fixed point and provide synthesizable code for the design.

In the first step of HDL code generation, New Project in Matlab file was created and then option was selected from type of code generation. Data, settings,

and references of other files which is used by the project commonly store in PRJ files. PRJ files can be open.

In the second step, after creating the project file, the two files viz. Matlab function and Matlab Testbench file was added in entry points of code generation.

In the third step, the HDL Workflow Advisor in HDL Coder automatically converts MATLAB code from floating-point to fixed-point and generates synthesizable VHDL code.

After successful simulation of all steps in HDL workflow advisor the .vhd file can be seen from code generation file. The two files was created first one is .vhd file from where code is seen and second one was HTML report that contains HDL code and a table of generated HDL files as shown in fig. 2.

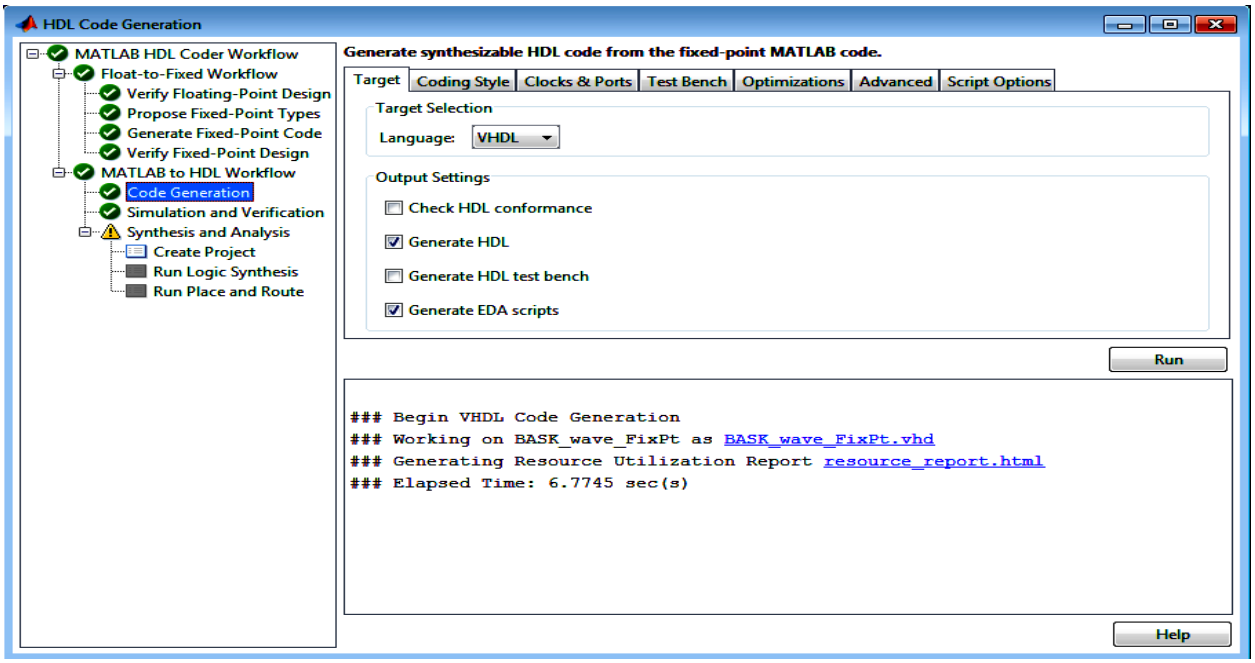

Fig. 2 VHDL and HTML file generation for Digital Modulator Model

Table 1 DUT Report File

BASK Project Status (06/08/2015 - 13:46:23)			
Project File:	bask_WAVE.xise	**Parser Errors:**	No Errors
Module Name:	BASK_wave_FixPt	**Implementation State:**	Programming File Generated
Target Device:	xc3s200-4tq144	**• Errors:**	No Errors
Product Version:	ISE 14.1	**• Warnings:**	5 Warnings (5 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	29	3,840	1%	
Number of occupied Slices	15	1,920	1%	
Number of Slices containing only related logic	15	15	100%	
Number of Slices containing unrelated logic	0	15	0%	
Total Number of 4 input LUTs	29	3,840	1%	
Number of bonded IOBs	59	97	60%	
Average Fanout of Non-Clock Nets	1.22			

Modelsim is verification software with the help of which simulated result of Digital Modulators is co-verified before implementation on board and the simulation and co-verified result of design should be same. If there is any error between results, then correct design is not implemented on FPGA board.

V. IMPLEMENTATION METHOD

Spartan-3E generation FPGAs was customized by loading configuration data/ setup information into strong, reprogrammable, static CMOS configuration latches (CCLs) which aggregately control all functional components and routing resources. The FPGA's configuration data is put away remotely in a PROM or some other non-volatile medium, either on or off the board. The Spartan-3 platform contains its own internal SPI flash configuration memory. When we apply power, the configuration data was composed to the the FPGA board using boundary scan method.

During implementation of project on hardware file is generated, which includes device utilization report as shown in table 1.

Before implementation on FPGA board a final layout of the project is generated in which ucf file , dut file is generated. After virtual implementation, second IC of project is generated. And design code have to by-pass in main IC from second IC as shown in Fig. 3.

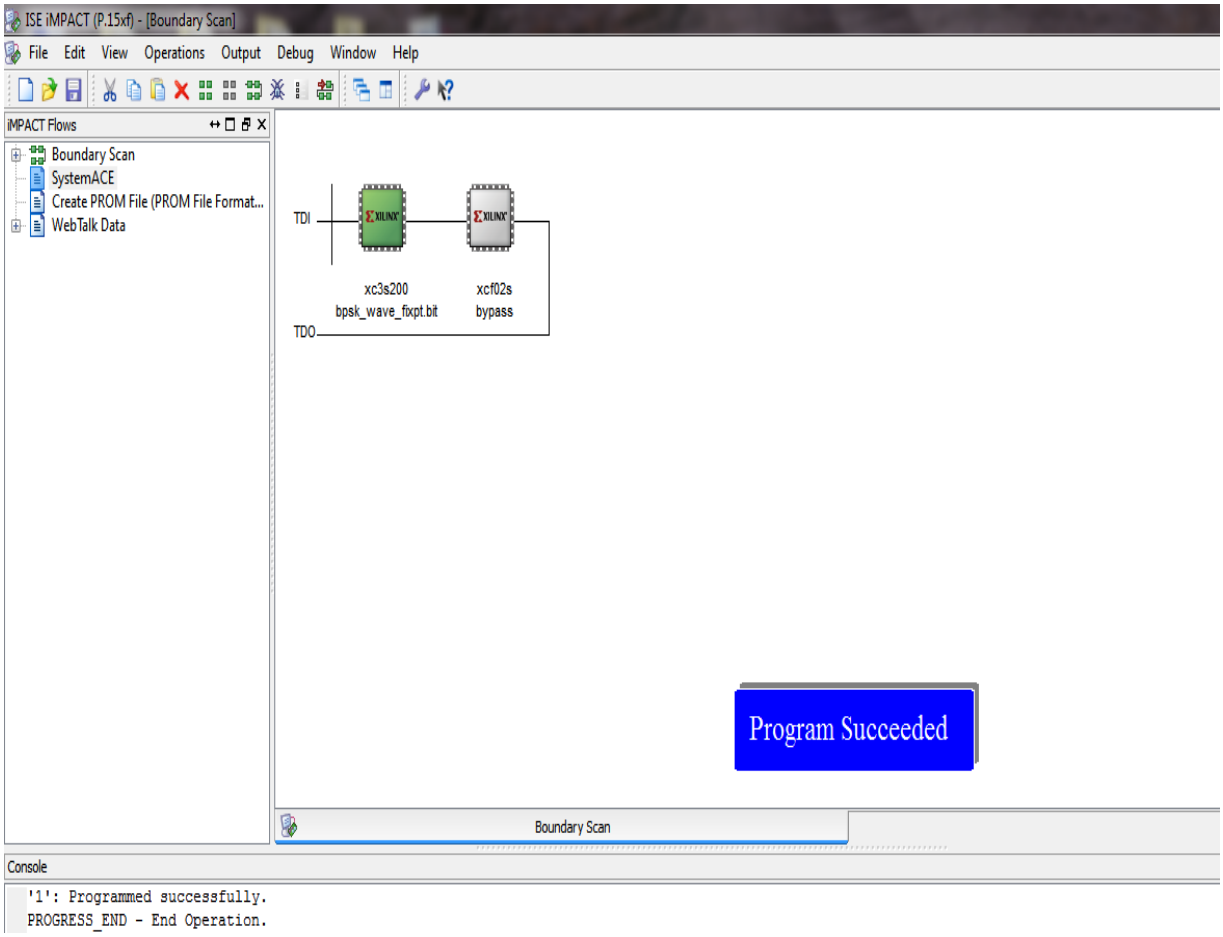

Fig. 3 Implementation of Design using Boundary scan method

For hardware implementation we have to Connect the Xilinx board laptop or computer using USB cable which attached with board as shown in fig. 4.

Fig. 4 Spartan kit

VI. RESULTS AND DISCUSSION

A. BASK simulation result

For generating the modulating signal of BASK the value of carrier frequency was 1000 Hz and Modulating frequency was 500 Hz. Simulation result of BASK modulator shown in fig. 5.

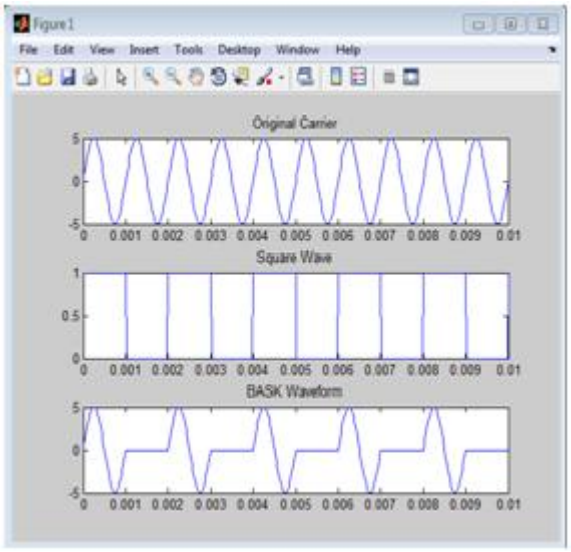

Fig. 5 BASK Result

B. BFSK simulation result

For generating the modulating signal of BFSK the value of first carrier frequency was 1000 Hz, second carrier frequency was 2000 Hz and Modulating Frequency was 125 Hz. Simulation result of BFSK modulator shown in fig. 6.

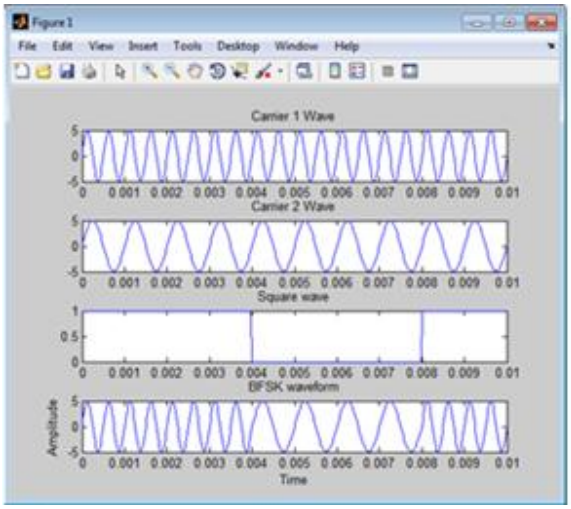

Fig. 6 BFSK Result

C. BPSK simulation result

For generating the modulating signal of BPSK the value of carrier frequency was 1000 Hz and Modulating Frequency was 250 Hz. Simulation result of BPSK modulator shown in fig. 7.

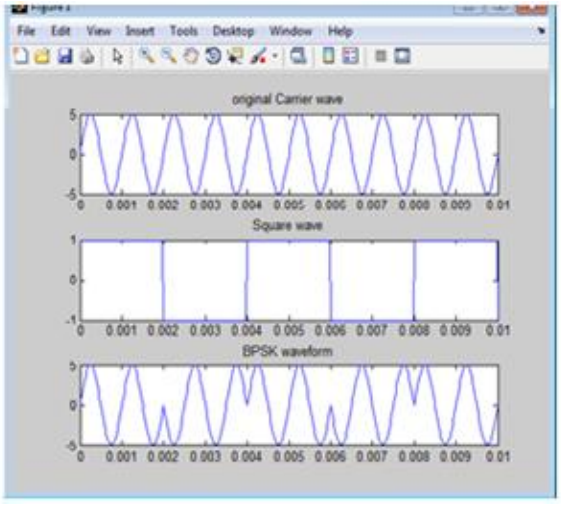

Fig. 7 BPSK Result

VII. CONCLUSION

We design Digital Modulators and observed their simulated result successfully. The design of Digital Modulators is established in MATLAB environment. Later design is implemented on Xilinx Spartan FPGA board by converting

MATLAB module in VHDL code. We get the VHDL code by the help HDL coder, which has built in tool in MATLAB software. Before implementation on board, simulated result of Digital Modulators is co-verified by Modelsim software. We observed that simulated and co-verified result of Digital Modulators were same. In this design we have used minimum no of digital blocks which are necessary in designing part.

Our future scope is to design Composit model of Digital Modulators in which all the basic modulators are present to reduce design timing, which canbe used by different communication systems. Because of this the cost will be reduced and also efforts will be reduced.

VIII. ACKNOWLEDGMENT

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