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A Novel Approach for Area Optimization in Han-Carlson Adder Using Gate Diffusion Input (GDI) Technique

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***Abstract*—Parallel prefix adders (PPA) are important and common in VLSI designs. There are more number of PPA's . Among these PPA's Han-Carlson Adder is a combination of KSA and BKA and which gives good performance according to area, propagation delay and power consumption. This paper introduces a new technique implemented using two transistors which is Gate Diffusion Input (GDI). This technique is applied to Han-Carlson adder. The goal of this paper is to reduce the area of adder by reducing the transistor count. Transistor count comparison with Han-Carlson and GDI based Han-Carlson adder is presented. This adder is implemented using Pyxis Schematic Editor (Mentor Graphics) 130nm technology. Simulation results are reported and measurement of power and delay is presented. Finally observed that the transistor count is heavily reduced hence area reduced.**

***Index Terms*—Han-Carlson adder, Parallel prefix adder, Gate Diffusion Input(GDI), power, area.**

I. INTRODUCTION

Addition is an important part of any computer architecture, since it is major component of an ALU. The speed and power performance are improved in FPGAs in practical applications as compared to processors and DSP's based applications [2].

Amongst the various parallel prefix adders, the Han-Carlson adder represents combination of Brent-Kung and Kogge-Stone adders. This adder is applicable to large word size at low complexity. This paper explores a modification of Han-Carlson adder with less number of transistors. This adder is implemented with two types of cells black cell (BC) and gray cell (GC). These black cell and gray cells are implemented using AND gate and OR gate. For the design of fast, low power circuits Gate diffusion input (GDI) is a technique more suitable to reduce the number of transistors than traditional CMOS and existing PTL techniques[3]. The aim of this work is to reduce the number of transistors than traditional CMOS design style.

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II LITERATURE SURVEY

In parallel prefix adders delay is logarithmically proportional to the length of input bits that is adder width so it gives better delay performance [2].

PPA's basically have 3 stages

- Pre computation
- Prefix stage
- Final computation

A. Pre computation

In this stage propagate and generate bits are calculated for every given input bits.

B. Prefix stage

Group generate/propagate signals are calculated in this stage for given inputs. Two operators are used in this stage they are black cell and gray cell. There logic definitions are shown below figure.

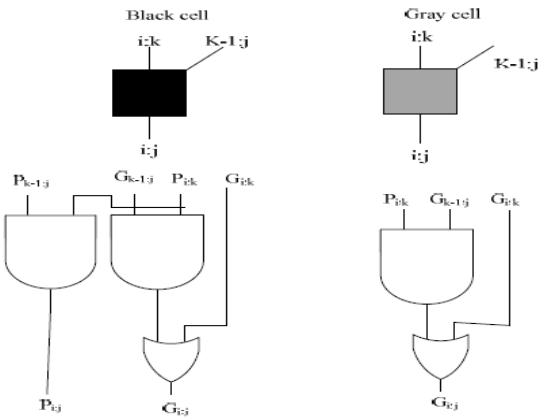

Fig 1. Black and Gray Cell logic Definitions

C. Final computation

The sum and carryout are calculated which is the final Output in this last stage

Classification of PPA's

- Kogge-Stone adder (KSA)
- Brent-Kung adder (BKA)
- Sparse Kogge Stone adder (SKA)
- Spanning Tree adder (STA)

Black cells, gray cells and full adder blocks are used in 16-bit SKA. This adder terminate with 4-bit RCA and calculate

the carries using the BC's and GC's. Totally it uses 16 full adders.

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With small modification in SKA according to interconnection between the cells gives STA adder.

KSA is another of prefix adder that use the less number of logic levels. The Kogge-stone adder is implemented with BC's and GC's only. The KSA of 16-bit designed with 36 BC's and 15 GC's and operates on generate and propagate blocks. Hence the delay is less as compared to the SKA and STA.

The last carry tree is BKA which uses BC's and GC's but less than the KSA hence it occupies less area then KSA[2]. Han-Carlson adder is introduced to reduce the area and number of stages which is shown below figure.

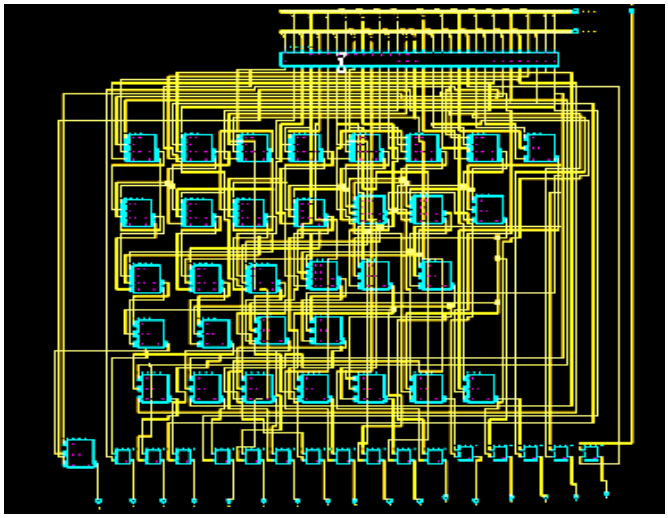

Fig 2 schematic of a 16-bit Han-Carlson adder.

It is observed from Fig. 2 that the number of prefix stages for the Han-Carlson adder is five, which is one more than the Kogge-Stone adder (log216=4) for the same wordsize[1]. However, the number of the prefix operations is less in the Han-Carlson design (32) than in the Kogge-Stone design (49). Thus, the Han-Carlson adder reduces the area in return for one extra stage of delay as compared to the Kogge-Stone adder and increase in the number of the prefix operations, the routing requirement increases and this represents a hurdle when designing adders of very large word sizes, where the routing demand may lead to very long wires and buffer requirements.

The results of Han-carlson adder are shown below figure 3.

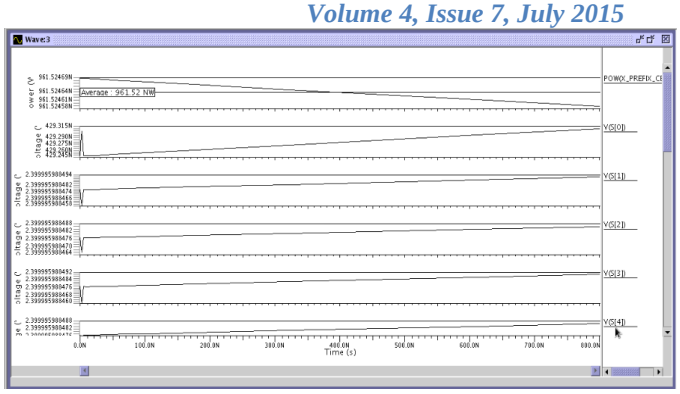

Fig 3(a)

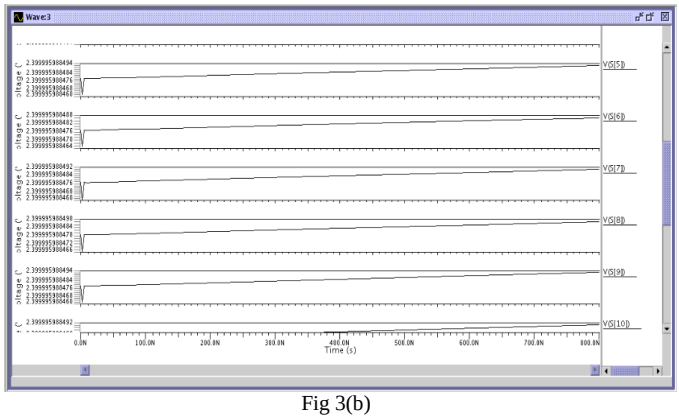

Fig 3(b)

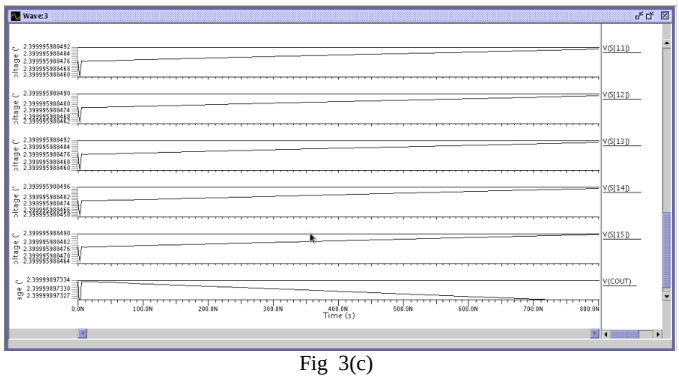

Fig 3(c)

Fig 3 output of normal Han-Carlson adder

III GATE DIFFUSION INPUT TECHNIQUE

To maintain the low complexity, reduced power consumption and less propagation delay the new technique is GDI as compared to traditional CMOS design [3].

The GDI technique [5] can be implemented using twin-well CMOS technology. The Fig. 5 shows the GDI cell which is well suited with standard CMOS process [5]. Some modifications in the standard CMOS inverter gives the basic GDI cell, where the sources of NMOS and PMOS are driven by input signals.

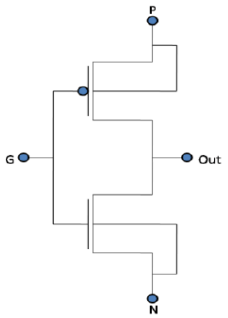

Fig 4. originally proposed

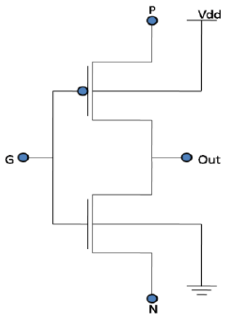

Fig 5. compatible with standard CMOS process

The well known CMOS process is twin well CMOS in VLSI designs which is used to implement the GDI cell with two transistors. To minimize the body effect the bulks of both NMOS and PMOS should be connected to the sources of constantly and respectively. Then impact of body effect is same to originally proposed GDI.

TABLE I
FOR DIFFERENT INPUT CONFIGURATIONS OF GDI CELL THESE LOGIC FUNCTIONS CAN BE FERFORMED

N	P	G	OUTPUT	FUNCTION
0	1	A	A^1	Inverter
0	B	A	A^1B	F1
B	1	A	A^1+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A^1B+AC	MUX
B^1	B	A	A^1B+B^1A	XOR

Table 1 below shows the various functions that can be implemented using basic GDI cell.

The GDI technique uses a simple and efficient algorithm. Usually it is based on the Shannon expansion. By using this Shannon expansion, this technique is possible for synthesis and realization of combinational circuits. As a result, GDI technique can be used for complex functions and also sequential circuits[4].

In PTL circuit designs problem is voltage swing degradation. There is one way for voltage swing restoration in GDI circuits under constraints of area and circuit frequency.

After every GDI cell, buffer stage should be added so that the voltage swing restoration can be achieved. Due to this, the voltage drop can be reduced. But delay, power dissipation and are increases. Hence the technique will be inefficient [5].

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VI RESULTS

The schematics of all simple GDI cells and the GDI based Han-Carlson adder are shown below.

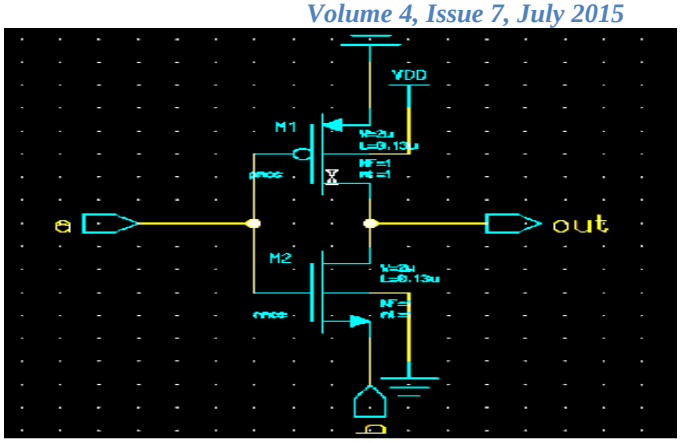

Fig 6 schematic of GDI based AND gate

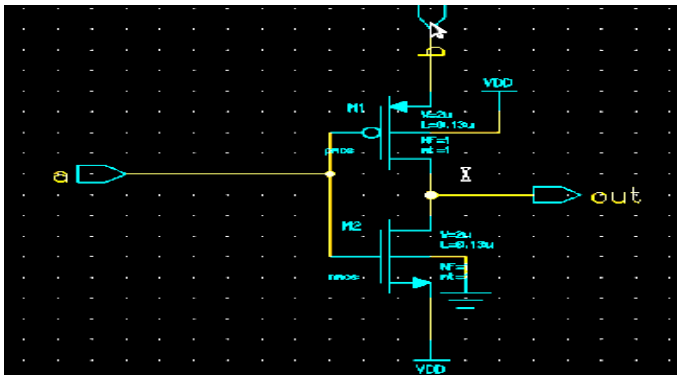

Fig 7 schematic of GDI based OR gate

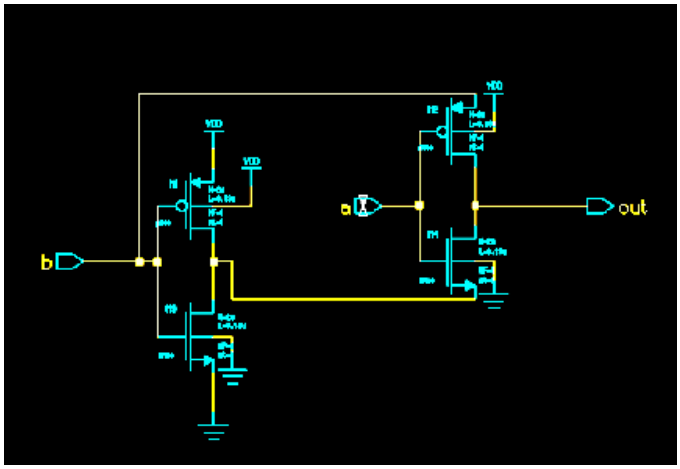

Fig 8 schematic of GDI based XOR gate

Based on GDI technique the AND gate, OR gate, XOR gate, Black cell and gray cell are implemented using pyxis schematic editor(mentor graphics) 130nm technology those are shown in fig 7,8,9,10,11. The transistor count is decreased as compared to CMOS design.

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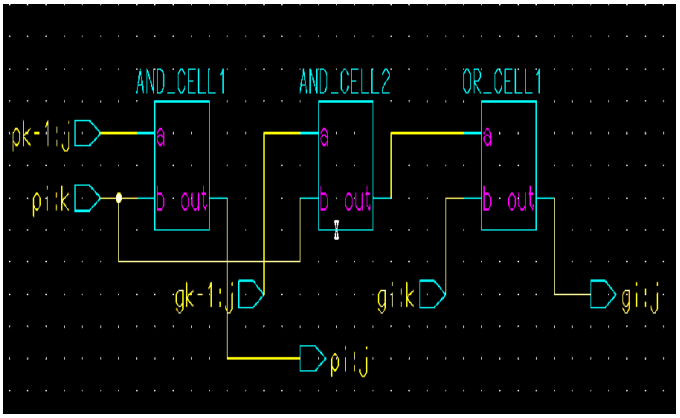

Fig 9 schematic of GDI based black cell

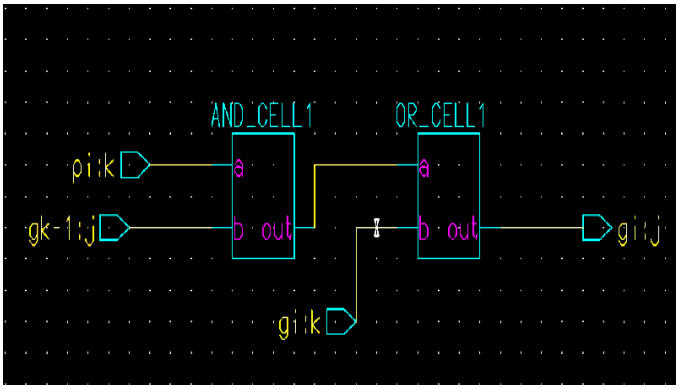

Fig 10 schematic of GDI based gray cell

The schematic of GDI based Han-Carlson adder is shown below.

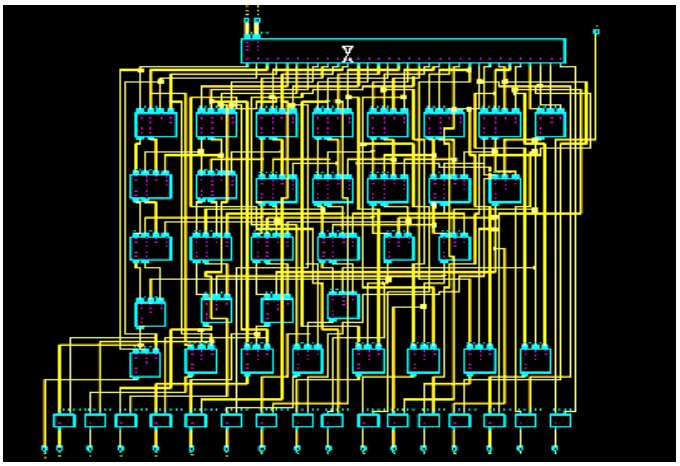

Fig 11 schematic of GDI based Han-Carlson adder

Results of GDI based Han-Carlson adder are shown in below figure

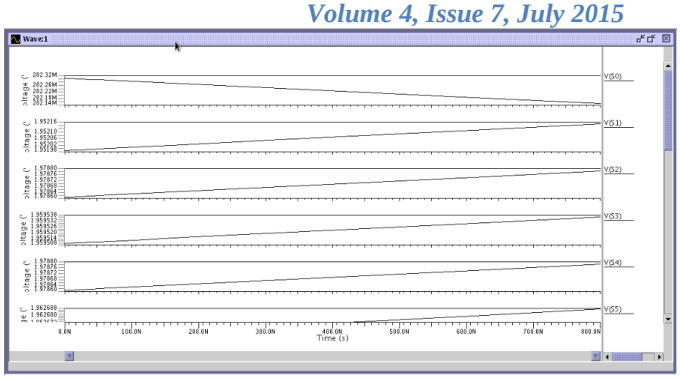

Fig 12(a)

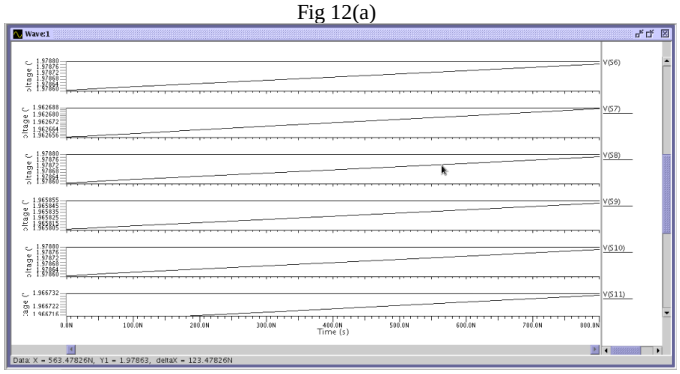

Fig 12(b)

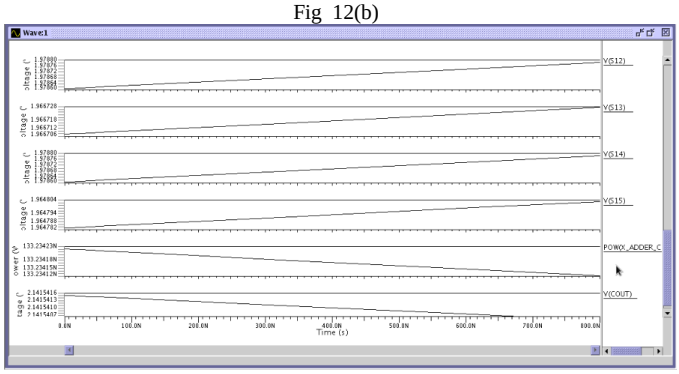

Fig 12(c)

Fig12 outputs of GDI based han-Carlson adder

From the above results observe that the voltage levels are varying and it depends on number of transitions in the input.

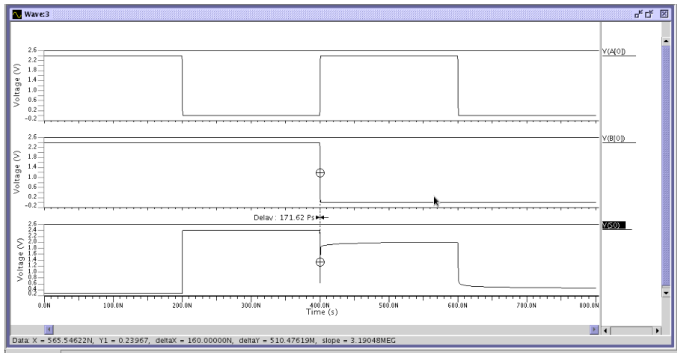

Fig 13 delay of GDI based Han-Carlson adder

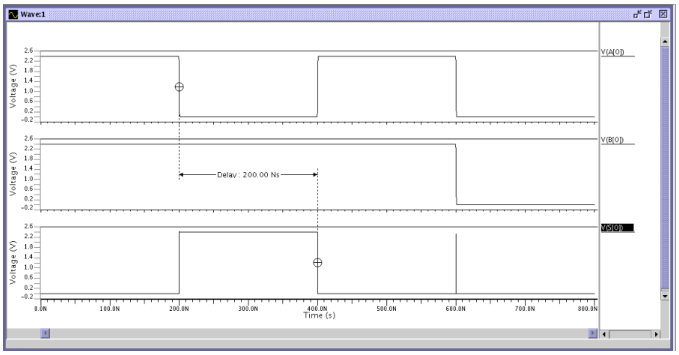

Fig 14 delay of Han-Carlson adder

TABLE 2
NUMBER OF TRANSISTOR COMPARISON FOR SIMPLE CELLS IN HAN- CARLSON ADDER

FUBCTION	CMOS DESIGN	GDI ADDER
AND	6	2
OR	6	2
BC	18	6
GC	12	4
XOR	6	4
PG(1 bit)	12	6
PG(16-bit)	192	96

Han-Carlson adder requires ,
Total num of BC =17
Total num of GC=16
Total num of xor gates=16
PG block (16-bit)= 1

TABLE 3
CALCULATION OF TOTAL NUMBER OF TRANSISTORS REQUIRED

Name of the cell	CMOS design	GDI adder
BC(17)	306	102
GC(16)	192	64
XOR(16)	96	64
PG block	192	96
TOTAL	786	326

For CMOS based Han-Carlson adder the area required=786*(W*L)
=786(2u*0.13u)
=204.36um^2
Similarly, for GDI based Han-Carlson adder the area required= 326*(W*L)
= 326(2u*0.13u)
=84.76um^2

From the above analysis observe that area required for Han-Carlson adder based on GDI occupies less area as compared to CMOS based design.

Total comparison of Han-Carlson adder according to area, power and delay is shown below table.

TABLE 4
COMPARISON OF POWER AND DELAY

Name of the adder	power	delay
Normal Han-Carlson adder	961nw	200nsec
GDI based Han-Carlson adder	133nw	171psec

V CONCLUSION

GDI based Han-Carlson adder is designed and simulation results are verified. By using the GDI technique power, delay and the transistor count required to design Han-Carlson adder are decreased as compared to CMOS design.

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