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Design of MIL-STD-1553B Bus Protocol Controller Using VHDL Simulation

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***Abstract*— The bus controller is a device which has a list of addresses of all bus users and sends a command to each one of them at a predetermined rate, giving each user the chance to access the data bus and send data required by other users. Data bus architecture scheme is used for transferring data between the devices in avionics systems. Nowadays, MIL-STD-1553B bus system is used for this purpose. This paper presents design of the MIL-STD-1553B bus protocol controller using VHDL. This paper aims at design of 1553B protocol controller with the addition of an arbitrator. It results in less complexity for accessing memory by the processor and protocol controller at the same time. This also provides memory management mechanism. The proposed system is designed using finite state machine in VHDL and simulated using ModelSim tool.**

***Index Terms*— Bus Controller (BC), MIL-STD-1553, ModelSim, Remote Terminal (RT), VHDL.**

I. INTRODUCTION

Modern military avionics systems which contain lot of devices that needs to communicate with each other for meeting their requirement for a particular application. In the earlier days, point-to-point wiring schemes are used for this purpose. But it became very complex, time consuming, bulky and affects the performance of the system very badly. So, a data bus architecture scheme is used for communicating between the devices in the avionics systems.

In the present scenario, MIL-STD-1553B bus protocol is used for sharing information between devices. MIL-STD-1553 is a serial bus which was originally developed by U.S Air force in 1973[1]. After some changes made, an improved version MIL-STD-1553A was released in 1975. Finally, it is modified to MIL-STD-1553B data bus and is used now in all avionics systems. It is a dual redundant bus, i.e., it has an alternative path in case of damage or failure. The bidirectional MIL-STD-1553 bus which connects the devices through a twisted shielded pair cable.

MIL-STD-1553B data bus uses Manchester II bi-phase encoding and decoding scheme because of its low error rate. Manchester coding has some advantages like easy error detection, high noise immunity etc. It has transition in each bit times[2].

The data bus architecture which is shown in fig. 1 explains a maximum of 32 devices can be connected to the MIL-STD-1553B data bus. Among these 32 devices, one should act as a bus controller (BC) and remaining as the remote terminal devices (RT). Bus controller is the only one device which can initiate all the communication through the 1553 bus system[6].

Most significant problem behind the existing bus protocol is the memory accessing. There may arise conflicts while accessing memory by both protocol controller and processor. To overcome this, the proposed system is designed with an arbitrator.

This paper aims to design a bus protocol controller for MIL-STD-1553B data bus. The 1553 bus controller is known as the *'heart of the system'* since it controls all the activities in the bus. The proposed system describes the 1553B bus protocol controller with an arbitrator, memory management mechanism and a protocol controller.

II. MIL-STD-1553 OVERVIEW

A. 1553 Bus Architecture

The MIL-STD-1553B is a military standard which runs on a single twisted shielded pair of wires. It has a dual-redundant architecture and extremely low error rate of one word fault per 10 million words make MIL-STD-1553 a highly reliable bus. Only a single computer is allowed to transmit on the bus at a given time. A 1553 bus system architecture is shown in fig. 1 below. The device that controls all the communication on the bus and acts as the master is called Bus Controller (BC) [1]. The BC can control multiple slave computers which are called Remote Terminals (RT) by sending commands to them.

There may also be one or more passive Bus Monitors (BM) deployed on the bus which are only used to monitor or record the messages on the bus but can't transmit any messages. As shown in fig. 1, a maximum of thirty one remote terminals can be connected to the bus in addition to the bus controller [2]. It consists of multiple computers having a master/slave relationship. Only the bus controller can initiate a transmission on the bus. The RT receives and decodes commands from the bus controller and responds accordingly within the strictly defined time of 12 microseconds.

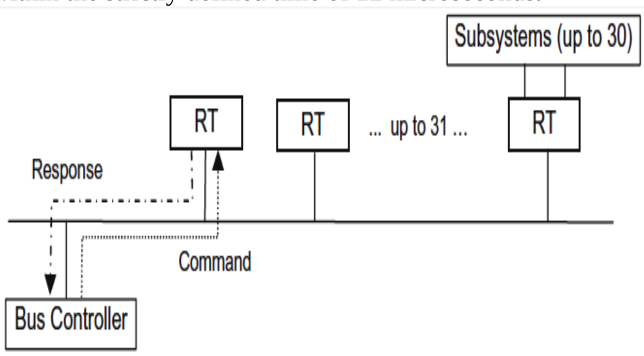

Fig. 1 MIL-STD-1553B data bus architecture

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An RT only performs transmission or reception of data when instructed to do so by the BC.

The BC is responsible for directing communications over the data bus. Although several of the systems connected to the bus may have the ability to perform the role of BC. Only one BC is allowed to active at any given time and that only may issue commands over the data bus[2]. These commands may be related to the management of the bus or may be oriented toward data communication to and from subsystems.

B. 1553 Word Formats

There are three different words that form the messages that are transmitted on the bus; command word (CW), data word (DW) and status word (SW) [3]. Each word is formed by a three-bit time sync, sixteen bits for the information field itself, and a parity bit at the end, which makes a total of twenty bits [5]. Fig. 2 shows an illustration of the three word formats.

Each bit is timed as one microsecond, resulting in one megabit per second transmission rate for the bus. The communications between two elements in the data bus system, the bus controller and the remote terminal is allowed only through information transfer formats of 1553B bus which is shown in fig. 3. In 1553, the bus controller controls all communication and it is the sole device allowed to transmit command words. Notice that all messages are initiated by the bus controller using command word.

The actual information that is to be transferred through the 1553 bus is contained within the data word of a message [4]. It is transmitted by the bus controller after it sends a receive command or by the remote terminals after they receive a transmit command. The sixteen bits of payload of the data word is application specific and is defined by the interface designers. The standard only requires that the most significant bit (MSB) of the data must be transmitted first. The status of the remote terminal to the bus controller is indicated in the status word.

Remote terminals must send a status word as the first word of a response to a valid message from bus controller. The only time when a status word is suppressed is when the optional broadcast operation is performed .

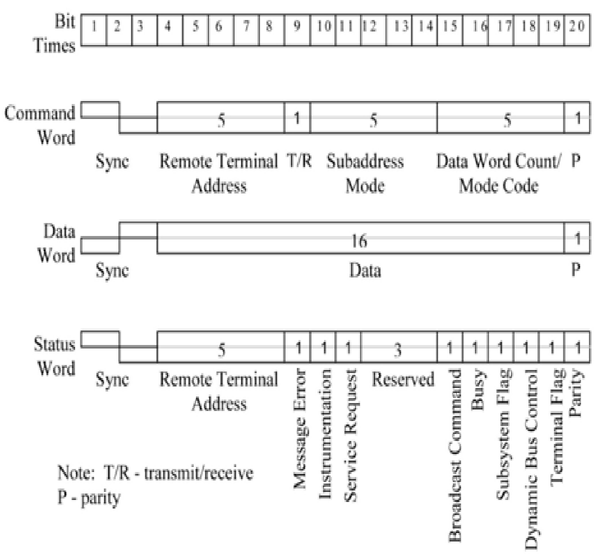

Fig. 2 1553 Word formats [5]

C. 1553 Message Formats

MIL-STD-1553 has a proven history of providing extremely robust performance at 1 Mbps. The primary purpose of the 1553 data bus is to provide a common media for the exchange of data between systems. All control messages originate with the active bus controller and are received by a single receiver or by multiple receivers (broadcast). A command word with a terminal address value of 31 (11111) indicates a broadcast message, while any other terminal addresses are to identify unique messages to a terminal on the bus. The exchange of data is based on message transmissions. A single message is the transmission of a command word, a status word, and a data word if they are specified.

Sole control of information transmission on the bus shall reside with the bus controller, which shall initiate all transmissions. The 1553 standard defines different types of information/message transmission formats [3]. All of these formats are based on the three word types just defined. Here we consider three important information formats which are shown in fig. 3. This information transfer formats are based on the command/response philosophy in that all error free transmissions received by a remote terminal are followed by the transmission of a status word from the terminal to the bus controller.

The bus controller to remote terminal (BC-RT) message is referred to as the receive command since the remote terminal is going to receive data [9]. The bus controller outputs a command word to the terminal defining the subaddress of the data and the number of data words it is sending. The remote terminal upon validating the command word and all of the data words issues its status word within the response time requirements which is maximum of 12μs.

The remote terminal to bus controller (RT-BC) message is referred to as a transmit command. The bus controller issues only a transmit command word to the remote terminal[9]. The terminal, on validating the command word, transmits its status word followed by the number of data words requested by the command word.

The remote terminal to remote terminal (RT-RT) command allows a terminal (the data source) to transfer data directly to another terminal (the data sink) without going through the bus controller. However, the bus controller may also collect the data and use them. (This is sometimes called a RT-RT-M command, since the Bus Controller monitors the data). The bus controller issues a command word to the receiving terminal immediately followed by a command word to the transmitting terminal [9]. Here, the message shall include the two command words, the two status words, and the data words.

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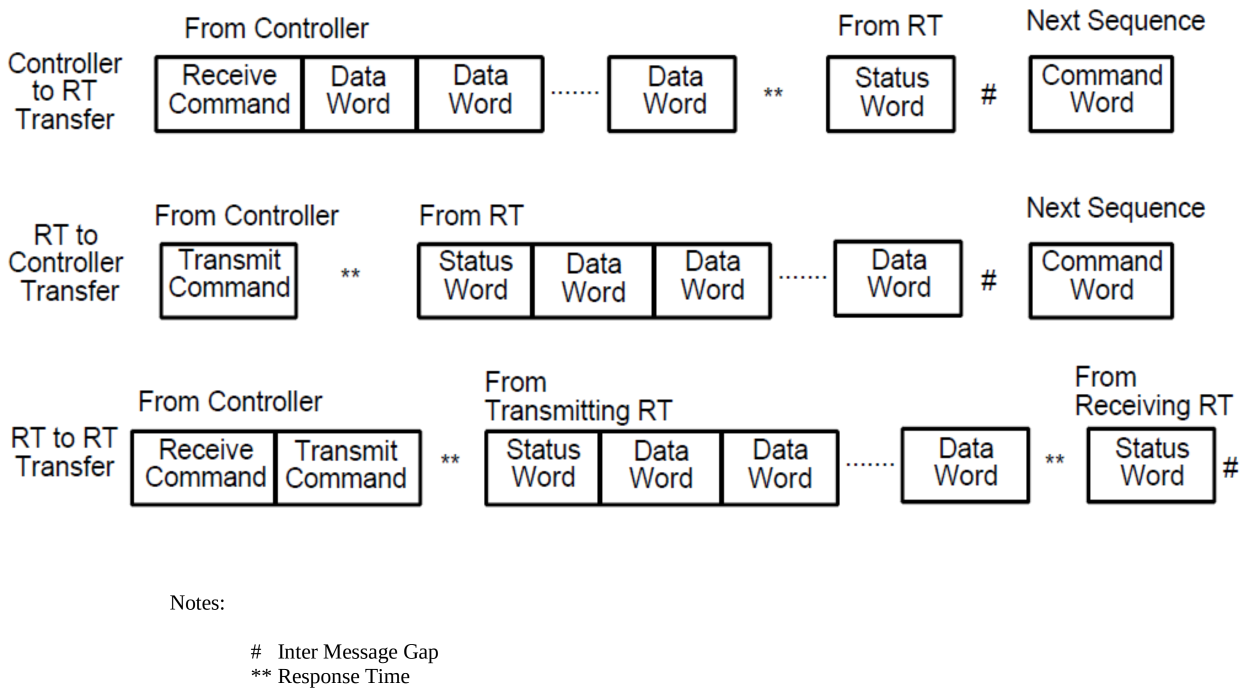

Fig. 3 1553 Information transfer formats

III. DESIGN

A 1553B bus system is composed of a bus controller and one or more remote terminals, connected by the 1553B serial data bus. Bus management is accomplished via a strict master-slave relationship between the BC and RTs. To provide multiple data paths for redundancy, a mission-critical system typically utilizes several 1553B buses. All bus transmissions are accessible to all units connected to the bus, but only one unit can "speak" at a time. The BC initiates all bus transfers by sending a command word to individual RTs, and each RT is required to respond with a status message acknowledging receipt of an error free BC's message. The entire control of the bus system is incorporated in the bus controller. Thus the bus controller is said to be the heart of the system.

Fig. 4 shows the overall block schematic representation of proposed 1553B bus controller system. The bus controller is placed in between the processor and the 1553 serial data bus. The entire block of the bus controller is incorporated with several other blocks such as Manchester encoder, Manchester decoder, arbitrator, block of memory, processor interface logic, protocol controller logic. All these blocks are designed as block by block basis using finite state machine in VHDL.

B. Bus Controller Design

Manchester II bi-phase encoding scheme is used by this MIL-STD-1553B Bus system. Manchester encoding provides a self-clocking waveform, that is, the clock is embedded in the data. So at the receiver side the clock can be recovered very easily. Manchester encoding encodes a "zero" with a low-to-high transition and a "one" with a high-to-low transition. It is easy to detect errors in Manchester encoding since there exists a transition at each bit times [6].

Manchester encoder requires a single clock with a frequency twice the desired data rate applied at the input of encoder. Manchester decoder requires a single clock with a frequency of 12 times the desired data rate applied at the decoder input. Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. Manchester encoded data bits coming from the 1553 bus is decoded and converted back to normal bits by using the decoder.

The bi-phase Manchester II encoder encodes the sixteen bits information fields of words. A logic "1" is represented by a 0.5 µs high to a 0.5 µs low transition, and a logic "0" is represented by the opposite low to high transition [9]. As shown in figure 2, each word is preceded by a three-bit sync which is encoded as 1.5 µs low and 1.5 µs high for data words and opposite 1.5 µs high and 1.5 µs low for command and status words. The command word can be transmitted only by the bus controller and as its name implies it contains a command to the remote terminals which indicates either to transmit or receive the data words.

Parallel to serial converter is used for converting the parallel data coming from the protocol control logic to serial data since the 1553 bus is a serial bus. Memory access for both protocol controller logic and processor is done through an arbitrator. The arbitrator which is also known as a mediator that helps to give access to the memory without any conflicts between processor and protocol controller logic.

A processor interface logic which is designed by using the finite state machine in VHDL. With the help of this processor interface logic, processor can also do its actions in parallel when it is used by the 1553 data bus. Processor need not wait for the completion of data transmission in 1553 bus. A 1kilobyte 16 bit RAM is also used to program the message transmission through the data bus.

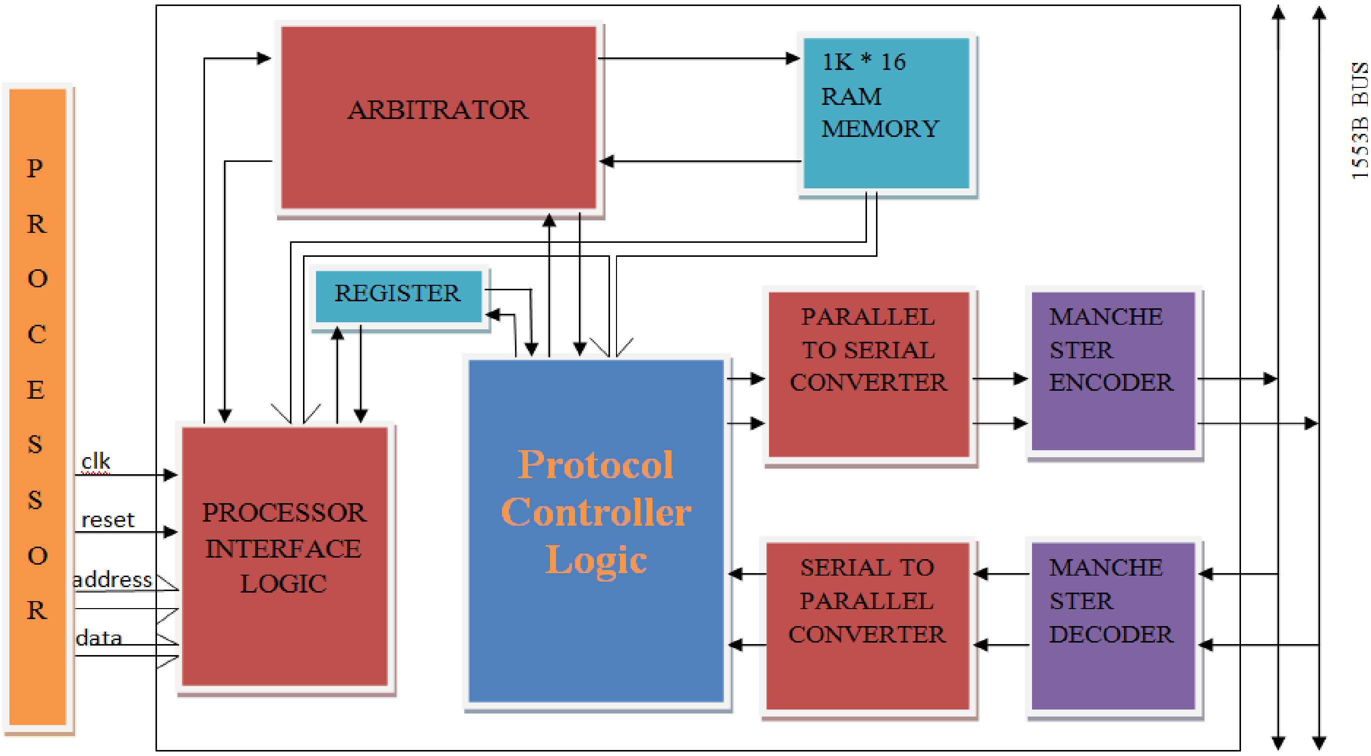

Fig. 4 1553B Bus protocol controller

The main block of this 1553 bus system is the protocol controller logic. It controls all the bus transmission through the 1553B data bus. In this work, the protocol controller logic is designed using finite state machine in VHDL which is shown in fig. 5.

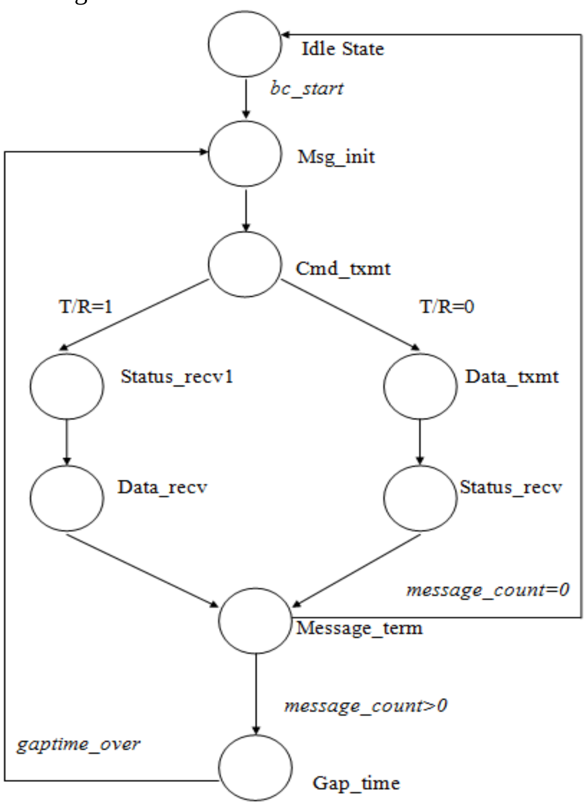

Fig. 5 State diagram of protocol controller

When the *bc_start* signal is active, the protocol controller starts sending messages. Initially bus controller transmits the command word (CW). If the Transmit/Receive (T/R) signal is '1' which indicates the BC which tells to the RT to transmit the data words. Upon receiving this command word, RT sends the status word (SW) followed by specified data words. If the Transmit/Receive (T/R) signal is '0' which indicates the BC which tells to the RT to receive the data words (DWs). Upon receiving the command word and data words from the BC, RT send the status word which indicates an error free reception.

B. Design of Memory block

The BC may be programmed to transmit multimessage frames. A single data transfer can transmit up to 32 messages. Each message may contain maximum of 34 words (32 data words, 1 command word, 1 status word) and a minimum of 3 words (1 data word, 1 command word, 1 status word). The number of messages to be processed is programmable by means of the fixed message count location in the shared RAM. Memory block in the proposed system describes a stack area of shared RAM to store the message details. Stack area maintains the details of every message that are transmitted through the bus. Each message resides in a designated message block area of the shared RAM. Stack pointer points to the block status address of every message. In the memory block, the value of stack pointer is incremented by three and value of the message counter is decremented by one at the end of each message processed.

IV. RESULTS

The designed state machine has been simulated using ModelSim and obtained waveform is shown in fig. 6 below.

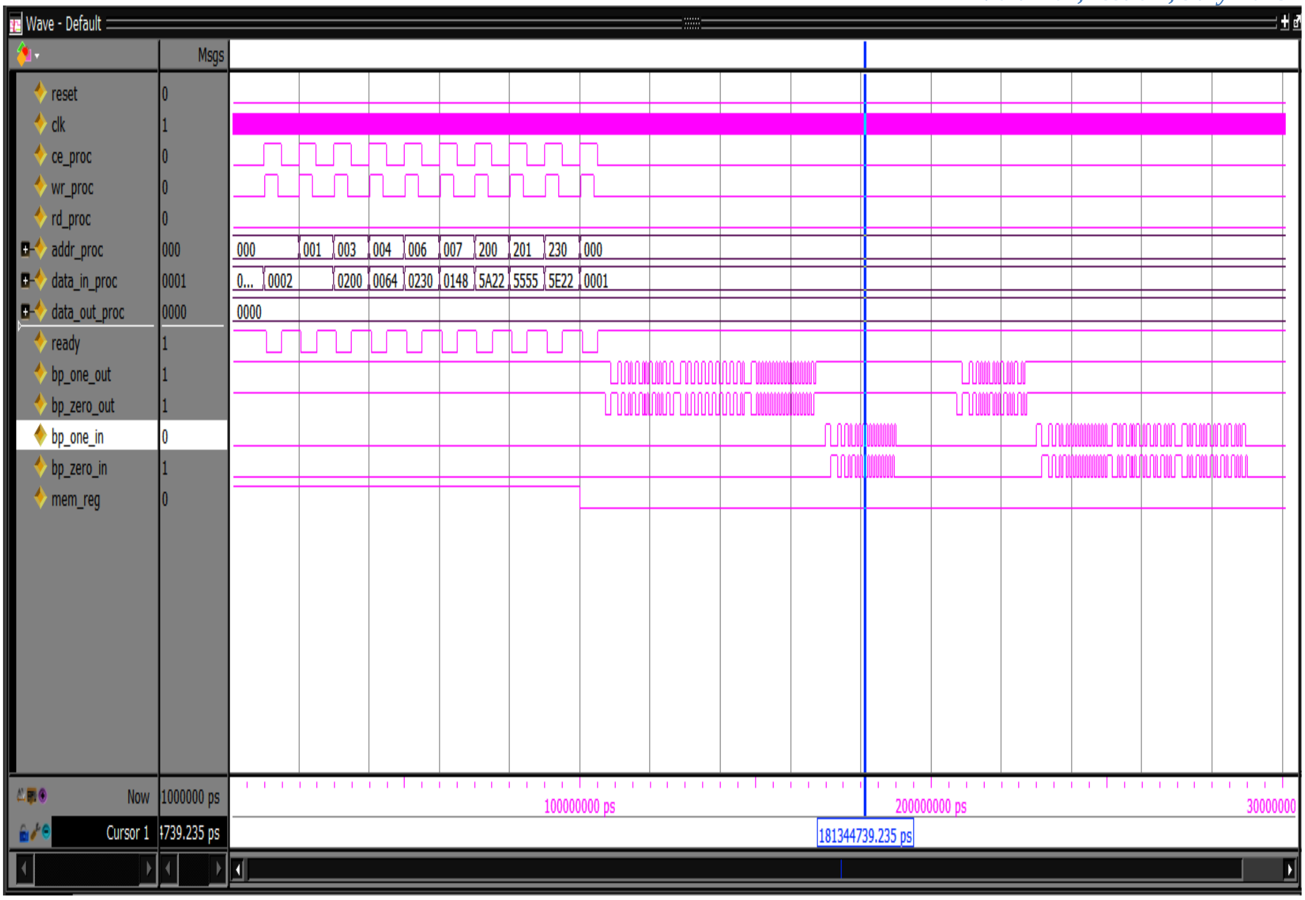

Fig. 6 Simulated waveform of 1553B bus controller

A finite state machine which designed the enhanced throughput message activity in a 1553B based bus controller have been presented. The proposed system works as a bus controller which controls the data transfer through the bus. For BC to RT transfer a command word followed by data word is send by the BC. Upon receiving this, RT sends SW indicating an error free reception. The RT to BC transfer includes a command word which is send by the BC and upon receiving this CW, RT sends status word followed by the data word.

V. CONCLUSION & FUTURE WORKS

This paper describes a MIL-STD-1553B serial data bus interface and the bus protocol controller VHDL simulation. The 1553B bus protocol controller which helps in controlling the data transmission through the bus. In the proposed system, 1553B bus controller is modeled as a finite state machine in VHDL. With the addition of an arbitrator, memory block and protocol controller, the performance of the entire system was improved. Since all the components needed for the bus controller was integrated as a single block, its area of utilization is reduced.

For future work, it may be possible to implement the MIL-STD-1553B bus controller onto a Xilinx based FPGA platform. It is expected to improve the performance of the system to a great extent, by varying any of the parameters such as delay, speed etc of bus controller. Compared to other avionics data bus standards 1553B is known for its reliability and flexibility.

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