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Enhanced Data Encoding Scheme for NoC Applications with Reduced Latency

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***Abstract*— Interconnection system is the main reason for power dissipation in Network-On-Chip (NoC). As technology reduces, the links are also contributing major power dissipation along with routers. A technique for reducing power and latency in the links of NoC is presented in this paper. Using this technique filts get encoded and decoded at the network interfaces (NI)[1]. As the encoder logic and the decoder logic are integrated in the Network Interfaces, architecture of the routers need not be altered. In order to reduce latency for NoC Globally Pseudochronous Locally Synchronous (GPLS)[4] clocking scheme is presented. In this the clock is distributed with constant phase difference. Due to the phase difference incurred, in the NoC some paths will work at higher speed. The results convey that the power dissipated by, the links, due to coupling switching activity, as well as latency gets reduced.**

***Index Terms*— Coupling Capacitance, Data Encoding, Low Power, Network On Chip (NoC), GPLS, Latency.**

I. INTRODUCTION

As the design complexity in system-on-chip(soc) increases, the noc is taken as the effective communication structure[2]. The interconnects on the chip cores are playing major role in factors such as power, reliability, cost and performance. For the good quality of service the on-chip communication system follows advanced routing algorithms, data protection methods. These factors decide the system performance in the power and energy aspects[1]. In the intel's 80-tiles teraflops processor the communication power is significant at 28% of tile power and synchronous tile-level clock distribution accounts for 11% of the whole.

As per today's design perspectives energy consumption and power dissipation are crucial objectives. By using data encoding technique it is a feasible way to reduce the power dissipated and consumed energy by the noc links. We propose an end-to-end encoding scheme which ventures the wormhole-switching technique and is translucent to noc. Added, distinctively from the bus-invert (bi) coding and the (cdbi) coupling driven bus invert coding[4], our encoding scheme reduces the power exhausted by the link considering both the contribution of the self switching activity and of the coupling switching activity.

II. RELATED WORK

In the way to reduce power dissipation in links, several data encoding techniques have been stated earlier. Odd inversion, Odd Even bus inversion techniques (OEI), etc,. For a random data bus invert (BI), and INC-XOR methods are followed for encoding. And for the correlated data patterns the gray code, working-zone encoding, T0 encoding and T0-XOR data encoding techniques are used. But these are not suitable in deep sub-micron regions as we are concentrating at chip-level.

As our aim is to reduce coupling switching activity so that the power dissipated at the deep sub-micron level can be reduced. End-to-end encoding [21] is one of the methods that is used in wormhole switching. Based on this we try to implement a encoding scheme which helps us to reduce the power and for that scheme by adding a clocking technique (GPLS) we try to reduce the delay.

III. ENCODING SCHEME

The urged encoding Scheme involves adding even inversion with odd inversion which will make a few of Type I (T1***) transitions convert to Type II. From Table II, if flit was even inverted, the transitions designated T1** and T1*** are reformed to TypeIV and TypeIII transitions. So, we can say that the power exhausted by the links get diminished by application of even inversion. In the proposed scheme the prevailing data is correlated with the earlier one in order to decide the type of inversion i.e., if odd, even, full, or no inversion, to be done so that link power get diminished.

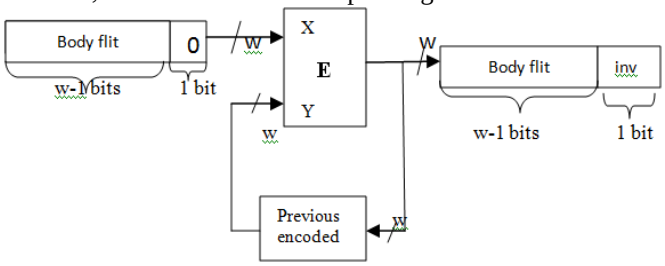

Fig 1: Encoding block diagram

TABLE I: Effect Of Even Inversion On Chance Of Transition Types

Time	Normal			Even Inverted		
	Type I			Types II, III, IV		
t- 1 t	01, 10 00,11	00, 11, 01,10 10, 01, 11,00	00, 11 01, 10	01, 10 10, 01	00, 11,01,10 00, 11,01,10	00, 11 11, 00
	T_1^*	T_1^{**}	T_1^{***}	Type II	Type IV	TypeIII
t-1 t	Type II 01, 10 10, 01			Type I 01, 10 00,11		
t-1 t	Type III 00,11 11, 00			Type I 00, 11 01, 10		
t-1 t	Type IV 00, 11, 01, 10 00, 11, 01, 10			Type I 00, 11, 01, 10 10, 01, 11, 00		

From the above table we can detect the type of transition and thus we can reduce them by applying different encoding methods. This table represents the change of transitions from one type to another when we even invert the flit i.e., when the bits in the even positions of the flits get inverted.

In the encoding process, the Ty block takes two contiguous bits of the flits inputted (e.g., X1X2Y1Y2, X2X3Y2Y3, etc.). The typeY transitions are ascertained by using the below derivation

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$$Ty = T_2 + T_1 - T_1^{***} \quad (1)$$

The type e and type 2 and type 4 transitions can be detected by using the below analysis.

The theoretical equation for dynamic power dissipation by interconnects and drivers is

$$P = [T_{0->1}(C_S + C_l) + T_c C_c] V_{dd} 2F_{ck}. \quad (2)$$

where T_(0→1) is the count of 0 to 1 transitions in the two consecutive bus transmissions, Tc is count of correlated switching among physically contiguous lines, Cs is line-substrate capacitance, Cl is load and Cc is coupling capacitances, Vdd supply voltage, and Fck clock frequency.

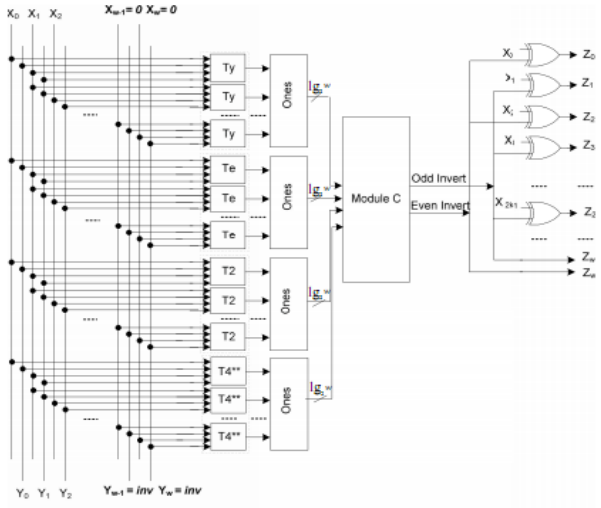

Fig 2: Encoder logic diagram for the implemented scheme.

Let P', P'' and P''' are the power exhausted by the link when flit get transported with no, odd and full inversions respectively. Akin to the analysis inured for Scheme I in [1], we can see condition P'''< P[1] as

$$T_1 + 2T_2 > T_2 + T_3 + T_4 + 2T_1^* \quad (3)$$

Defining

$$T_e = T_2 + T_1 - T_1^* \quad (4)$$

We obtain condition as P''' < P as

$$Te > ((w-1))/2$$

Similarly P''' < P' is shown as

$$T_2 + T_3 + T_4 + 2T_1^* < T_2 + T_3 + T_4 + 2T_1^{***}$$

Using above equations we can say that

$$Te > Ty$$

We obtain the condition as p''' < p'', as

$$T_2 + T_3 + T_4 + 2T_1^* < T_1 + 2T_4^{***}$$

From this we define

$$T_r = T_3 + T_4 + T_1^* \quad (5)$$

$$T_e = T_2 + T_1 - T_1^* \quad (6)$$

Assuming link width is w bits and the total transitions between neighbouring lines is w − 1, hence

$$T_e + T_r = w\text{-}1 \quad (7)$$

From the definition of Te and Tr, we can say that

$$2(T_2 - T_4^{**}) < 2T_e - w+1. \quad (8)$$

The even inversion will reduce power dissipation when the conditions P''' < P, P''' < P', and P''' < P'' get satisfied. Based on the above derivations [1] we obtain

$$T_e > ((w-1)/2), \quad T_e > T_y, \quad 2(T_2 - T_4^{**}) < 2T_e - w+1. \quad (9)$$

And full inversion will reduce power dissipation when the conditions P''' < P, P'' < P', and P'' < P''' get satisfied. Therefore, using above equations we can obtain condition for full inversion as,

$$2(T_2 - T_4^{**}) > 2T_y - w+1, (T_2 > T_4^{**}) \quad (10)$$

$$2(T_2 - T_4^{**}) > 2T_e - w+1. \quad (11)$$

Similarly, from conditions P' < P, P' < P'', and P' < P''' get satisfied the condition for odd inversion is obtained. This statement is concluded as

$$2(T_2 - T_4^{**}) < 2T_y - w+1, \quad T_y > ((w-1)/2) \quad (12)$$

$$T_e < T_y. \quad (13)$$

When none of (10), (11), or (12) is satisfied, there will be no inversion get performed. In the initial stage, the Te segments have been joined which will determine any of the transition types of T2, T1**, and T1*** get detected or not for each two bits of the inputs. For these transition types, the power of links can get reduced by even invert action. The Ones blocks will determine the number of transitions detected for each type corresponding to each Ty, Te, T2, T4** [3] blocks. These outputs are given as inputs to Module C block. This block is designed based on the conditions (10), (11), and (12). Based on the outputs of Module C "10," "01," "11," or "00,", the odd, even, full, or no invert actions are implemented respectively. The outputs "01," "11," and "10" show that whether (10), (11), and (12), respectively, are satisfied.

Now the Decoder can be designed according to the block diagram as below,

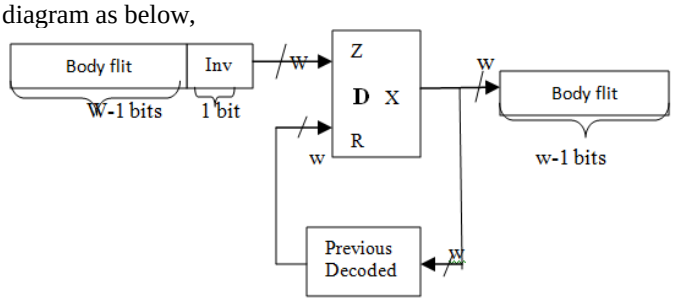

Fig 3: Decoder Block Diagram.

The decoder can be designed using basic gates [1]. Same operation is done as in the encoding but by comparing the input encoded data with previously decoded data. The logic diagram for decoder is designed as shown

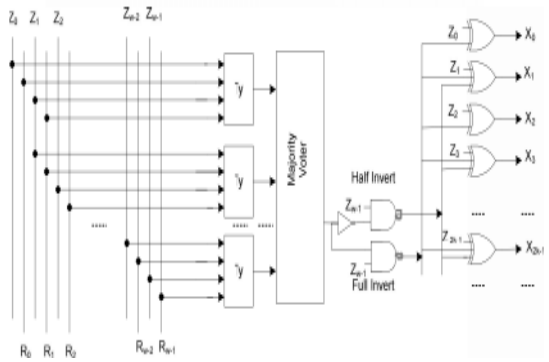

Fig 4: Decoder Circuit Diagram

The decoder contains the T_y blocks which will have the present encoded data and previously decoded data as inputs. These are given to the T_y blocks. This block outputs are given to a majority voter. The majority voter will find out the major input i.e., either '1' or '0' and produces it at the output. And

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the final decoding process is done using the simple nand and or gates.

IV. Proposed Method

The main problem today present is to disperse a clock which is skew-free and synchronous over the whole chip. Several methods have been figured out in research literature over past stating that maximum of the power is burned in distribution of clock and latches and turn up with remedies like GALS[4] (Globally Asynchronous Locally Synchronous). For Networks-on-Chip (NoC), where estimating resources are arranged in a 2-D mesh allied together over switches in an on-chip network. Another fortuity exists is Globally Pseudochronous Locally Synchronous (GPLS) clock distribution [4].

Pseudochronous is short for pseudo-synchronous which is a mesochronous clock with invariable phase difference among local clock fields. The main concept is to allot a clock with likewise frequency over the chip to each local clock region by making one region to forward clock from one to the next[4]. The disadvantage in GALS technique is the asynchronous communication between the clock regions has to be controlled with the help of handshake signals, which reduces maximum frequency and increases area overhead.

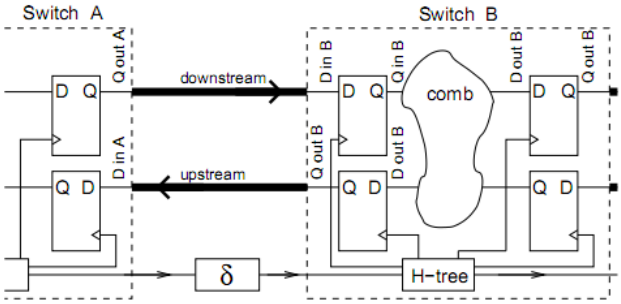

Fig 5: Block Diagram of Globally Pseudochronous Locally Synchronous Technique.

A switch will have both input and output buffers to assure internal signal stability at the time of switching, as shown in below figure5 [4]. The pseudochronous clocking avail a constant frequency but with distinct phase. By choosing the phases of switch nodes, the communication in some assured paths is built with lesser latency compared to a case if every switch had same phase.

In the proposed technique the combinational circuit in 'switch A is the encoder' and in 'switch B is the decoder'. By introducing the delay between the two switches, the phase of the encoder clock and decoder clock are made different. Delta delay has been introduced in between encoder and decoder. In the VHDL simulations, when assigning signal , they will have some infinitesimal delay, called delta delay. Delta delay has no measurable units. But a hardware designer should think that delta delay is a smallest time, in the range of femtoseconds which could be measured.

V. Results

The performance of proposed technique is designed by VHDL language and the effectiveness of the coding is analysed by using a modelsim simulator. Fig6 shows simulation output for the 8 bit data bus with random sample.

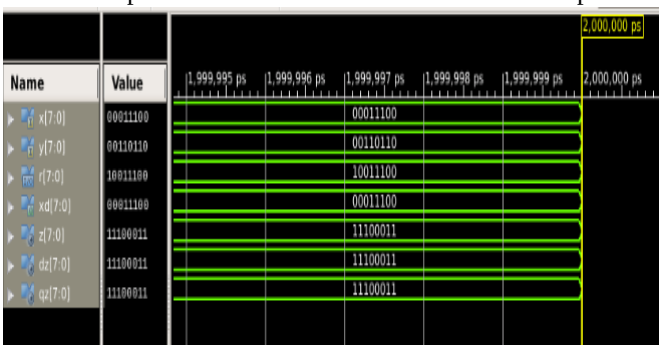

Fig 6: Simulation output.

TABLE II:Tabular form for result analysis

Design	Power	Delay
Data encoding scheme	3.422w	10.066ns
Encoding scheme with GPLS clocking technique	1.309w	9.841ns
Percentage decrease (%)	61.74%	2.24%

Tabular form for the obtained results comparison is shown above. The results obtained shows that delay as well as power in proposed design has been reduced when correlated to the encoding scheme without applying clocking technique.

VI. Conclusion

This paper presents data encoding scheme, reducing power dissipation in NoC links and the delay in transmitting the data from one switch to another. GPLS clocking technique is a variant of mesochronous clocking, in which the phases of clock are different but constant for two switches. From the results the delay and the power has been decreased significantly in the proposed design when clocking scheme is applied compared to the existing data encoding scheme.

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