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Hybridized Power Efficient 32 bit Comparator using Less Transistor Count

Meena Aggarwal, Rajesh Mehra

Abstract - Comparators are basic design element in digital VLSI design, digital signal processors (DSP) and data processing application-specific integrated circuits (ASIC).This paper comprises of design of 32-bit comparator. The above said designs are prepared by combining two different design approaches: Gate Diffusion Input (GDI) and PTL .The two mentioned design approaches are designed in a way to endow with good quality performance. The performance of this proposed 32-bit comparator by hybridizing the two design styles has been compared in terms of transistor count and power which are the important parameters that are considered while designing any digital circuit. The schematic are designed and simulated for its behavior using DSCH-3.1.The layout of simulated circuits are created using Verilog based netlist file which is then simulated in Microwind 3.1 to analyze the performance of comparators at 180 nm CMOS technology. The proposed design provides 57% better performance in terms of transistor count and 21% power efficient design.

Keywords- ALU, Adder module, Comparators, CMOS style, Digital Arithmetic, Full, GDI technique, PTL logic.

I. INTRODUCTION

Comparator is eminent to be a extremely basic and useful component of arithmetic units of the digital systems. The basic function of the comparator is to compare two n-bit numbers and determine the output based on the comparison results. The output results can be either of the three possible outcomes i.e, whether and which number is greater then, equal to or less then. Fig.1 depicts the fundamental block of N-bit magnitude comparator. The result of comparison is represented by 3 binary variables that indicate whether **A>B, A=B, or A<B.** If two n-Bit numbers are to be compared then the circuit will have 2n inputs & 2^{2n} entries in the truth Table [1].

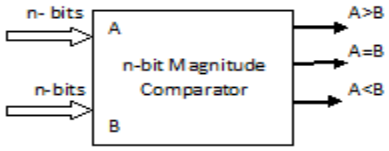


Fig. 1: Block Diagram of n-Bit Magnitude Comparator

II. DESIGN APPROACHES

As per recent trends of miniaturization in chip sizes, VLSI design has become a very important research area. In VLSI technology, silicon area, power consumption and propagation delay are the major design issues which play vital role in it. In today's world, the demand of portable devices is increasing day by day. Thereby, it is required to fabricate more number of devices on a small silicon area in order to reduce the size of the devices. The main factors on which the portability and popularity of these devices depends are area, number of transistors used to implement basic functionality, power dissipation, speed and reliability.

There are numerous approaches which will be useful in designing CMOS comparators. Each scheme will put forward different operating speed, power consumption, and circuit complexity. All the above said parameters may vary evidently from one logic style to another and for that reason proper choice of logic style is very important for desirable circuit performance. The main principle of all the design styles and modifications is to bring down the number of transistors to be used to perform the desired logic, lesser the power consumption and attain an increased speed.

Design approach using combinational logic gates helps in designing fastest comparators. Even though increased speed is achieved but at the cost of area which gets increased due to increased transistor count. Power consumption has two main components: Dynamic Power and Leakage power .

Dynamic and leakage power both are the equal involved for the total power consumption. Basically, dynamic power consists of both switching power and short circuit power. As the dynamic power occurs through computing activity, it cannot be completely removed. Static power dissipation results from leakage produced by CMOS transistor parasitic [2].There are various methods to decrease the power dissipation in VLSI circuits. The most effective method is to decrease the supply voltage V_{DD} since CMOS power quadrically depends on *VDD*. But on the other hand sub-threshold leakage power increase exponentially [3].

PTL (Pass Transistor Logic) is widely used alternative to CMOS applications and this helps in reducing transistor count required to carry out logic in certain cases. Another design approach commonly referred to as Gate Diffusion Input (GDI) Logic also helps in reducing the number of transistors used to implement the logic as compare to CMOS logic style which utilizes both NMOS and PMOS transistors. This technique also helps in reducing the power consumption.

In this paper, a 32-bit comparator is designed using hybridized approach in which firstly 2-bit comparator is designed which utilizes full adder module that is designed by hybridizing PTL and GDI logic and consumes only 9 transistors. By using this 2-bit comparator, 4-bit comparator is designed and then finally 32-bit comparator has been designed to provide the final output of 32-bit comparator i.e. whether first number is greater then, equal to or less then the second number. In this the carry output of first 2-bit comparator is given as third input i.e. carry input to the second 2-bit comparator in order to design the 4-bit comparator circuit. Similarly, by following the same procedure, 32-bit comparator circuit has been designed.

III. COMPARATOR LOGIC STYLES

The work presented herein is focused on basic two styles of design which are as under:

a. GDI Logic b. PTL Logic

A. *GDI logic*

It is also one of the technique which helps in designing low-power digital combinatorial circuit with less number of transistors. Due to reduction in transistor count, it also allows in reducing power consumption, propagation delay which in turn increases the speed of the circuit, and area of digital circuits while maintaining low complexity of logic design [4].

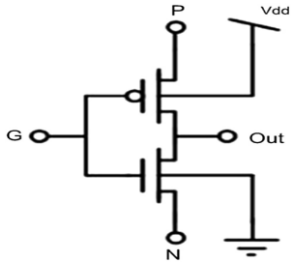


Fig. 2: The Basic GDI cell [4]

Fig.2 shows the basic GDI cell which has three inputs: G i.e. gate which is common to both NMOS and PMOS), P i.e. input to the source/drain of PMOS and N i.e. input to the source/drain of NMOS. As the GDI cell consists of only two transistors, so a wide range of complex logic functions can be implemented using only two transistors. The various logic functions which can be implemented or performed by utilizing this basic GDI cell are given in Table 1. All these functions which are described in table can also be implemented using another technique also but GDI technique provides the fast implementation of these functions. This is also best suited for low power applications.

Table 1. Logic Function using GDI cell [5]

N	P	G	Out	Function
'0'	B	A	AB	F1
B	'1'	A	A+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	AB+AC	MUX
'0'	'1'	A	A	NOT

The various functions which can be performed using GDI basic cells are:

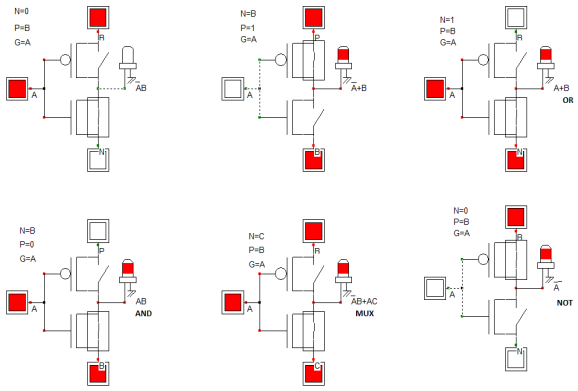


Fig. 3: Various Functions of Basic GDI Cell

B. *PTL logic*

Chief edge of Pass Transistor Logic is to use purely NMOS Pass Transistors network for any logic operation. The fundamental variation of pass-transistor logic style and the CMOS logic style is that the source of the logic transistor networks is connected to some input signals instead of the power lines as shown in Fig.3. In this design approach, transistor acts as a switch and thereby passes logic levels from input to the output [1].Such a design approach requires lesser number of transistors because one pass-transistor network (either NMOS or PMOS) is sufficient to perform any logic operation. Lesser number of transistors result in increased speed.

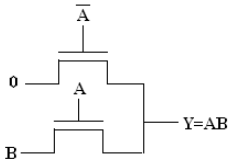


Fig. 4: Symbol for AND Gate using PTL

So, by hybridizing both the techniques we can reduce the area of the circuit as well as power consumption as GDI logic helps to improve the results in terms of power dissipation and PTL logic will help in terms if area utilization.

IV. FULL ADDER DESIGNS

In digital electronic devices, arithmetic unit plays an important role .Full adder is a basic building block used in these arithmetic units. Different logic styles can be used to design the fill adder circuit. The main criteria of concern in full adder design are area consumption, speed and power consumption which often conflict with the design methodology and act as a constrain on the design of full adder circuits. In full adder, the XOR gate is the basic building block. By improving the performance of the XOR gate, the performance of the full adder can be enhanced. So, there are lot of techniques have been designed in order to decrease the transistor count to increase the performance of full adder[6,16]. These performance criteria's must be individually investigated and analyzed for the efficient performance of the digital circuits. Various full adder designs have been presented in [7] - [10], [17],[18].

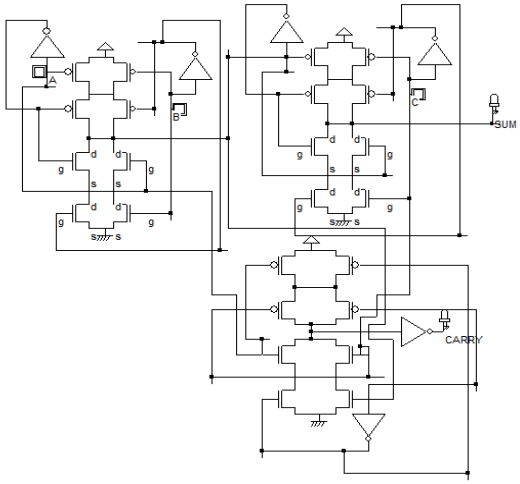


Fig. 5: CMOS Full Adder Design By 2x1 MUX [7]

In Fig.5 a full adder has been designed by using complementary CMOS design which utilizes 36 transistors. In this schematic, 12T complementary CMOS XOR and 12T 2x1 MUX has been used. The sum output is obtained from XOR module and Carry is obtained by using MUX. The drawback of this design is that it consumes large area as ic consumes large number of transistors but it provides full output voltage swing.

Fig.6 shows the full adder designed by using transmission gate technique which utilizes less number of transistors as compare to previous design i.e 22 transistors.

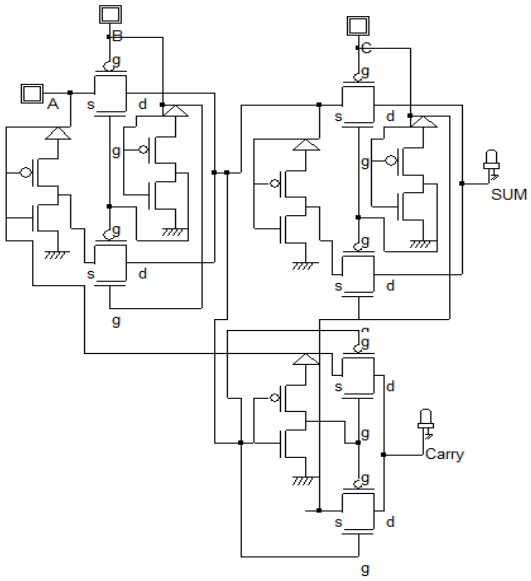


Fig.6: TG Full Adder Design by using 2xl MUX [8]

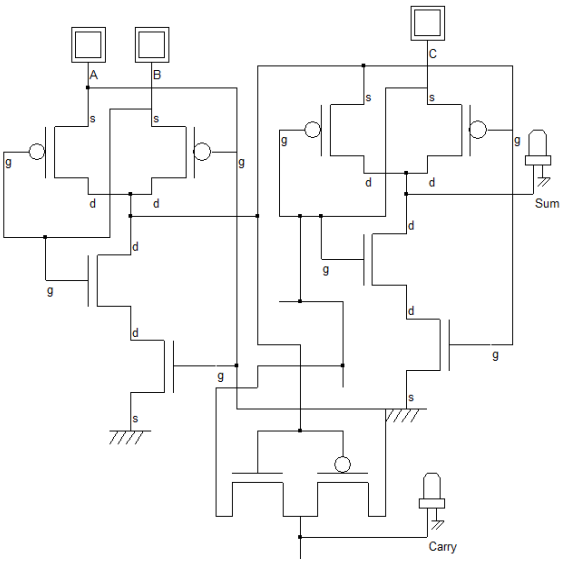


Fig.7: PTL Full Adder Design By 2x1 MUX [9]

Fig.7 shows the schematic of full adder based on PTL logic which utilizes only 10 transistors. If one logic style gives good performance in terms of one parameter it can give degraded performance in other. So, this logic based fill adder design consists less transistors as compared to CMOS and TG full adder designs but can't give full voltage swing at the output [11].

In [12]-[15], the full adder module designed by using GDI technique consists of 10 transistors to obtain the Sum and Carry output. This technique will help in reducing the power consumption. The schematic of this design is shown in Fig.8.

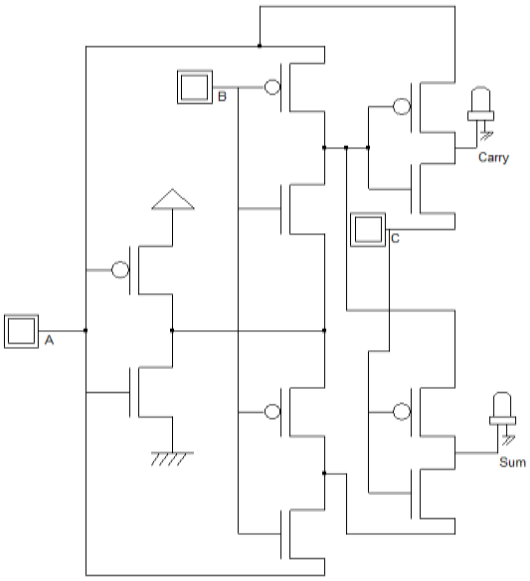


Fig.8: GDI Full Adder Design By 2x1 MUX [10]

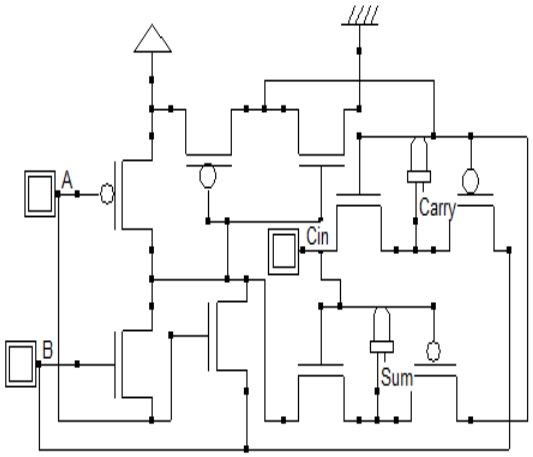


Fig. 9: Hybrid Full Adder Design

In Fig. 9, only 9 transistors are used to design the full adder based on hybridized approach which uses GDI and PTL logic in order to improve the performance of the circuit in terms of area and power consumption.

V. PROPOSED 32-BIT COMPARATOR SCHEMATIC

To design the proposed 32-bit comparator, firstly 2-bit comparator has been implemented which utilizes the full adder module which is designed by using hybridized approach. The design of proposed comparator based on two techniques i.e, PTL and GDI. The schematic of 2-bit comparator based on hybridized full adder module is shown in Fig.10.

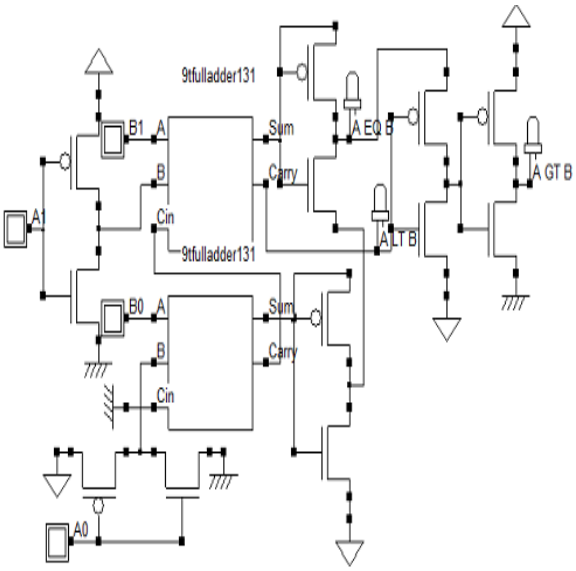


Fig. 10: Hybrid full adder based 2-bit comparator

The 2-bit comparator shown in Fig. 10 is designed to obtain the three output after comparing two numbers

i.e, to find whether first number is less than , equal to or greater than the third number. In this 9T hybrid full adder block is used whose schematic is shown in fig. This schematic will provide good performance in terms of area (number of transistors) and power. Similarly, by using this 2-bit, 4-bit comparator has been designed in which carry output of first 2-bit comparator becomes third or carries input to the second block of 2-bit comparator. By following the same procedure, 32-bit proposed comparator has been implemented. The schematic of proposed 32-bit comparator design is shown in Fig. 12. The proposed design of comparator is hybridized design because it is designed by using two different logic styles in order to implement this circuit.

The timing diagram of 2-bit comparator is shown in Fig.11

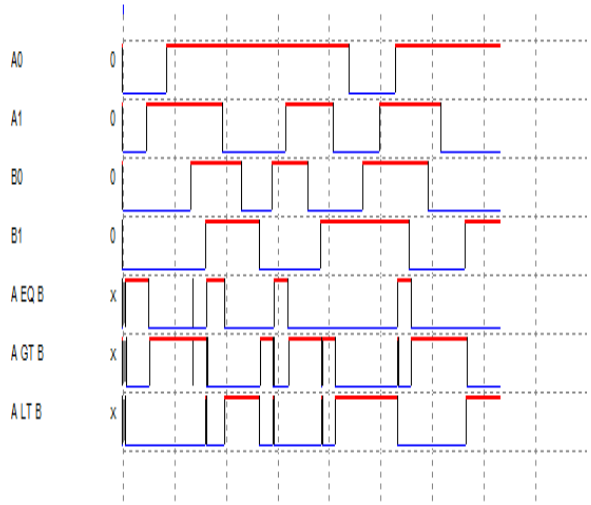
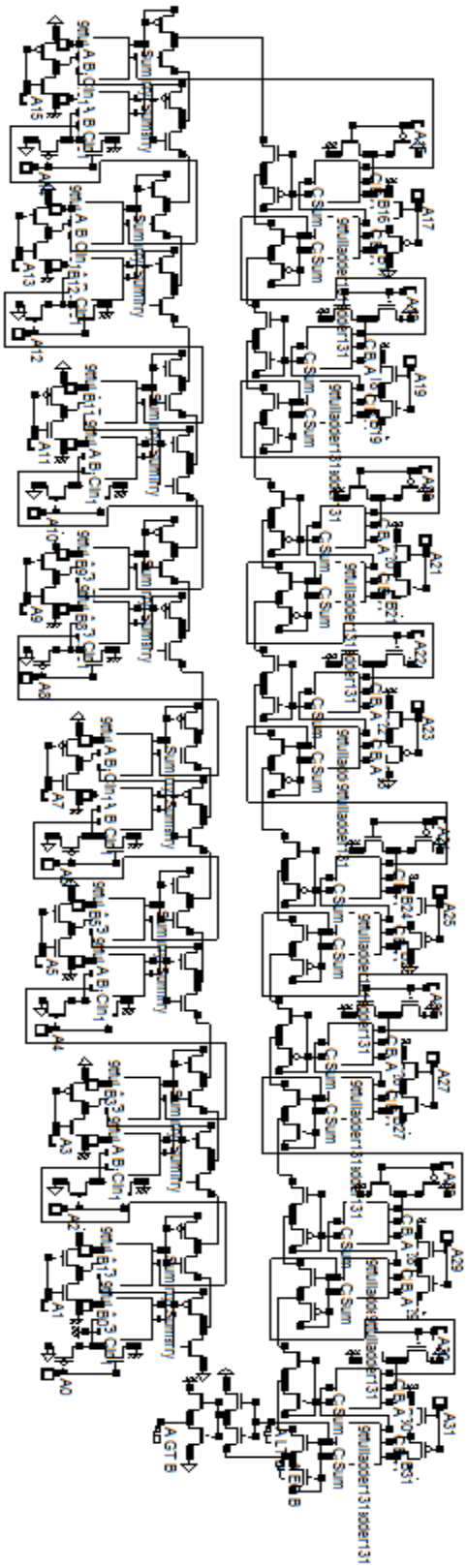


Fig. 11: Timing Diagram of Hybridized 2-bit comparator

The 32-bit comparator shown in Fig.12 is implemented in DSCH3.1 which consists of two inputs A and B each of having 32-bits .This circuit compares the two numbers and provides three values at the output i.e. either A is greater than B, A is less than B or A is equal to B. This comparator utilizes 420 transistors to design the comparator. In this, by using 2-bit comparator , 4-bit has been designed, then from 4-bit 8-bit has been designed , similarly 16-bit and finally 32-bit comparator has been implemented. The carry output of first 2-bit become input to the second 2-bit comparator block.A0 and B0 are the least significant bit whereas A31 and B31 are the most significant bit of the inputs.



Fig, 12: 32-bit proposed comparator schematic

VI. LAYOUT ANALYSIS

In order to design the layout of a very complex circuit, it is very difficult to design it manually. So, an efficient and good approach is to use automatic layout generation tool. . In this approach, firstly the schematic is designed and validated in DSCH tool at logic level. Then simulation is done to check the functionality of the circuit. After that verilog file is generated using DSCH which is further used by MICROWIND tool to generate the layout of the schematic diagram automatically by follow the appropriate design rules [20]. Figure 13 shows the layout of the proposed 32-bit tree structure based hybridized comparator at 180-nm technology. By varying the technology, the area of the layout will also vary.

Fig. 13: Layout of proposed 32-bit comparator

VII. RESULTS AND ANALYSIS

The performance of above mentioned diverse logic styles based 32-bit magnitude comparator has been evaluated in terms of area (number of transistors) and power on 180 nm CMOS technology by using BSIM Level-4 model for different supply voltages. Simulation of various schematics drawn in DSCH-3.1 has been done in Microwind3.1. The results of simulation are shown in Table 2.

Table 2: Result Comparison

Comparator Design	Supply Voltage (V)	Power Consumption (mW)	Transistor Count
J.Y Kim et. Al Using Bitwise logic [21]	1.8	2.53	964
PTL[9]	1.8	2.812	564
GDI[10]	1.8	1.591	596
Proposed comparator (PTL+GDI)	1.8	0.555	420

The result shown in above table is obtained by simulating the 32-bit comparator in Microwind 3.1 at 180nm technology. As it is observed from the above table that when the proposed 32-bit comparator is compare in terms of transistor count with the 32-bit comparator designed in [21] , then it is found that it is 57% less in count and when proposed design is compared with the schematic design by using PTL logic, then it is 26% less in count. Also the proposed design consumes very less power as compare to other. From the above table, it is also observed that PTL logic is better in terms of transistor count whereas GDI provides better results in terms of power consumption. So, to obtain improved results for both the parameters, both PTL and GDI are hybridized. So, it is concluded from the above simulation result that the proposed design of 32-bit comparator implemented using hybridized approach provides better results in terms of number of transistor count and power consumption.

VIII. CONCLUSION

By performing simulation of 32-bit comparator using hybridized approach at 180nm technology by implanting the design using PTL and GDI logic techniques, the final results are obtained in terms of transistor count and power of the device .It has been observed that both PTL and GDI logic helps in reducing the transistor at a great extent and the GDI logic also helps in reducing the power consumption caused by designing on a gate level..This reduction in power consumption results in improvement of performance of circuit. So, it provides area efficient and power efficient design integrating number of stages into one stage. The simulation results have been obtained on BSIM LEVEL-4 model.

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