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VOLTAGE MODE UNIVERSAL FILTER USING VDIBA

Tina Varshney [1], Devesh Singh[2]

Abstract- This paper presents, a voltage mode (VM) multi input single output universal (MISO) filter using voltage differencing inverting buffered amplifier (VDIBA) element. All the filter function such as low pass, band pass, high pass, band reject and all pass can realize without changing the circuit configuration. The pole frequency can be independently tunable by its transconductance parameter. The filter circuit does not require any component matching constraint and enjoys low sensitivity figures. The workability of the filter is verified by cadence using 0.18µm TSMC technology.

Index terms: Tunability, Universal Filter, VDIBA.

I. INTRODUCTION

In analog signal processing, an active filter is very important. It is widely used in various fields such as communication, measurement, instrumentation, control systems and biomedical applications. The design of the active filter, called as multifunction or universal filter has received considerable attention because it can provide several responses using same circuit topology.

The critical issue with continuous time filter approach typically is the RC time constant variation problem where the RC time constant of the circuit varies due to processing tolerance, environmental effects of temperature drift, humidity and aging of components[7].This drawback can be compensated by the use of tunable filters. Thus, there is a growing interest in designing of tunable electronic filters which could compensate for the variation of RC time constant. The progress of analog technology has bred several electronically tunable filters using different active elements such as operational transconductance amplifier (OTA), current conveyors such as second generation current conveyor (CCII), second generation current controlled conveyor CCCII and current differencing transconductance amplifier (CDTA), current controlled conveyor differencing transconductance amplifier (CCCDTA), voltage differencing transconductance amplifier (VDTA), voltage differencing differential input buffered amplifier (VD-DIBA), voltage differencing inverting buffered amplifier (VDIBA), voltage differencing buffered amplifier (VDBA) etc. They are versatile and powerful building blocks for many signal processing applications due to their higher frequency operation, wide dynamic range, and current mode (CM) operation, high bandwidth and low power consumption.

Some recently introduced active building blocks such as VDIBA, VDTA are providing more flexibility in analog circuit designing. These blocks are equipped with tunability feature through their transconductance parameters and also, the circuits based over it do not require any passive resistor. Apart from this, the circuits based over these blocks occupy lesser area because of their low component count. Additionally, the current mode processing of these blocks results into simpler circuit structures. Thus, the use of these blocks results in optimized and high performance circuits. The literature survey reveals that a lot of attention has been given to tunable filters utilizing different active element. Unfortunately, these reported circuits lack one or more of the following important features:

(1) Incompetent to realizing all the five standard filtering functions namely Low pass (LP), High Pass (HP), Band Pass (BP), Band Reject (BR), All Pass (AP).[4]
(2) Independent control of filter parameters. [1, 2, 4, 6]
(3) Lesser sensitivity figures.
(4) Cascadability [1, 2], and
(5) No Component matching constraint [3, 5, 6].

The purpose of this paper is to overcome the aforementioned drawbacks of reported filters. The proposed MISO VM filter circuit employs two VDIBA and two capacitors only. It is capable of realizing all the five filter functions simultaneously without changing the circuit configuration. The bandwidth (BW) and angular resonance frequency (ω_0) of proposed filter can be tuned independently. The performance of the proposed circuit has been verified in 0.18µm TSMC technology.

The paper is organized as follows. Starting from the introduction, section II briefly describes the active element VDIBA. Section III discusses the realization of proposed universal filter. Section IV compares the proposed filter with a previously published filter. Section V shows the simulation result of proposed filter. Finally, the conclusion is drawn in section V.

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II. INTRODUCTION TO VDIBA:

The VDIBA is recently introduced new active element [8]. It is a four port block associated with the feature of electronic tuning. The circuit symbol and behavioral model is shown in Fig. 1 and Fig. 2 respectively. The configuration is having a pair of high impedance voltage differencing inputs *v+* and *v*, a high impedance current output port-z, and low impedance voltage output port-w. The input stage of VDIBA can be implemented by a differential input single output OTA as shown in Fig. 3, which easily converts the input voltage to output current that flows out from the z terminal. The OTA is followed by a unity gain inverting voltage buffer (IVB) amplifier. The introduced active block is very attractive for the realization of resistorless and electronically controllable circuit applications.

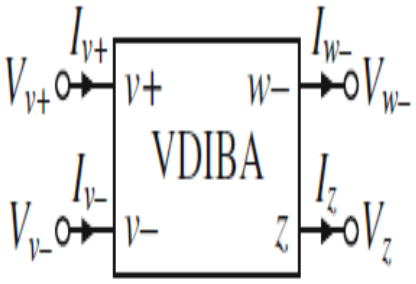

Fig. 1: Symbol of VDIBA

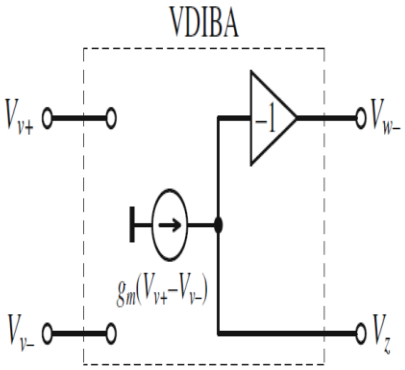

Fig. 2: Behavioral model of VDIBA

Port relation of VDIBA is described by following matrix.

$$\begin{bmatrix} I_{v+} \\ I_{v-} \\ I_z \\ V_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & -\beta & 0 \end{bmatrix} \begin{bmatrix} V_{v+} \\ V_{v-} \\ V_z \\ I_{w-} \end{bmatrix}$$

where, g_m and β stands for the transconductance and non-ideal voltage gain of VDIBA, respectively. The value of β ideally is unity.

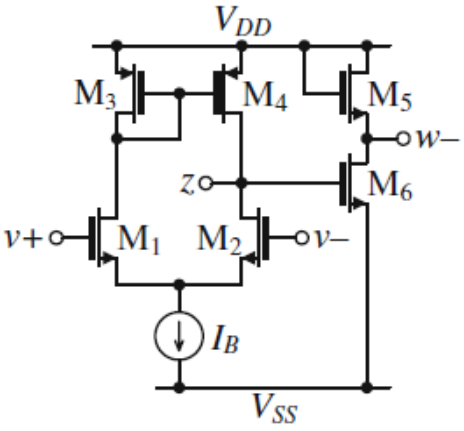

Fig. 3: CMOS structure of VDIBA

III. PROPOSED UNIVERSAL FILTER

The proposed MISO VM universal filter configuration is shown in Fig. 4. It consists of two VDIBA and two capacitors only. It is having three inputs and two outputs. The circuit has the capability to realize filter functions in inverting and non-inverting forms. The biquad filters have low output impedance which is essential for cascadability for voltage mode circuits.

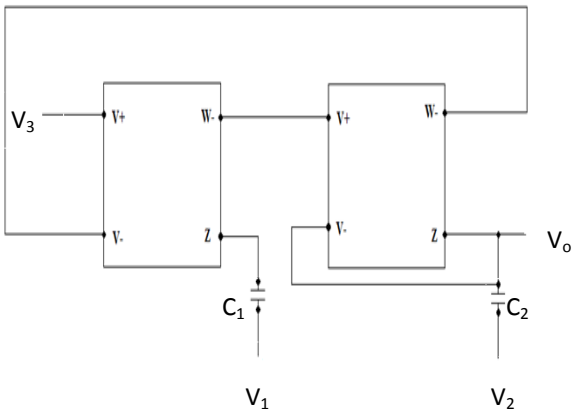

Fig. 4: Proposed VM universal filter

Routine analysis of the circuit, yields the following transfer function

$$V_o = \frac{s^2 V_2 - s\left(\frac{gm_2}{C_2}\right)V_1 - (gm_1 gm_2/C_1C_2)V_3}{s^2 + s\left(\frac{gm_2}{C_2}\right) + (gm_1 gm_2/C_1C_2)} \quad (1)$$

It can be seen from (1) that the proposed filter realizes all the filter functions from the same topology without requiring any component matching conditi

$$Q = \sqrt{\frac{gm_1 C_2}{gm_2 C_1}} \quad (2c)$$

It can be seen from (2) that BW and ω_0 of proposed filter can be tuned independently by first setting the BW by gm_2 and then varying ω_0 by gm_1. The value of Q can be set by capacitance ratio C_2/C_1. Sensitivity analysis of the proposed filter with respect to active and passive elements is less than 1.

Table II: Comparative study of universal Filters

Features/ References	1	2	3	4	5	6	7	8	9
[1]	N	N	N	N	0/1	0/2	5	VM	1(VDIBA)
[2]	N	N	N	N	0/1	0/2	5	VM	1(VDIBA)
[3]	Y	Y	N	Y	0/2	2/0	5	VM	2(VDTA)
[4]	N	N	N	N	0/0	2/0	3	VM	1(VDTA)
[5]	Y	N	N	Y	1/0	2/0	5	VM	1(VDTA)
[6]	N	Y	N	Y	0/0	2/0	5	CM	1(VDTA)
Proposed	Y	Y	Y	N	0/0	0/2	5	VM	2 (VDIBA)

Table I shows realization condition of all the filter functions for various combinations of input variables.

Table I: Input set for different filter functions

S.No.	Input	Filter Function
1	$V_1 = V_2 = 0$, $V_3 = Vin$	LP
2	$V_1 = V_3 = 0$, $V_2 = Vin$	HP
3	$V_2 = V_3 = 0$, $V_1 = Vin$	BP
4	$V_1 = 0$, $V_2 = Vin$, $V_3 = -Vin$	BR
5	$V_1 = V_2 = Vin$, $V_3 = -Vin$	AP

For all filter responses the bandwidth, resonance angular frequency (ω_0) and quality factor (Q) can be expressed from the denominator of (1) are given by

$$\omega_0 = \sqrt{\frac{gm_1 gm_2}{C_1 C_2}} \quad (2a)$$

$$BW = \frac{gm_2}{C_2} \quad (2b)$$

IV. COMPARISON

The proposed filter has been compared with previously published filter in Table II on the basis of following important features such as (1)Independently tuned filter parameters (2) Appropriate input port impedance (High-for voltage, Low for current Grounded/ floating) (3) Appropriate output port impedance-(Low-for voltage, High for current) (4) Component Matching constraints (5) No of resistors (Grounded/ floating) (6) No of capacitors (Grounded/ floating) (7) No of filter functions –Low pass, High pass, Band pass, Band stop, All pass (8) Mode of operation (CM/VM) (9) No of active elements with name. Thus, it can be seen that the proposed filter provides better features, while the other filters listed in Table II lack one or more important features.

V. SIMULATION RESULTS

To validate the proposed configuration, it is simulated using cadence. The DC power supply voltages used for CMOS VDIBA is 0.9V. The aspect ratios of the OTA (M1-M4) and the IVB (M5 and M6) has been taken as $W/L_{(M1-M4)}$ =18µm/1.08µm and $W/L_{(M5,M6)}$=54µm/0.18µm. The transconductance (gm_1, gm_2) of VDIBA has set to 656.01µA/V. The bias currents has been selected as I_{B1} = I_{B2} =100 µA. The value of passive components C_1 and C_2 is taken as 30pf and 15pf respectively. The transconductances are controlled by bias currents of VDIBA. Fig. 5 shows the simulated filter responses of LP, BP, HP, BR and AP. The choice of component values results in Q = 0.707, f_0= 4.9 MHz, and BW= 43.7 MHz for equal bias currents i.e. for gm_1 and gm_2. These result, thus confirm the validity of proposed filter.

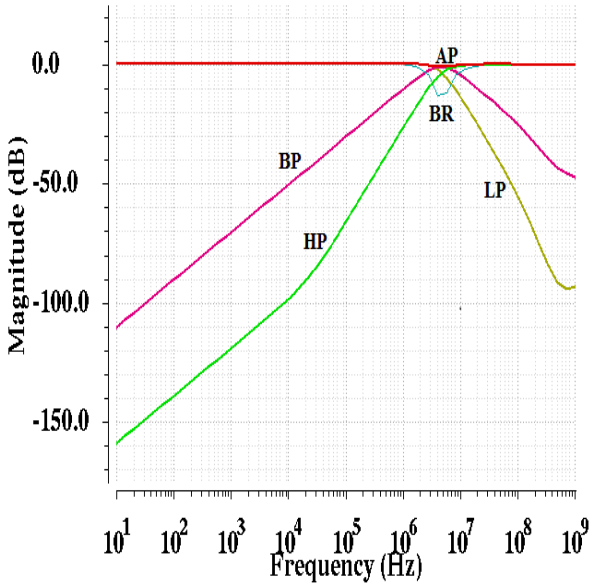

Fig. 5: Frequency response of proposed universal filter

VI. CONCLUSION

The proposed circuit uses two VDIBAs, two grounded capacitor. The circuit is capable to realize all the filter functions without changing circuit topology. The circuit enjoys independent electronic tuning between pole frequency and Bandwidth. Moreover, the configuration does not require any component matching constraints and has low active and passive sensitivities. The performance of the proposed circuit is verified by cadence simulations using 0.18µm technology.

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Tina Varshney (M.Tech scholar) received the degree of B.Tech in Electronics and communication engineering from Shobhasaria Engineering College, Rajasthan in 2010. Her areas of interest are design of analog signal processing circuits and low power CMOS VLSI design. Currently pursuing M.Tech at A.K.G Engineering College, Ghaziabad

Devesh Singh received the degree of B. Tech. in Electronics and Communication from Institute of Engineering & Technology, Jaunpur and degree of M.E in Communication System from Jabalpur Engineering College, Jabalpur, India in 2001 and 2005 respectively. He is working as an

Assistant Professor in A.K.G. Engineering College, Ghaziabad as since 2005. He has published five papers in various international journals and conferences. His research includes design of analog signal processing circuits.