

# An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi standard DUC

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**ABSTRACT:** Most of the area occupied in the design of FIR filter is the multiplier. The low power and area architecture of pulse shaping FIR filter for digital up converter was designed. In the existing system, the two bit binary common sub-expression based binary common sub-expression elimination algorithm and shift and add method was used to generate the partial products. In this paper, carry save adder is used instead of shift and add method and also the simple arithmetic adders of multiplexer unit is replaced by carry save adder. The number of additions and multiplications are reduced using this technique. The designed pulse shaping FIR filter is synthesized and simulated using Xilinx ISE 14.3.

**KEYWORDS:** Digital up converter (DUC), finite-impulse response (FIR) interpolation filter, reconfigurable hardware architecture, software defined radio (SDR) system.

## I. INTRODUCTION

Software Defined Radio (SDR) technology is significantly used in wireless communication and it refers to the class of reconfigurable radios in which the physical layer behavior can be flexible through reconfiguration. In the SDR system, FIR filters are mostly used in Digital Up Converter and Digital Down Converter. Digital Up Converter (DUC) is widely used in communication systems for converting the signal sample rate. It is needed when the signal is transmitted from baseband signal to Intermediate band. The input signal which is given to the DUC is filtered and transformed into higher sampling rate and then the signal is modulated with carrier signal. The various sections of Digital Up Converter (DUC) have been optimized individually and then compound in concert. The digital signal processing application using variable sampling rates can improve the flexibility of a software defined radio. It reduces the need for expensive anti-aliasing analog filters and enables processing of different types of signals with different sampling rates. It allows partitioning of the high-speed processing into parallel multiple lower speed processing tasks which can lead to a significant saving in computational power and cost.

## THE RECONFIGURABLE ROOT-RAISED-COSINE FIR FILTER AND ITS PROPOSED METHOD FOR SOLUTION

### A. Issues in Designing the Reconfigurable RRC FIR Filter for Multi standard DUC

As a design example of multi standard DUC, we have considered three standards, namely universal mobile telecommunication system, wideband code division multiple access, and digital video broadcasting. These three standards have adopted root-raised-cosine (RRC) filter as the pulse shaping filter for its ability to decrease the bit error rate by disallowing timing jitter at the sampling instant. Efficient hardware implementation of a reconfigurable RRC FIR interpolation filter with the specification mentioned.

1) For a filter of  $N$  tap with interpolation factor of  $R$ ,  $N/R$  equivalent multipliers (to implement the convolution operation between the inputs and the filter coefficients), and structural adders (to perform the final addition operation for generating the output) are required. Implementation of three different filter lengths of  $L$ ,  $M$ , and  $N$  with three different interpolation factor  $P$ ,  $Q$ ,  $R$  would require  $L/P + M/Q + N/R$  number of equivalent multipliers and structural adders. Now, if the filter parameters (roll-off factors for RRC filter) are different, the total number of multipliers and structural adders will linearly increase with the number of parameters considered for designing the filter. For a constant propagation delay, the problem of area and power consumptions increases as the number of multipliers and structural adders increases for implementing the variable length higher order filter in a single architecture.

2) Amongst several techniques proposed earlier, the BCSE method is the recently proposed popular method for implementing an efficient constant multiplier. In BCSE algorithm, a coefficient of  $m$ -bit word length can form  $2m - (m + 1)$  BCS amongst themselves. Proper choice of the length of the BCS is

an important factor to avoid the inefficient utilization of hardware.

3) In BCSE technique, LD is the critical path that mainly depends on the number of addition operations in a chain. Propagation delay of the filter is measured by the computation time of  $(LD + 1)$  addition operations. Proper use of BCS to decrease the LD that maximizes the operating frequency of the filter is a challenge.

4) CMs are performed through shift and add operations. For example, if  $X$  is the number of adders required for a single CM operation, implementation of  $L$ -,  $M$ -, and  $N$ -tap filters will require  $\{[L/2 + M/2 + N/2] * X\}$  number of adders. By reducing the number of adders by  $Y$  say, for a single CM, one can save  $\{[L/2 + M/2 + N/2] * Y\}$  number of adders to implement the desired reconfigurable FIR interpolation filter. Therefore, the task of maximizing the value of  $Y$  can pose a challenge to the designer.

## B. Proposed Method for Solution

The technique proposed in this brief to solve the problem addressed above consists of the following steps.

1) In the first coding pass (FCP) block, the coefficient sets of the two RRC filters of the same length differing only by the filter parameters are multiplexed through one 2:1 multiplexer, where one control parameter (FLT\_SEL) selects the desired filter depending on the roll-off factor. This multiplexing technique helps in decreasing the requirement of the multiplier by 50% as the total number of coefficients is 111 instead of the initial requirement of 222.

2) In the second coding pass (SCP), the coefficients obtained from the FCP block are passed through another set of multiplexers, where one control parameter (INTP\_SEL) selects the desired filter depending on the interpolation factor. This technique reduces the total number of filter coefficients that will be processed further from the earlier requirement of 111–49 after the FCP. Combination of FCP and SCP steps reduces the requirement of MPIS from 42 to 7 and APIS from 36 to 6, which facilitates 83.3% improvement for this design. According to the proposed method, considering more filters of different specifications will cause more reduction in the APIS and MPIS.

3) Instead of 3-bit BCSE presented, we have proposed 2-bit BCS-based BCSE technique, where the LD can be defined as

$$LD_{2BCS} = \lceil \log_2 2 \rceil + \log_2 \left\lceil \frac{16}{2} \right\rceil = 4 \quad (1)$$

where the term  $\log_2 2$  is due to the 2-bit BCS and the term  $\log_2 16/2$  is due to the fact that the word-length for the coefficients has been considered to be 16 bits. Hence, for the 2-bit BCS-based FIR filter, its propagation delay can be defined as

$$T_{2BCS} = 4 \times t_{add} + t_{4:1mux} + t_{acc} \quad (2)$$

where  $t_{add}$  is the delay of each adder used in the constant multiplier,  $t_{4:1mux}$  is the delay for the 4:1 multiplexer, and  $t_{acc}$  is the delay for the final adder in the delay chain of FIR filter. From (1) and (2), it can be clearly seen that use of 2-bit BCS leads to a good amount of saving in the propagation delay compared with the 3-bit BCS-based constant multiplier design.

4) In any FIR filter, the multiplication operation between the inputs and the coefficients, for which the word length of the coefficient is 16 bits can be written as

$$y1 = x1 + 2^{-1}x1 + 2^{-2}x1 + 2^{-3}x1 + \dots + 2^{-14}x1 + 2^{-15}x1. \quad (3)$$

Considering 2-bit BCS in the proposed architecture i.e.,

$$x2 = x1 + 2^{-1}x1 \quad (3) \text{ can be rewritten as}$$

$$y1 = x2 + 2^{-2}x2 + 2^{-4}x2 + \dots + 2^{-10}x2 + 2^{-12}x2 + 2^{-14}x2. \quad (4)$$

In the proposed architecture, the shift add unit has been grouped in eight preshifted values of  $2N + 1$  bit, where  $N = 8, 7, 6, 5, 4, 3, 2, 1$  to implement (4). This will help in reducing the multiplexer and the adder width. As this shifting is done prior to the addition operation, the maximum error (due to truncation) has been precalculated and added in the final addition operation of the constant multiplier block. This technique helps in reducing the hardware, as explained in the previous section.

## II. PROPOSED METHODOLOGY

### A. Data Generator

When the clock signal is applied to the data generator, the data has been mechanically furnished by sampling the input signal. The input data is sampled based on the selected value of the selection lines of multiplexer. The fig.1 shows the flow diagram representation the RRC filter.

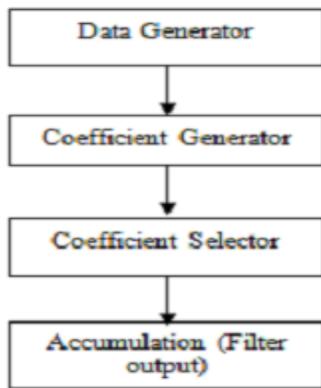


Fig .1 Flow diagram of RRC filter design

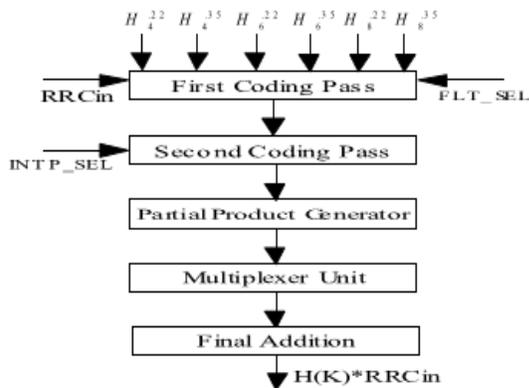


Fig.2 Flow diagram of Coefficient Generator

### B. Coefficient Generator

Coefficient generator comprises of first coding pass, second coding pass, Partial Product Generator, multiplexer unit and addition. The multiplication operation between the inputs and the filter coefficients is performed by coefficient

generator. The hardware usage has been reduced by two-phase optimization technique. Each of the blocks in coefficient generator are structured using multiplexer. The operation performed by the first coding pass and the second coding pass are similar.

#### i) First Coding Pass

It takes the input from the output produced by the data generator. The inputs are selected from the data generator are processed and the outputs are produced based on the selected values of the selection lines of multiplexer.

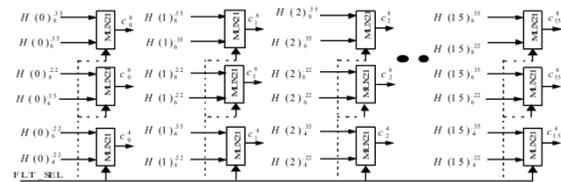


Fig.3 Architecture for implementation of FCP block.

#### ii) Second Coding Pass

The operation of the second coding pass is similar to the first coding pass. It takes the input from the produced output by second coding pass. It produced the output based on the inputs selection which are processing then based on the selected values of the selection lines of the multiplexer, the output has been produced.

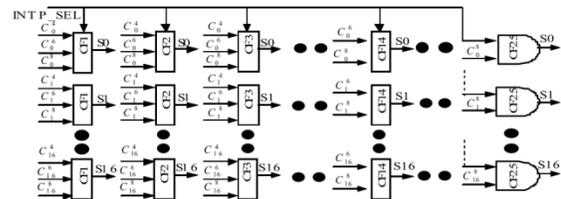


Fig.4 Architecture for implementation of SCP block.

#### iii) Partial Product Generator (PPG) Unit:

Shift-and-add method is used to generate the partial product during the multiplication operation between the input data (Xin) and the filter coefficients. In BCSE technique, realizations of the common subexpression using shift-and-add method eliminates the common term present in a coefficient. In the proposed architecture, 2-bit BCSs ranging from 00 to 11 have been considered. Within four of these BCSs, an adder is required only for the pattern 11. This facilitates reduction in hardware and improvement in speed while performing the multiplication operation.

The shift-and-add block used in this brief is shown in Fig. 5.

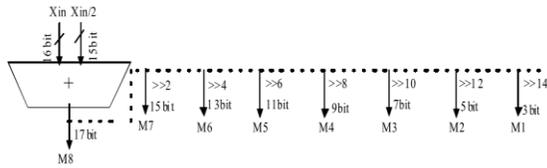


Fig.5 Architecture for implementation of PPG block.

**iv) Multiplexer Unit**

The output of carry save adder is shifted and it is given as the inputs to the multiplexer. It will choose the required data from the carry save adder based on the coded coefficients. The selected inputs are processed and the outputs that are produced from the mux unit are again summed up with carry save adder.

**v) Addition**

For addition unit, the inputs are taken as the input from the output of multiplexer unit which gets added using carry save adder and the produced outputs are varied depending on the sign magnitude and then it is given to multiplexer and produces the output.

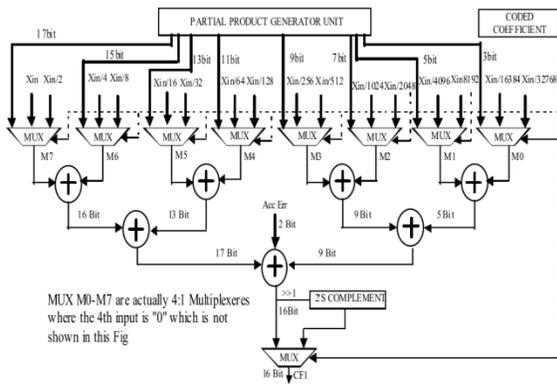


Fig.6 Block diagram of multiplexer and final addition unit.

**C. Coefficient Selector**

The inputs are taken from the output of the coefficient generator which selects the required data for processing. Then the selected inputs are then multiplied using the operation of AND then based on the multiplexer's selection line, outputs will be produced.

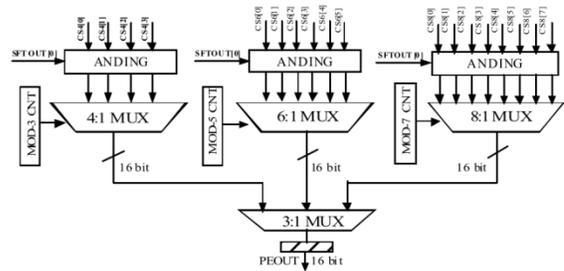


Fig.7 Hardware architecture of CS block.

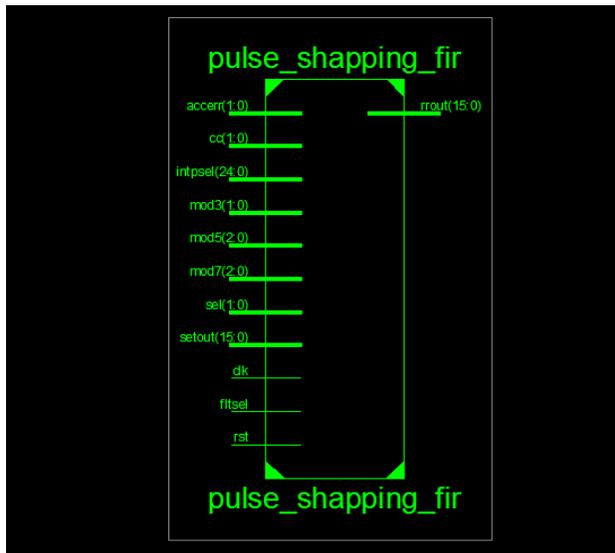
**D. Accumulation**

The inputs for accumulation were taken from the output of the data generator, coefficient generator and coefficient selector which are then added and the filter output will be produced.

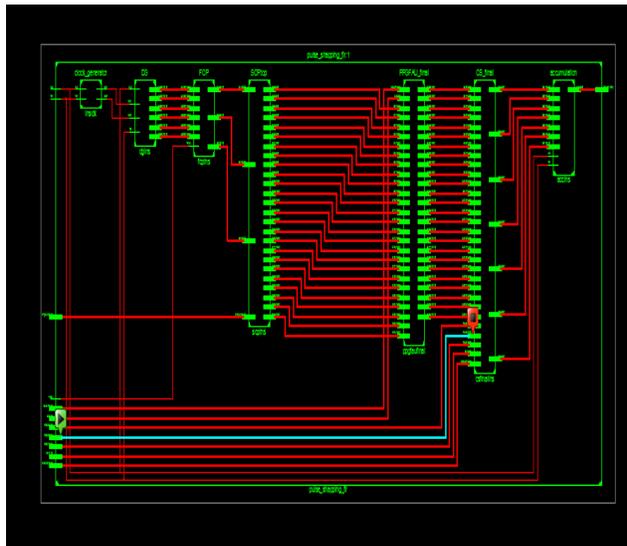
**III. RESULTS AND DISCUSSION**

The low power and area efficient architecture of pulse shaping FIR filter for digital up converter has been designed and simulated using Xilinx. The parameters considered for the designed architecture are area and speed. The serial input data is passed to the data generator to sample the input which are then processed and produced the output based on the selected values of the selection lines of the multiplexer. In coefficient generator, the sections are first coding pass, second coding pass, partial product generator, multiplexer unit and addition unit are processing the inputs and produced the output based on the coded coefficients. For coefficient generator, the inputs are taken from the output of the data generator. Then coefficient selector takes the input from the output of the coefficient generator and it will steer the proper data based on selection lines. Finally, the final accumulation block produces the filter output by summing up all the outputs.

**Block diagram**



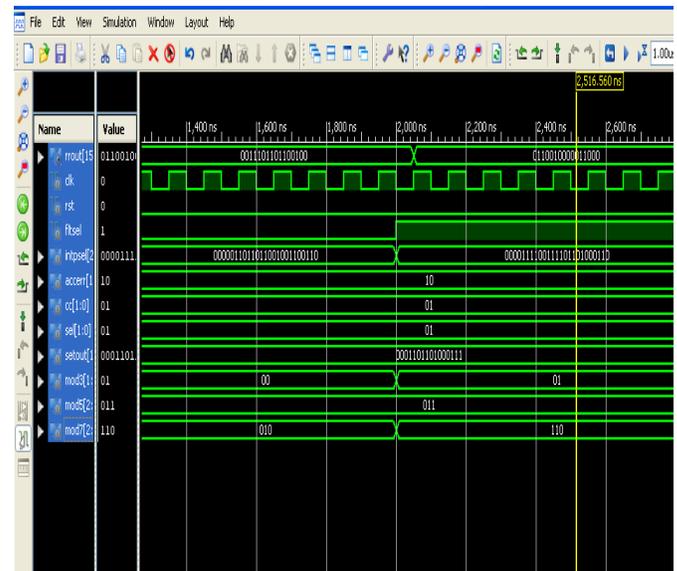
**RTL schematic**



**Design summary**

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	26	126800	0%
Number of Slice LUTs	5618	63400	8%
Number of fully used LUT-FF pairs	20	5624	0%
Number of bonded IOBs	74	210	35%
Number of BUFG/BUFGCTRLs	1	32	3%

**Output waveform**



**IV. CONCLUSION**

In this paper, reconfigurable pulse shaping FIR filter was designed for multistandard digital up converter for Software Defined Radio system. The complexity

of area is caused by the multipliers. The modification to the architecture is included by which carry save adder was used to reduce the power and area consumption. So that the speed of the operation gets increased and also area of the architecture gets minimized. While using this technique, the additions and multiplications were reduced for generating the partial products.

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