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5-Bit Interpolating ADC Using Low Power Encoder

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***Abstract*— This paper presents the design of 5-bit interpolating analog to digital converter using Low power encoder used in most of Ultra Wide Band applications. The architecture of ADC consists of input amplifier, sample and hold circuit, Resistor ladder , comparator array and digital encoder .The N-bit Interpolating ADC consists of 2^n comparators .The output of the comparator array is in the form of thermometer code .This can be converted into binary using digital encoder. The usual implementation of this encoder is based on XOR gates .This design takes more hardware and high transistor count hence power hungry .Here a new encoder is designed which is based on multiplexers .This Multiplexer based encoder reduces power ,area and utilizes minimum number of transistors .So ,Low power design of multiplexer based thermometer code to binary code encoder helps in improving the performance of complete system .This 5-bit Interpolating ADC is designed in 180nm technology in CADENCE using Virtuoso tool.**

Keywords*—Analog-*to-Digital conversion ,XOR based encoder , Multiplexer based encoder ,resistor ladder ,Low power.

1. Introduction

Signal processing plays a major role in many of the system on chip applicatios.With the advancement in technology, digital signal processing posses significant importance in the field of telecommunication. Ethernet and ultra wideband applications.

Ultra Wide Band (UWB) is new wireless technology that uses train of pulses to transmit information. An ultra wide band signal [11] is typically composed of train of narrow second pulses, resulting in a high bandwidth. Digitization an RF signal near the antenna, a high speed, high resolution analog to digital converter is complex to design and it is power hungry. Because of large bandwidth used, ultra wide band links are capable of transmitting data over tens of megabits per second .A single receiver could support different modulation schemes, bit ranges ,quality of service and operating ranges.

The minimum number of bits needed for reliable detection of an ultra wide band signal is a critical parameter. If the bits are large, ultra wide band receiver infeasible.

In 2002, The Federal communications commission allocated spectrum for a new radio communication technique called Ultra Wide Band with the frequency band between 3 GHz to 10 GHz being made available for UWB based applications .Many researches are involved in developing new electronic devices and applications that can work in this band. The great potential of UWB [11] lies in the fact that it can co-exist with the users of already lienced spectrum and that it opens a wide range of applications. Such applications include high speed wireless personal area networks wireless USB.

ADC is a mixed signal device that converts analog signals into digital signals for processing the information .In the recent years ,the need to design a low power ,low voltage ,wide bandwidth and high speed analog to digital converters has increased rapidly .Normally analog to digital conversion involves sampling[1] the input analog signal and processing the sampled signal to generate the discrete output bits .The rate at which the signal is converted into its digital form determines the conversion speed and the number of output bits represents the resolution of the ADC.Among several types of ADC Interpolation analog to digital converter is one of the category of high speed and low to medium resolution type of ADC. Interpolation ADC provides less input capacitance along with simplified design of the comparator.

Hence interpolation ADC's are faster in speed and have higher input signal bandwidth. Low resolution interpolation analog to digital converters are used as sub blocks in comparatively low power ADC's like sigma delta ADC and time interleaved ADC's .So ,the low power design of low resolution interpolating ADC can plays a major role in reducing the power consumption of other high resolution ADC's.and there by improving the total system performance .In interpolation ADC there are various blocks such as pre amplifier ,resistor ladder ,comparator and thermometer code to binary code encoder .Even though the comparator array and resistor ladder consumes major part of ADC power, the encoder block also plays some significant role in total power consumption of the ADC.

The paper is organized as follows. Chapter 2 explains the proposed architecture of interpolating ADC .The details of preamplifier ,sample and hold ,comparator and digital encoders is shown in Chapter 3.Chapter 4 discusses the comparisons of Mux based Encoder with Xor based Encoder interms of power and hardware.Simulation results are shown in Chapter5.Finally the conclusion is presented in Chapter6.

2 ADC Architecture

Interpolating ADC is suitable for high speed and low to medium resolution conversion.There are basically two methods for interpolation namely resistive interpolation[10] and current mode interpolation .Current mode interpolation[5] is based on summation of currents reflected through current mirrors with different ratios.However this method is complex proves to be power hungry and not very precise due to the non idealities of the current mirrors[5].For these reasons resistive interpolation is preferred .The resistive interpolation can be implemented

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using resistor ladder .Figure1 shows the architecture of 5 bit interpolating ADC .The ADC is consists of frontend Preamplifier ,sample and hold circuit ,comparator array and digital encoder block. During first stage the analog input signal is fed into amplifier and this amplified output signal is sampled by sample and hold circuit [2] and a Comparator compares the sampled input signal with reference voltage generated by resistor ladder. The output of comparator array produces thermometer code .Finally a multiplexer logic then converts the thermometer code into binary with power power consumption.

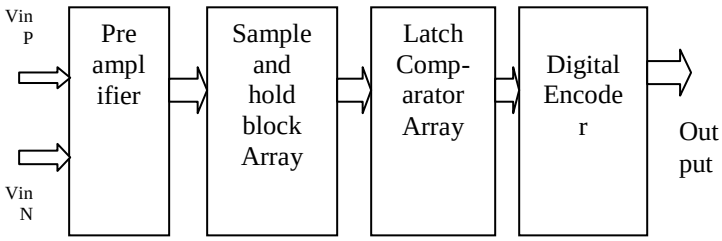

Figure 1: 5-Bit Interpolating ADC

3. Circuit Implementation

The design of different blocks in ADC are shown below.

3.1 Pre amplifier

The principle of the preamplifier is that the preamplifier amplifies the input signal and the amplified signal is inputted into the sample and hold circuit. In figure2, Mos transistors M1 and M2 are driven by the resistive loads. The two input signals with opposite polarity are amplified and resulting in interpolated output voltage. The number of preamplifier stages varies depending on the ADC bit resolution and its Interpolation factor. Normally higher resolution results in more stages. It also amplifies small input voltage difference to a large enough voltage to overcome the offset voltage of the comparator [7].

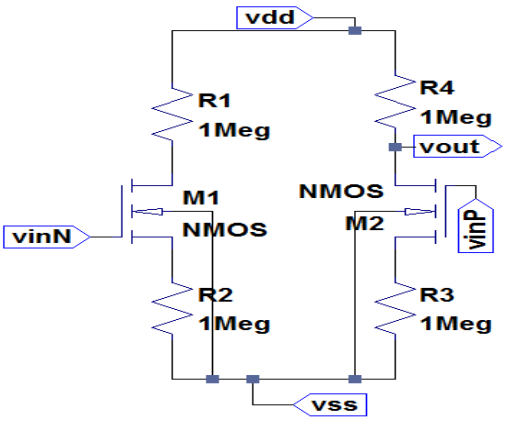

Figure 2: Pre Amplifier

3.2 Sample and Hold

The performance of Interpolating ADC depends on its ability to sample the input without jitter. The function of the sample and hold circuit is to sample the amplified analog signal.Figure3 shows the sample and hold circuit with two MOS transistors and one capacitor. During the sampling phase [1] when the clock goes high, the input signal is sampled and the capacitor is charged to the input level. During hold mode when clock is low the sampled signal is held on constant and the capacitor discharges through the same path.

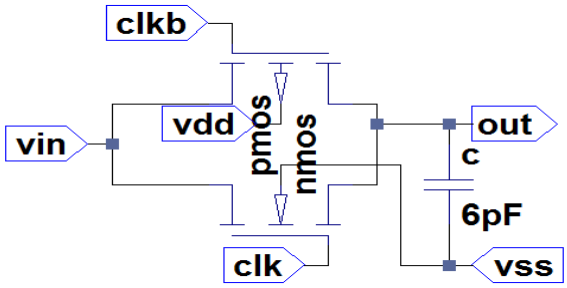

Figure 3: Sample and Hold circuit

3.3 Latch Comparator

Comparator is the basic building block of Interpolating ADC as it determines the speed and accuracy of adc.For N bit Interpolating ADC we require 2^N comparators. Figure4 shows the design of comparator .The comparator compares the sampled input signal with the reference voltage generated by a resistor ladder. A voltage of 1.5V is provided to the resistor ladder as full scale voltage [8] of Interpolating ADC.The bias voltage and the width of the transistors must be chosen carefully to ensure all transistors are in saturation.

The output of the comparator is High, if the input voltage is larger than the reference voltage at the input of the comparator, otherwise the output is low. The output of the comparator array is in the form of thermometer code ,as it is called thermometer code because as the amplitude of the input signal increases the number of ones in output increases linearly which is similar to the mercury rise in the thermometer.

During the operation, the architecture of comparator consists of three stages, preamplifier stage, decision circuit (latch) stage and finally output Buffer stage. The two nmos transistors M1 and M2 are driven by the current source. Differential pair is loaded by two pmos transistors M3 and M4.The four transistors M1, M2, M3 and M4 forms preamplifier stage. Preamplifier in comparator must have sufficient gain in order to amplify the difference between two inputs.

Second stage uses positive feedback [6] mechanism. The purpose of positive feedback is to boost the differential voltage gain obtained by M1 and M2 and to balance the output resistance. Output Buffer converts the output of decision circuit to logical signal.

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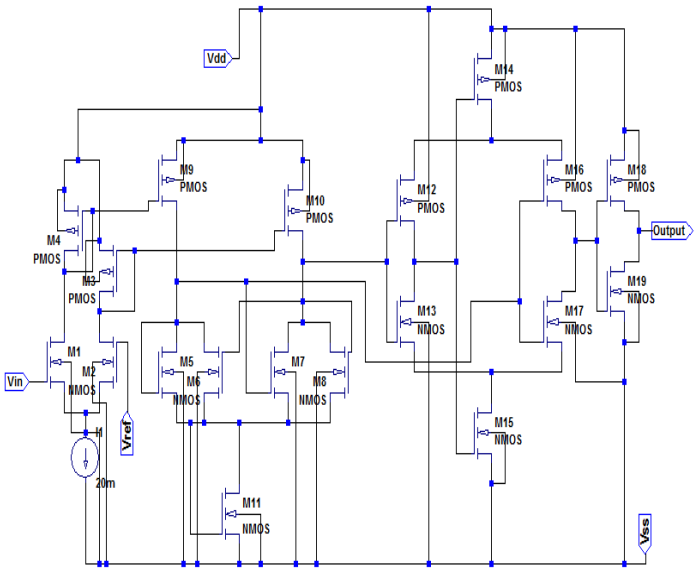

Figure 4. Latch Comparator

3.4 Encoder

3.4.1 Xor based Encoder

The output of a thermometer-to-binary encoder is the Summation of digital ones in input thermometer code. For high speed applications the Xor based encoder is shown in figure5.This architecture consists of totally thirty one Xor gates. The disadvantages of this Xor based encoder is that, it occupies more area due to utilizing of more number of logic modules and transistors. Hence it seems to be power hungry. Also it makes ADC infeasible to low power applications. Hence there is a scope to improve the performance of Encoder, which utilizes minimum number of transistors.

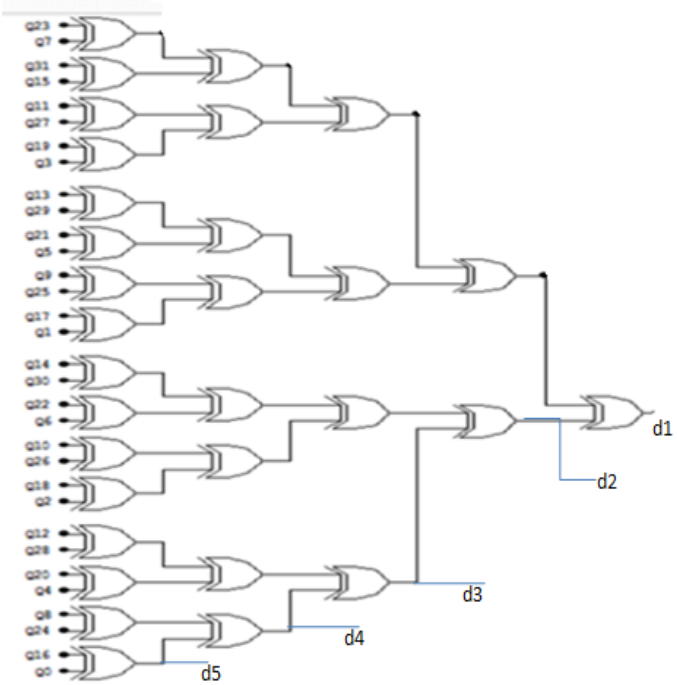

Figure 5: Xor based Encoder

3.4.2 Multiplexer based Encoder

Thermometer code to binary code conversion circuits are considered as the bottleneck in the design of interpolating analog to digital converters. Since the speed of the entire circuit affected by this digital backend of complete architecture .Choosing a perfect design for encoder portion is very important. In this architecture the thermometer code can be converted into gray code using 2:1 multiplexers [4] and then XOR logic [8] is used to converting gray code to binary code. Converting the thermometer code to gray code will help in reducing bubble errors [9].

The basic building blocks of entire architecture are 2:1 multiplexers [4] and two input XOR gates as shown in figure6.Proposed architecture is consists of two stages. First stage is conversion of thermometer code to gray code and second is getting binary code from gray code.

From figure6, Thermometer code input T16 is kept as select line of Mux1, T32 is connected to input0 and T16 itself connected to input1.To get G4 Thermometer code input T24 is kept as select line of Mux2, T8 is connected to input0 and input1 is grounded. To getG3, the output of Mux3 is given to input1 of Mux4 by keeping T12 as selection line. The process is repeates for remaining Mux's until to obtain all gray codes. The Boolean expression for this conversion is shown below.

$G5=\overline{T16}.T32+T16$

$G4=\overline{T24}.T8$

$G3=\overline{T12}.T4+T12.(\overline{T28}.T20)$

$G2=\overline{T6}.T2+T6.(\overline{T14}.T10+T14.(T22.\overline{T18}+T22.(T30.\overline{T26})))$

$G1=\overline{T3}.T1+T3\ (\overline{T7}.\overline{T5}+T7\ (\overline{T11}.\overline{T9}+T11\ (\overline{T15}.T13+T15\ (T19.T17+T19\ (T23.T21+T23\ (T27.\ T25+T27\ (T31.T29)))))))$

In the second stage, XOR logic [8] is used to convert gray code to binary code. The Boolean expression for this conversion is shown in below.

B5=G5

B4=G4XORB5

B3=G3XORB4

B2=G2XORB3

B1=G1XORB2

Converting the thermometer code to gray code will help in reducing bubble errors. Bubble error is result of many sources, for example, clock jitter, device mismatch. The input thermometer code of an Encoder circuit is invalid code. Consequently, if there is no correction circuit, the output of the thermometer code to binary circuit or the output of the ADC in this case is incorrect.

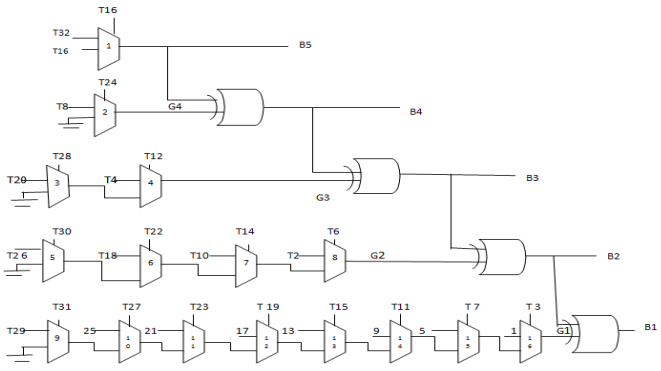

Figure 6: Multiplexer based Encoder

4. Comparisons of the Approaches

The Multiplexer based Encoder seems to have capable and beneficial interms of amount of hardware and power consumption. A comparison of the performance between the Xor based encoder and Mux based Encoder is given in below table 1.

Table 1: performance comparison of 5 bit interpolating ADC

Type of Encoder	Power	No.of Transistors
Xor based Encoder	1.303 nW	248
Mux based Encoder	0.854 nW	128

As seen in Table 1, the hardware is significantly reduced when using Mux based Encoder. For the mux based encoder, the number of transistors are reduced by more than 50% compared to the Xor based encoder.

5. Simulation Results

Figure7 shows that, the 5 bit Interpolating ADC is successfully simulated using low power Encoder. The below figure shows the transient analysis of proposed ADC obtained in Cadence Virtuoso Visualization and analysis editor.

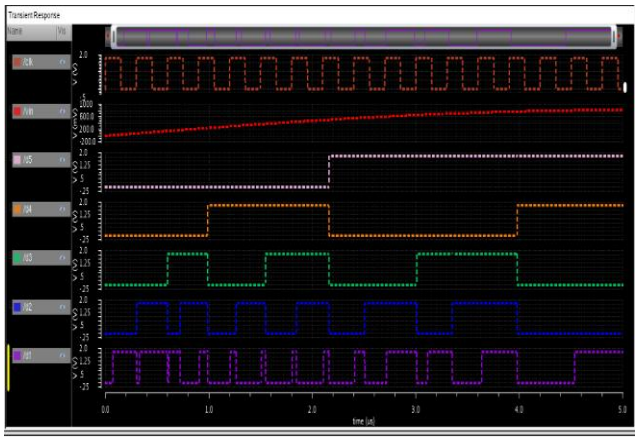

Figure 7: Simulation results

6. Conclusion

This work presents design of 5-bit Interpolating ADC using low power Encoder. Our study demonstrates that the multiplexer based encoder is an attractive approach for designing thermometer-to-binary Encoder. The amount of hardware and power consumption is less than compared to the Other existing Encoders. This should make it possible to design for lower power applications. In addition, it has a more Regular structure than the other encoders, which is an advantage When doing the layout.

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