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A New Power and Area Efficient 4-bit Flash ADCUsing Multiple Selection Method

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Abstract:This paper presents the design of a 4 bit flash ADC using multiple selection method using CMOS technology of GPDK 180nm. The architecture used in this ADC uses comparators with multiplexers instead of comparators as in conventional flash ADC. The proposed flash ADC uses less comparator as compared to conventional flash ADC. Simulation on Cadence analog tool (Virtuoso) results show that power and area (in the terms of transistor count) of designed flash ADC is considerably less as compared to conventional flash ADC.

Keyword: Flash ADC, Multiple Selection method, sample and hold circuit, Cadence tool

I.INTRODUCTION

ADC plays a very important role between analog and digital signals. Almost all the applications needs digital output in this modern era of digitization because it is easy to store and understand it. Digital imaging systems commonly use analog-to-digital converters in digitizing pixels. Radar systems commonly use analog-to-digital converters to convert signal strength to digital values for subsequent signal processing. Many other in situ and remote sensing systems commonly use analogous technology.Flash ADC suits most of the application that requires medium to high conversion time and resolution but the problem with flash ADC is that it requires large area.

This paper presents the design of flash ADC using multiple selection method. This paper is organized as follows. A brief introduction about flash ADCs is given in Section I. In section II, the conventional ADC architecture has been discussed. In section III, the designed flash ADC with its components has been explained briefly. In section IV, Simulation results have been given. Finally, conclusion is given in section V.

II. CONVENTIONAL FLASH ADC

Traditional flash ADC architecture uses 2^Nresistors and 2^N-1 comparator. All comparators will work in parallel, which will cause high power consumption. The component count of a flash ADC grows exponentially with resolution. Therefore, the area and power consumed by the ADC circuit increase exponentially with resolution [10].

III. DESIGNED ADC ARCHITECTURE

The four bit flash ADC using multiplexer consists of one mux 2:1, three mux 4:1, six comparators and logic circuitry. The architecture of the designed ADC is shown in fig.1.

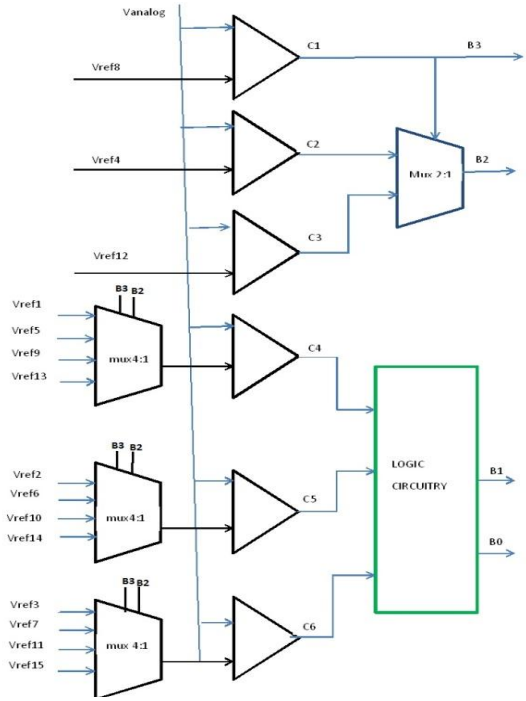

Fig.1. Block Diagram of four bit Flash ADC using Multiplexer

The major disadvantage of the conventional flash ADC is its high chip area, high power consumption and high input capacitance. Generally, this type of architecture uses $2^{(N-2)}$ +2 comparators instead of 2^N-1 comparators which are very less in number, in addition to overhead of logic circuitry.

Main components of this ADC include Sample and Hold circuit, Comparator, Multiplexer 4:1, Multiplexer 2:1 and logic circuitry. Flow diagram for its operation is shown in Fig. 2.

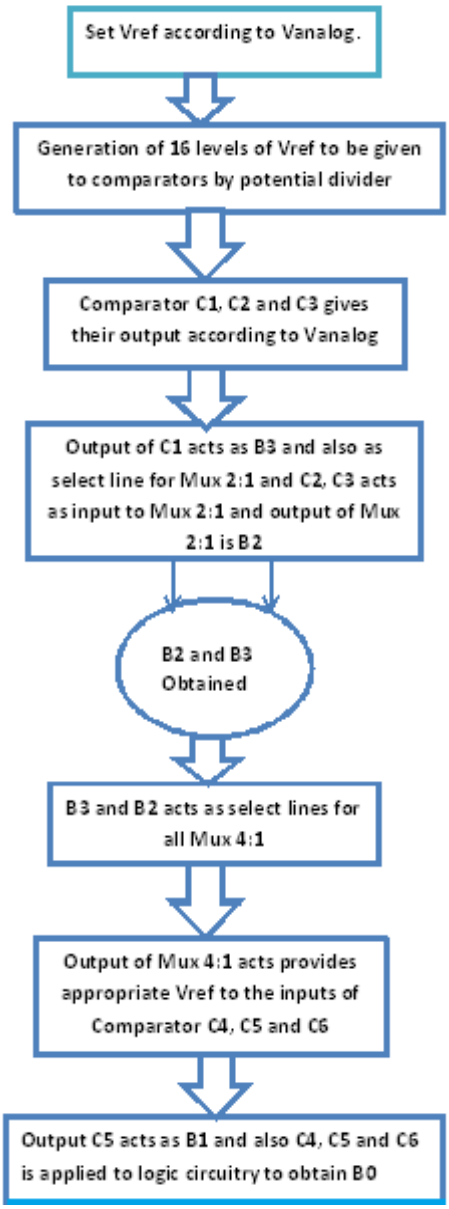

Fig. 2:Flow Diagram for the operation of Flash ADC using Multiplexers

Analog input given to the ADC through sample and hold circuit. This input goes to the non- inverting input of comparator C1, C2 and C3 and inverting inputs are connected to 8Vref/16, 4Vref/16, and 12Vref/16 respectively to generate the MSBs. the outputs of comparators are used to control the output of Multiplexer 2:1. Thus, B3 and B2 are decided by the outputs of comparators C1, C2, C3 and Multiplexer 2:1.

TABLE I
Outputs B3 and B2 Corresponding to Vin

C1 acts the select line and Output bit B3.
C2 and C3 are the inputs of Mux.
B2 is the output of Mux.

Vin	C1	C2	C3	B3	B2
0 <Va<Vref4	0	0	0	0	0
Vref4<Va< Vref8	0	1	0	0	1
Vref8<Va<Vref12	1	1	0	1	0
Vref12<Va<Vref16	1	1	1	1	1

The outputs B3 and B2 are connected to select line of each of the Multiplexer 4:1, this leads to appropriate Vref at the input of comparator C4, C5 and C6. The outputs of the comparator C4, C5 and C6 decide the output binary bits B1 and B0.

The design of the flash ADC uses six comparators and some extra overhead of multiplexers instead of fifteen comparator, sixteen EXOR gates and encoder of conventional flash ADC. Thus, it decreases area and power consumed.

VARIOUS COMPONENTS

The following section discusses the various components used in the designing of flash ADC using multiple selection method. Components include comparator, differential amplifier, current mirror, Mux design and logic circuitry used.

COMPARATOR

Comparator consumes significant power in ADC circuits but plays very critical role in the designing. The parameters such as propagation delay, power consumption, input offset voltage, and input range of comparator decides the important parameters of flash ADC.

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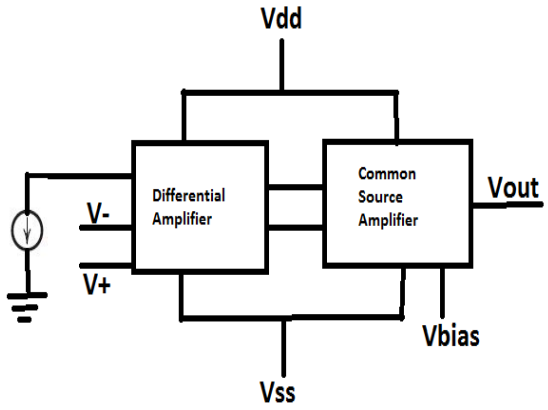

Fig. 3: Block diagram of Comparator

The number of comparator increases as the number of bits increases, a result the power consumed and area also increases exponentially. The noise generated at high frequencies in the comparator is considerable.

Block diagram of comparator used in designed ADC is shown in Fig.3. As the CMOS technology consumes less power so comparator used in flash ADC is designed using CMOS technology so that it consumes minimum power. The two stages of comparator are (i) Differential amplifier (ii) Common source amplifier

(i).*DIFFERENTIAL AMPLIFIER*

The active loaded MOS differential amplifier schematic is shown in fig 3. It consists of two matched transistors, NM0and NM1, whose sources are joined together and biased by a constant-current source *I*. The constant current source is usually implemented by a MOSFET circuit of current mirror. Generally, each drain of differential amplifier is connected to the positive supply through a drain resistance, but active (current-source) loads are employed here. Whatever type of load is used, it is essential that the MOSFETs not enter the triode region of operation.

Transistor NM0 and NM1 are biased using constant current source which has been implemented using a current mirror circuit i.e. source of NM0 and NM1 are connected to each other and current source is applied to them. Current mirror has been implemented using NM2 and NM3. PM0 and PM1 mirror.are used as an active load also acts as a current

Differential gain = $\frac{Vout}{V1-V2}$ and $A_d = \frac{1}{2} g_m r_0$

Where $A_d$represents the differential gain of the differential amplifier, $g_m$denotes the transcendence of MOS transistor and r_0 denotes the output resistance of MOS transistor.

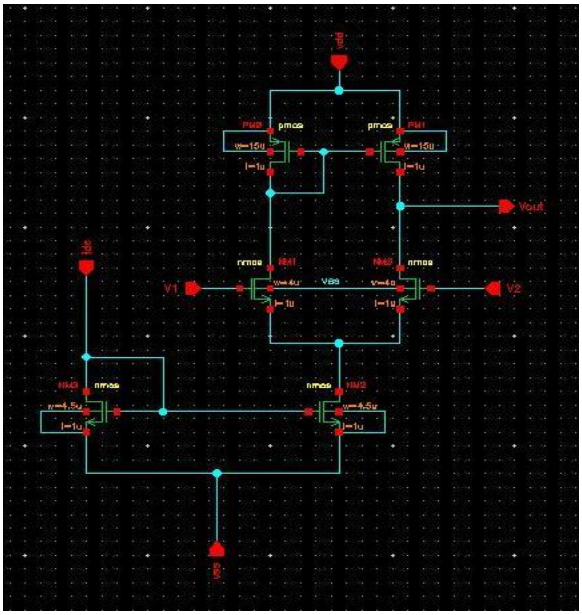

Fig.3. Circuit Diagram of Differential amplifier

(ii).*COMMON SOURCE AMPLIFIER*

The Schematic of the Common Source Amplifier is shown in the fig. 5

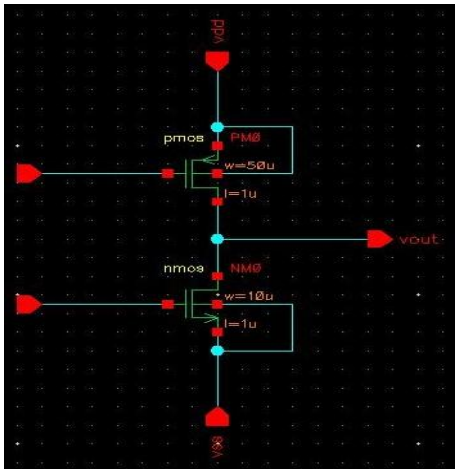

Fig.5. Schematic of Common Source Amplifier

As shown in the schematic, the input to CS amplifier is given between source and gate terminal of NMOS

and output is taken between source and drain of NMOS. PMOS acts as active load and input given to it keeps the amplifier in saturation region. The input of CS amplifier is the output of differential amplifier and gain of the CS amplifier is such that if the difference between V1 and V2 applied to the differential amplifier is positive then output saturates to the $+V_{DD}$ otherwise $-V_{DD}$.

B. MUX 2:1

CMOS transmission gates provide an efficient way to build steering logic. Steering logic circuits are circuits that route data inputs to outputs based on the settings of control signals. Transmission gates implementation is shown in fig. 6 and Schematic of mux 2:1 is shown in fig. 7.

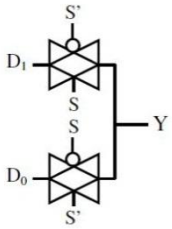

Fig.6. Mux 2:1 using Transmission gate

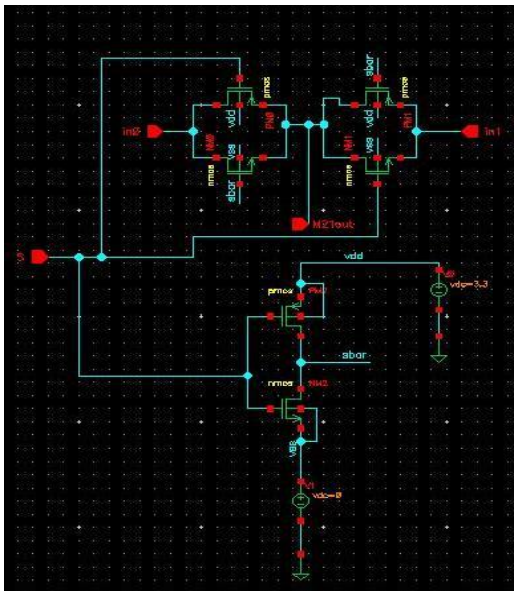

Fig.7. Schematic of Mux 2:1

The main advantage of using transmission gate in Mux implementation is that the number of the transistor used has reduced significantly. This has been observed that the number of transistor is reduced by 3.3 times as compare to umber of transistor in mux 2:1 designed with logic gates.

C.MUX 4:1

Mux 4:1 has been implemented using transmission gates. It has been implemented using mux 2:1 as show in the fig. 8 and fig. 9.

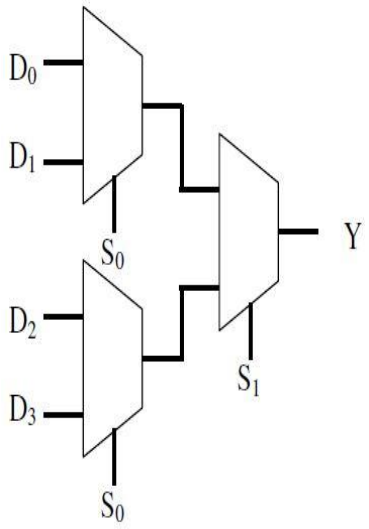

Fig.8. Symbol Schematic of Mux 4:1

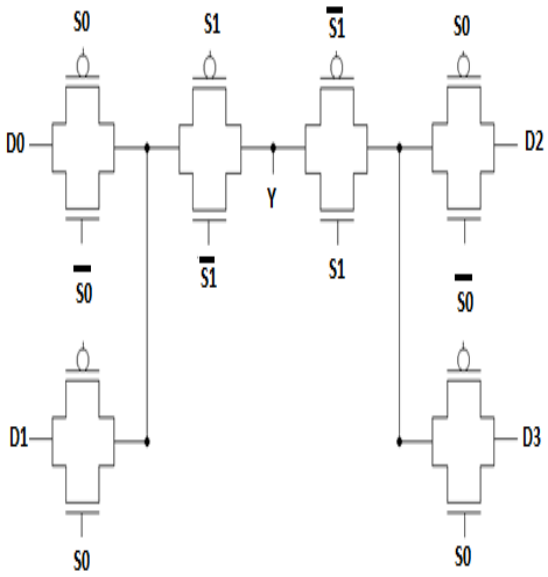

Fig.9.Mux 4:1 using Transmission gate

This has been observed that the number of transistor used in mux 4:1 using transmission gates are 35% less than the mux 4:1 designed with logic gates.

D. LOGIC CIRCUITRY

The logic circuitry used in the architecture of the proposed ADC implement the following truth table to generate the B0 bit of the binary output.

Table II
Truth Table to Generate B0

C3	C4	C5	B0	B1
0	0	0	0	0
1	0	0	1	0
1	1	0	0	0
1	1	1	1	1

Logic circuitry used to generate the B0 bit of the binary output with C4, C5 and C6 as inputs are shown in the fig. 10.

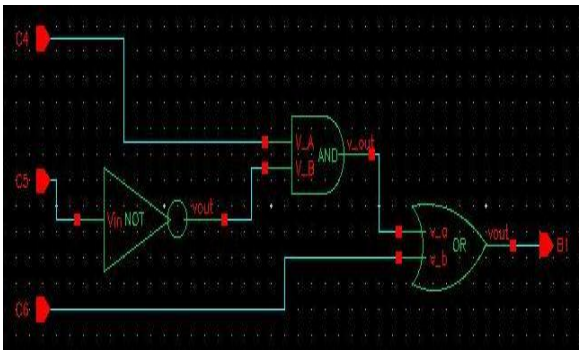

Fig.10.Logic circuitry used to generate the B0

IV.SIMULATION AND EXPERIMENTAL RESULTS

Simulation of four bit designed Flash ADC using multiplexers have been achieved with Cadence Analog tool using 180 nm technologies at schematic level. For the simulation purpose, an input analog signal of 1.2 V, 1 KHz with a DC level of 1.2 V has been used. Transient analysis has been done for a period of 1ms. The sampling period used is 64µs. In the outputs results Vanalog, Vhold and B1, B2, B3, B4 has been plotted. Simulation results have been shown in fig 11. The average power consumed and number of transistors used has been shown in table III.

TABLE III
Power consumed and area

Arch. / Spec	**Multiple selection flash ADC(Designed)**
Technology	GPDK 180nm
Power Supply	3.3V
Resolution	4 bit
Input Analog Range	0~2.4V
Power Consumed	6.40mW
Area (in terms of transistor count)	122

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V. CONCLUSION

The proposed flash ADC consumes less power and less area. The flash ADC designed with multiplexer consume 6.40mW power and the number of transistor used in flash ADC designed with multiplexer is 122 Thus, this designed ADC is both power and area efficient.

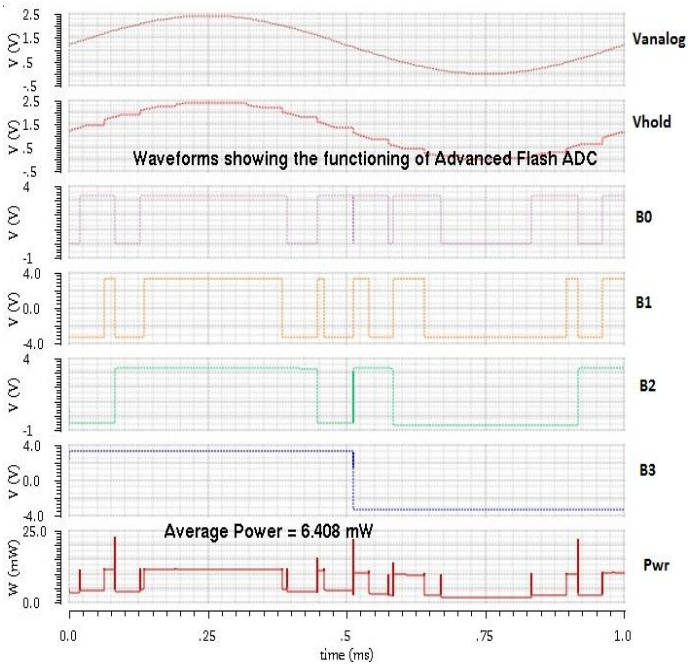

Fig.11. The Simulation results of Flash ADC using multiplexer (Vsin= 1.2V at DC 1.2V)

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