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IMPLEMENTATION OF TAP CONTROLLERFOR NON-JTAG DEVICES

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ABSTRACT

Testing of Integrated Circuits using Test Access Port Controller is a widely implemented issue in recent years. The output generated using the TAP Controller is a fixed test case which requires all the test cases to prove the correctness of the circuit. In the proposed work the device is tested using fewer test cases, to prove the correctness and results in a low testing as compared to the previous approach. The test cases generated in the proposed approach are random and device must be tested on these test cases. The Simulation results of the implemented approach are shown in the results section.

Keywords: Test Access Port Controller, TAP testing, Single Port RAM

1.INTRODUCTION

The IEEE 1149.1 tap controller is probably one among the foremost wide used circuits found in business IC chips. The tap controller could be a major element of the IEEE 1149.1 commonplace whose main objective is to facilitate board-level testing through boundary scan. However, the tap controller is usually used for coordinative check activities as well as scan check at the board-level, RAM BIST, logic BIST, place of faulty chips, etc. There are publications suggesting the utilization of the check access port for facilitating testing of embedded cores in an exceedingly system on- a-chip Bhattacharya ninety eight, Whetsel 97, Whetsel 01. The tap controller is beneficial for non-testing functions. for instance, the boundary scan port is used for loading configurations onto programmable logic circuits like Field Programmable Gate Arrays. The boundary scan port can even be used for recovery of dependable systems from failures. At a stop, the logic values of the interior bistables of the system are scanned out and keep in safe storage protected by error correcting codes. Upon error detection throughout rollback recovery, the check pointed state is scanned into the system bistables victimization the boundary scan port.It is clear from the higher than discussion that the tap controller, despite its little size, plays a really vital role in VLSI systems. If the tap controller fails, then the higher than mentioned functions won't be performed correctly; therein situation, the check engineer could pay plenty of your time and energy suspecting that one thing else has gone wrong once the faulty tap controller is that the main wrongdoer – so, we'd like to envision whether or not the tap controller in an exceedingly chip is functioning properly or not. this is often true throughout production check at the IC-level and also the board-level. If there's method yield downside such the tap controller gets affected, then it becomes terribly tough, if not not possible, to perform initial rectify. Hence, it's vital to

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check the tap controller totally before it's used for debugging functions.

Moreover, if the tap controller is employed throughout system operation, we tend to should certify that the tap controller is truly operating properly. The question that involves mind is – "how can we check these tap controllers throughout production check, board-level check and once it's used throughout system operation?" in an exceedingly testing technique for the tap controller has been according. This method was employed in AT & NT's trip the light fantastic toe program to get check sequences for the tap controller. However, the check length for this method is extremely long. for instance, for a chip with two hundred I/O pins, Dahbura's technique can want a sequence of length 4234 to check the tap controller.

For a module with one,000 to 1,500 I/Os, the check length of this method are going to be over twenty,000 associate degree for an IC with three,000 I/Os [NEC 98] the check length are going to be around forty,000. Moreover, for a system-on-a-chip with check wrappers containing a tap controller for every core, every tap controller can want totally different sequence and also the responses from every tap controller are going to be different. During this paper, we tend to describe techniques to style tap controllers such that:

(1) Associate degree complete check of the tap controller is simply performed throughout production, board-level and system-level tests;

(2) Elaborated response knowledge from the tap controller check doesn't have to be compelled to be keep within the tester and compared

(3) It's simple to spot chips

The TAP Controller

The IEEE-1149.1 commonplace defines a typical interface for JTAG management, referred to as the check Access Port. the tap interface could be a set of output and input pins that permits serially inserting and extracting internal register knowledge, and at constant time to manage the embedded JTAG controller's state. Since the info is processed serially, the registers that may be scan or written through the tap area unit organized in an exceedingly link fashion. This structure is termed a boundary scan chain. Chains aren't certain to one physical device. The tap interface was designed such multiple ICs that support JTAG could also be connected along to make compound chains.

Figure 1 shows the 16-state FSM for TAP controller. The value on the state transition arcs is the value of TMS. A state transition occurs on the positive edge of TCK and the controller output values change on the negative edge of TCK. The TAP controller initializes the Test-Logic-Reset state. While TMS remains a 1 (default value), the state remains unchanged. In the Test-Logic-Reset state and the active (selected) register is determined by the contents of the Hold section of the Instruction register. The selected register is either the Identification register, if present, else the Bypass registers.

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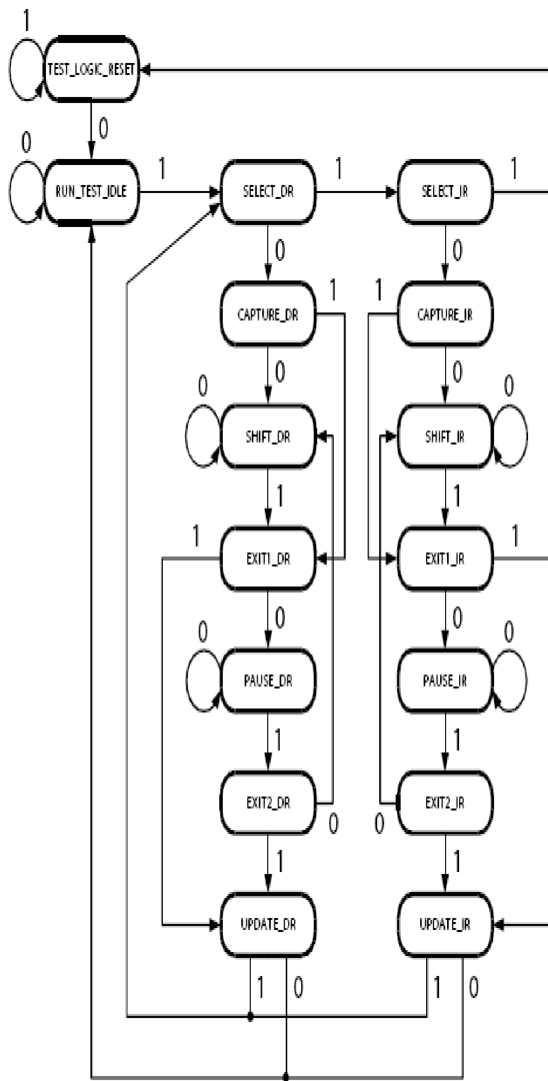

Figure: 1. TAP State Machine

Pulling TMS low causes a transition to the Run-Test/Idle state (Awake and do nothing state). Normally, want to move to the Select IR-Scan state ready to load and execute a new instruction.

TAP Signals

The signals proposed in an exceedingly tap interface. The TMS, TDI, TDO and TCK signals are area unit obligatory. The TRST signal is no obligatory since it's continually attainable to soft reset the tap machine continuance 5 ones into the TMS pin.

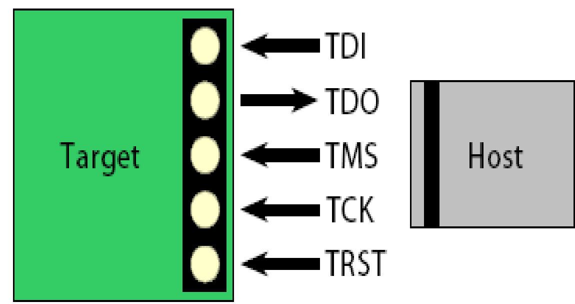

Figure: 2. TAP Signals

TAP Association

Originally, because the JTAG name implies, the interface was formed to perform electrical property tests between parts in an exceedingly board; but in time developers found alternative uses for it. This is common to use the tap to at the start program the Flash recollections of a board so as to bootstrap it, and a few chemical element vendors use the interface to implement embedded In-Circuit Emulators for his or her processors

2.RELATED WORK

In this paper, Bhattacharya et al. [1] proposed issue of handling multiple embedded 1149.1- compliant tap controllers in an exceedingly 1149.1- compliant IC, has received vital attention, in recent times. The class-conscious tap design, and developed by this author, provides a scientific answer to the present downside, by permitting multiple embedded TAP's to share one set of 1149.1-specified take a look at pins on the IC.

In this paper, Mitra et al. [2] proposed a look at Access Port controller could be a vital circuit gift all told IC chips that area unit compliant with the IEEE 1149.1

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Boundary Scan customary. Though the most purpose of boundary scan is to facilitate board level testing, it's conjointly used for several different testing and non-testing functions e.g., memory and logic BIST, wrappers to alter embedded core take a look at, programming

In this paper, Nadeau-Dostie et al. [3] proposed IEEE-1149.1 customary defines a standard interface for JTAG management, known as the take a look at Access Port. the tap interface could be a set of output and input pins that enables serially inserting and extracting internal register information, and at an equivalent time to regulate the embedded JTAG controller's state.

In this paper, Abramovici, et al. [4] proposed HTAP design needs Associate in Nursing increased version of the 1149.1-specified tap – selected the Snoopy tap – within the top-ranking of the look hierarchy, that handles 1149.1-specified tap functions for the non-TAP’ed components of the IC, and performs arbitration of the shared IC pins between multiple embedded taps.

In this paper, Dahbura et al. [5] proposed the required signals of the JTAG serial-test bus – take a look at clock, take a look at mode choose, take a look at information input, and take a look at information output is connected from the TBC to a target device while not extra logic. this is often done as a series of IEEE customary 1149.1-1990 boundary-scannable parts that share an equivalent serial-test bus.

In this paper, McCluskey et al. [6] proposed for TBC operation beneath the management of a bunch microprocessor/microcontroller via the 5-bit address bus and therefore the 16-bit read/write information bus. Browse and write strobes area unit enforced specified the vital host-interface temporal order is freelance of the TCKI amount.

In this paper, Mitra, S et al. [7] proposed an overview of the IEEE 1149.1 Boundary Scan customary and therefore the specification of the tap controller. In Sec. 3, we have a tendency to describe our technique for planning simply testable tap controller circuit mistreatment synchronic error detection. It describes the benefits of mistreatment the CED-based tap controller style.

In this paper, Nadeau-Dostie et al. [8] proposed testing technique for the tap controller has been reportable. This method was utilized in AT&T’s trip the light fantastic program to get take a look at sequences for the tap controller. However, the take a look at length for this method is extremely long.

In this paper, Touba et al. [9] proposed TAP controller DFT technique is to scan the tap controller and use standard Automatic take a look at Pattern Generator programs to get tests. However, this method isn't applicable once the tap controller itself is employed for scanning functions like wrappers for embedded cores, throughout BIST, unless additional I/O pins area unit dedicated for scanning the tap controller.

In this paper, Bhattacharya et al. [10] proposed second instruction register to the SNTAP, selected Snoopy-Mode IR or SNIR, that is chosen because the IR, as long as SNTAP remains in an exceedingly snoopy state. In different words, once the SNTAP is within the snoopy mode, any

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instruction scan – presumptively meant for the embedded tap that's presently connected to the take a look at bus.

In this paper, Maunder et al. [11] proposed an SNTAP that may be waken up mistreatment implicit instruction-driven mechanism is devised, that doesn't need the SNIR: this variant of the SNTAP is selected SNTAP-I2, whose design is displayed. During this style, a counter opted Cnt-Sn-Sh-IR is introduced within the SNTAP controller – that replaces counter C0 in Figure four, in an exceedingly manner of speaking.

In this paper, Whetsel et al. [12] proposed CED approach is to duplicate the tap controller FSM implementation and compare the first outputs and therefore the flip-flop outputs. Within the presence of one fault in one among the 2 copies, it's warranted that the circuit can manufacture correct outputs or indicate error once incorrect outputs area unit created

3.PROPOSED METHODOLOGY

The IEEE 1149.1 is implemented using the state machine which shows various states of the Test Access Port Controller along with the Linear Feedback Shift Register (LFSR). LFSR is used to generate the random address in which the data is written in the Memory. A four bit LFSR is used to generate these addresses which is implemented using the exclusive –or gates. The state machine of TAP controller also outputs the data which must be written into the Single Port RAM (Design Under Test). The output of the DUT is feed back to the TAP Controller for verification. Figure 3 shows the implementation block diagram of the TAP Controller along with the DUT.

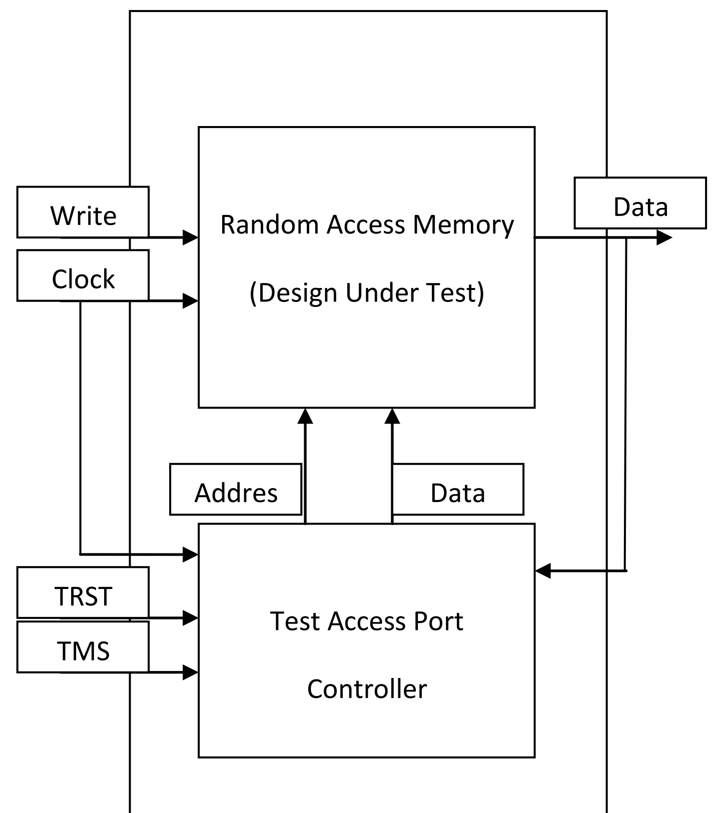

Figure 3: Implementation Block Diagram

4.RESULTS AND DISCUSSIONS

The Proposed model of TAP Controller and the DUT is implemented using the XILINX ISE in VHDL language. The FPGA device used for the synthesis and the simulation is SPARTAN 6 and the software used for simulation is XILINX ISim. The resources used for the whole simulation and the delay are shown in Table 1.

Table 1: Logic utilization of Xilinx Spartan 6

Logic Utilization	Used	Available
Number of Slice Registers	15	4800
Number of Slice LUTs	24	2400
Number of fully used LUT-FF pairs	15	24
Number of	1	16

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BUFG/BUFGCtrls		
Number of bonded IOs	12	102

The delay calculated using the Xilinx device is 3.597 ns. The top module diagram is shown in figure 4. The Simulation results using the ISim Simulator is shown in figure 5. The waveforms for each input and output along with the top module signals are shown in figure.

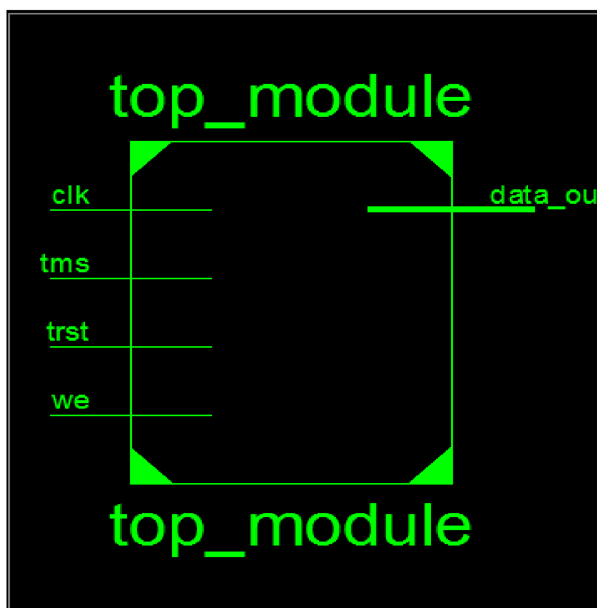

Figure 4 Top Module of the Implemented Design

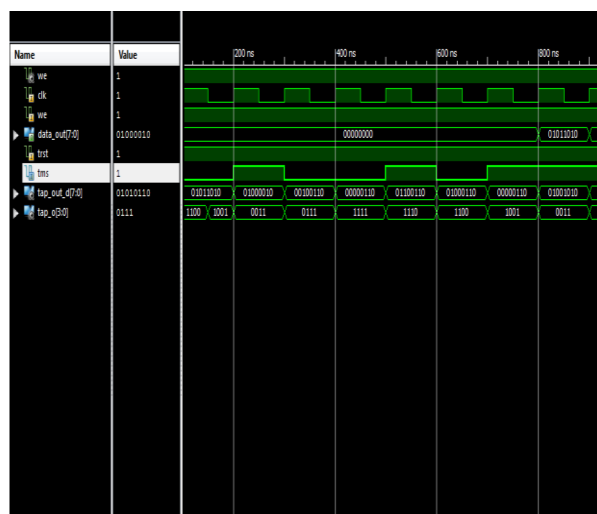

Figure 5 Simulation Results of the Proposed Approach

5.CONCLUSION

The above result shows the implementation of the TAP controller and its use for testing a Single Port RAM. From the Simulation results it is clear that the data written in the memory is accessed using the addresses in which the data is written. The data is verified and tested successfully by the TAP Controller. In future various other devices must be tested using the controller.

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