ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 9, September 2015

Design of Low Power 7T SRAM Cell Using Low-Vth Transistor

G.Surekha, Dr.N.Balaji, Dr.Y.Padma Sai, R.Prashanth Kumar,

***Abstract*— This paper is mainly focusing on reducing total power consumption of Static Random Access Memory (SRAM).The SRAM is a memory device and is widely used in various VLSI chips for low power consumption. SRAM serves as external cache memory and is interfacing between main memory and internal cache. This paper discover a new technique to reduce static power dissipation of conventional 6T SRAM cell using low threshold voltage (V_{th}) transistor. The additional NMOS device is added between power supply and pull up device to apply reduced power supply (V_{DD}) in standby mode and send maximum V_{DD} in active mode to 6T SRAM cell. To do this, gate of extra nmos is connected to word line of SRAM and substrate is biased to V_{dd}. Cadence Virtuoso 180nm Technology EDA tool is used for simulation. The transient analysis for read, write and hold operations of conventional 6T, Proposed 7T SRAM are performed and static power dissipation, total power consumption is calculated using Cadence Virtuoso EDA tool.**

***Index Terms*— 6T SRAM, static power dissipation, substrate, Low threshold voltage, NMOS**

INTRODUCTION

The demand for battery operated applications is increasing. these days. So methods for reduction of the power consumption of the memory has received significant interest

***Manuscript received sept , 2015*.**

G.Surekha *Associate professor* ,GRIET, Hyderabad, Telangana, India.

Dr.N.Balaji *professor* JNTUK University College of Engineering, Vizianagaram, Andhra Pradesh, India.

Dr.Y.Padma Sai *professor* VNR Vignana Jyothi Institute Of Engineering And Technology. Hyderabad, Telangana, India.

***R.PrashanthKumar**,M.Tech (VLSI)* Gokaraju Rangaraju Institute Of Engineering & Technology, Hyderabad, Telangana, India

SRAM cells are preferred for many applications because of its high speed and robustness.

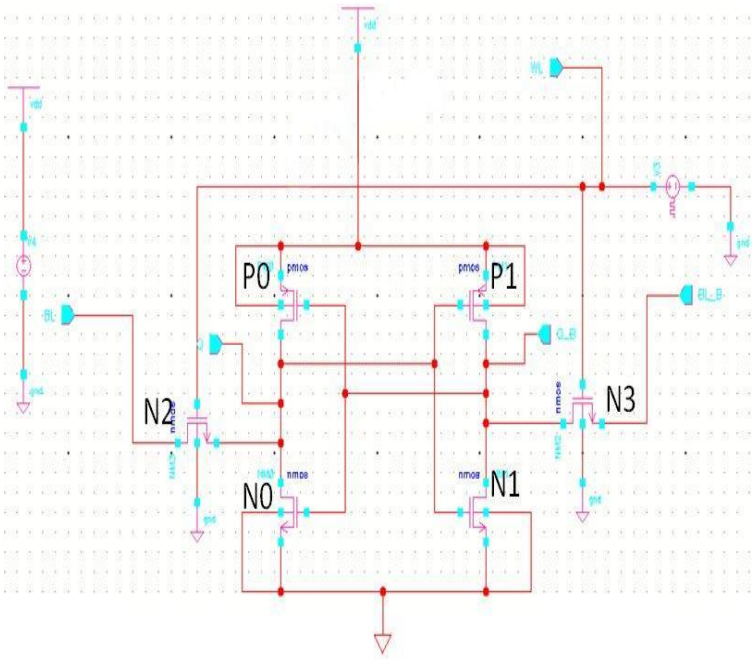

Figure 1: 6T SRAM CELL

The figure 1 shows conventional 6T SRAM Cell consists of six transistors. The two inverters N0, P0 and N1,P1 are connected in feedback loop and output of these two inverters are Q and Q_B.The data basically stores in Q,Q_B and they are complimentary to each other. The transistors N2,N3 are pass transistors used for accessing the data from the Q,Q_B. So transistors N2,N3 are called as access transistors. Word Line(WL) is connected to gates of two access transistors and BL,BL_B are given to source or drain of access transistors.

Basically SRAM operates in three modes. Which are

1) Standby Mode 2) Read Mode 3) Write Mode

In standby mode no write or read operation is performed which means the circuit is idle, in read mode the data is read from output node to the bit lines and the write mode the data or contents are updated.

The three different modes work as follows

Standby Mode:

If the word line WL is low '0' then the access transistors N2,N3 will be turned off and the BL,BL_B are disconnected from the cell. The cross-coupled inverters will continue the data which it had previously, in this mode the current drawn from supply voltage is called standby or leakage current.

Read Mode

In read mode, bit lines BL,BL_B are Precharge to maximum supply in the circuit(V_{dd}) and during Precharging the world line should be turned off. After completion of Precharging word line will be turned on. Assume that the 1 is stored at Q and '0' at Q_B. So no current flows through N0 and some current is flowing through N1.There is no voltage difference between Q and BL, hence there is no change at BL,but BL_B gets discharged due to some small voltage difference between Q_B and BL_B. This small voltage difference between BL_B and BL gets amplified by sense amplifier that pull the data and produce the output.

Write Mode

In write mode, suppose if we want to write a '0' at the storing node Q, we would apply a '0' to the BL means setting BL to '0' and BL_B to '1'.After setting the bit lines, WL is then asserted.

I. LEAKAGE CURRENT MECHANISM IN SRAM

There are mainly two important leakage currents in SRAM. They are

1) Sub threshold leakage current
2) Gate tunneling leakage current

Sub threshold leakage current

Sub threshold leakage is the drain-source current of a transistor when the gate-source voltage is less than the threshold voltage. Sub threshold leakage flows when the transistor is operating in the weak inversion region. The sub threshold current depends exponentially on threshold voltage, which results in large sub threshold current in short channel devices. To reduce the sub threshold leakage of an SRAM cell, one can increase the threshold voltage of all or some of the transistors in the cell.

Gate tunneling leakage current

Electrons (holes) tunneling from the bulk silicon through the gate oxide into the gate results in gate tunneling current in NMOS (PMOS) transistor. Gate tunneling current is composed of three major components one is gate to source, gate to drain overlap current and gate to channel current, part of which goes to source and the rest goes to drain and gate to substrate current.

6T SRAM Cell with Leakage Currents When WL=0, Q=0 shown in figure

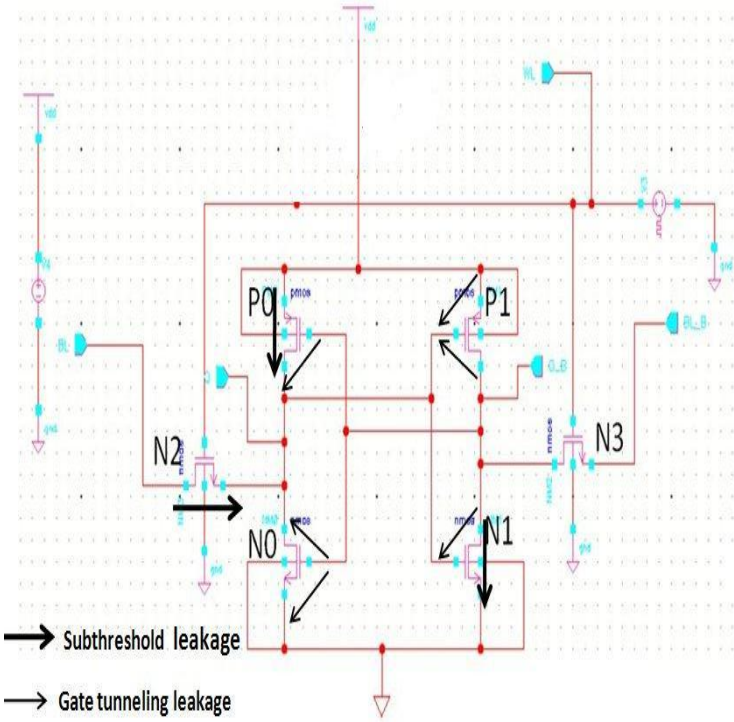

Figure 2: Leakage currents in SRAM CELL

Generally leakage current flows when the device is stand by mode. SRAM is standby mode when WL=0.When word line and storage node(Q) is zero means transistors N2,N3,P0,N1 are off then sub threshold leakage is flows through them. The sub threshold current is dominating all leakage currents. Aim of this work is reducing the sub threshold leakage to further reduce static power dissipation.

Many techniques are found for reducing this sub threshold leakage current. These are mainly Stacking Effect, Multi-threshold CMOS(MTCMOS),Variable threshold CMOS(VTCMOS) etc. Placing the transistors are in series by making width of them half is known as stacking effect. When series transistors are in off state, sub threshold leakage will flow through them and small voltage will be generated at sources of all series transistors. Then gate to source voltage becomes negative and gate to source voltage and sub threshold current are inversely related and then leakage will be reduced.

In MTCMOS technique two additional transistors are placed at the top and bottom of the cell with increased threshold voltage.Subthreshold leakage current is

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 9, September 2015

inversely proportional to threshold voltage (V_{th}).So during standby mode small leakage current flows through high V_{th} transistors compared to low V_{th} transistors. Due to series connection of high and low V_{th} transistors, result of them will follows the current, which is flowing through high V_{th} transistors. In VTCMOS technique, threshold voltage will be varied by substrate biasing.

II. PROPOSED METHOD

The proposed 7T SRAM cell consists of seven transistors five NMOS from N0-N4 and two PMOS from P0-P1 as shown in Figure

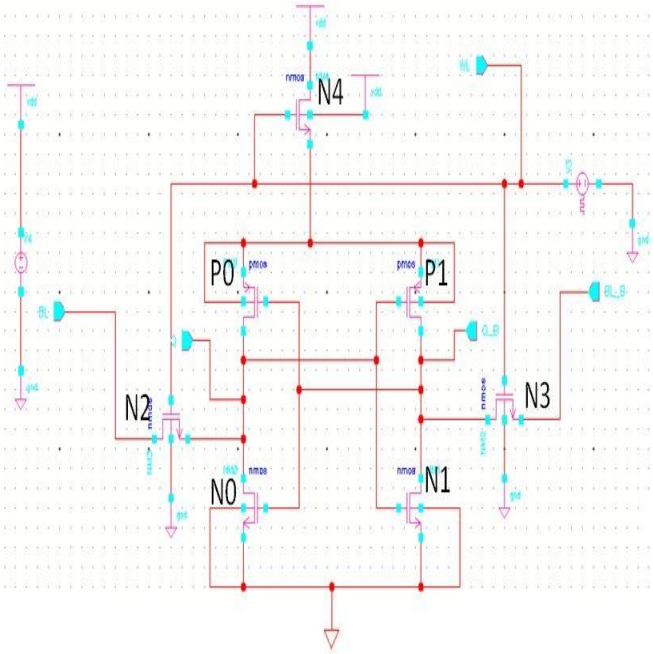

Figure 3: proposed 7T SRAM Cell

In Proposed 7T SRAM Cell, during active mode a nearly full supply voltage V_{DD} is applied to SRAM but during inactive mode or in standby mode a reduced supply voltage of V_D is applied using substrate biasing. If the transistor P1 is in on state, the drain voltages of transistors N0 and N1 are also at V_D, the value of V_D is less than V_{DD}. So The gate leakage currents of transistors N0 and N1 get reduced because gate leakage currents is depend on the gate-source and gate-drain voltage of transistor and here the gate-drain voltage of N1 and gate-source voltages of NO are reducing. Also a decrease in drain voltage of transistor N3 gives a less gate leakage current through it.

Methodology

Total power dissipation in CMOS circuits is

$P=P_{dynamic}+P_{static}$ ……..(1.1)

$P_{dynamic}$ = Dynamic power dissipation

P_{static} = Static power dissipation

$P_{dynamic}$ is the power dissipation when the circuit is working or in active mode and P_{static} is the power dissipation when the circuit is stand by (not in active) mode.

$P_{dynamic} = 1/2*\alpha*C_L*V^2_{dd}*f$……(1.2)

α=Switching activity of transistors

C_L = Load capacitance

V_{dd} = supply voltage

f = operating frequency

$P_{static}= V_{dd}*(I_S+I_G+I_D)$ ……(1.3)

$I_S=f(V_{dd},V_{Th},S,T)$ ……..(1.4)

I_S = Sub threshold Leakage Current

I_G = Gate leakage current

I_D = Drain junction leakage

V_{th} =Threshold voltage

S = Size of gate

T =Temperature

As can be seen from Eq (1.2), the power dissipated can be reduced by reducing either the clock frequency f or the load capacitance, C_L , or the rail voltage, V_{DD} , or the switching activity parameter, α. Reducing the clock frequency is the easiest thing to do, but it seriously affects the performance of the chip. Another method to reduce the dissipated power is to lower the load capacitance, C_L . But this method is more difficult than the previous approach because it involves conscientious system design, so that there are fewer wires, smaller pins, smaller fan-out, smaller devices etc.

As can be seen from Eq (1.3) Sub threshold leakage current is strongly depends on supply voltage. If supply voltage is reduced , then there will be lot of reduction in leakage current.

Proposed Methodology

Word line of SRAM is connected to gate of extra NMOS transistor and substrate (bulk) is given to V_{DD} as shown below.

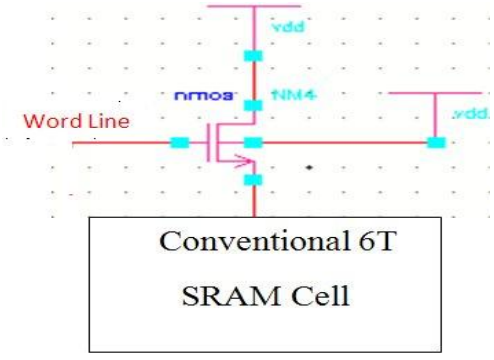

Figure 4: Proposed Methodology

In Active mode:

WL=1(V_{DD})

Then NMOS is switched on, but the NMOS will not transmit complete V_{dd} due to threshold voltage drop in the NMOS. In active mode maximum power supply is given to cell. From the voltage transfer characteristics between substrate biasing voltage and threshold voltage shown in figure 5 shows that, threshold voltage of NMOS can be reduced if positive supply voltage is given to the substrate.

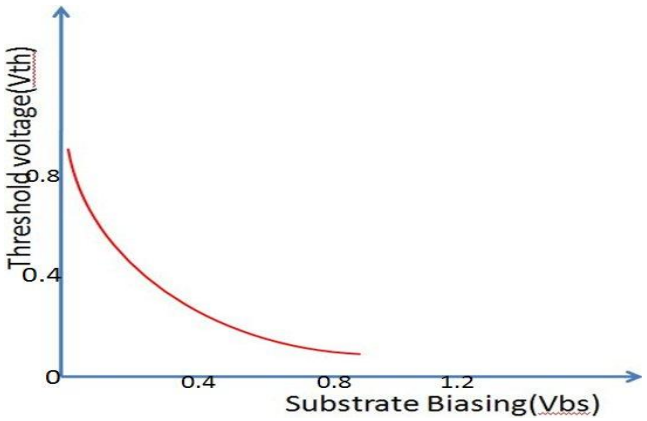

Figure: 5 Voltage transfer characteristics Vth & Vbs of NMOS

In order to give full supply voltage during active mode, threshold voltage of NMOS is reduced using farward biasing of substrate.

Equations

$$V_{th} = V_{th0} + \lambda\left(\sqrt{|2\varphi_f - V_{BS}|} - \sqrt{|2\varphi_f|}\right)$$

……(1.5)

V_{th} = Threshold voltage when substrate bias is present

V_{BS} = Base - to - Source substrate bias

$2\varphi_f$ = Surface potential

V_{tho} = Threshold voltage for zero substrate bias

λ = Body effect parameter

When

gate voltage (V_G) = drain voltage (V_D) =power supply (V_{dd})

then the source voltage V_S is

$V_S = V_{dd} - V_{Th}$ ……..(1.6)

If V_{Th} is reduced, maximum supply voltage will be passed to cell through source voltage V_S in active mode.

it can also be explained using drain current equation (1.7)

$$i_D = \frac{1}{2}k_n\left(\frac{W}{L}\right)\cdot(V_{GS} - V_{TN})^2$$

……..1.7

Equation 1.7 states, NMOS is perfectly switched on by reducing threshold voltage (V_{TN}) and transmit nearly full voltage to SRAM Cell.

In Standby mode

WL=0

NMOS is off. In off state, sub threshold leakage current flows through the NMOS. Due to this low sub threshold voltage (source voltage) will be generated.

SRAM is volatile memory i.e once power supply disconnected from the cell ,the data which is stored in the cell will also be lost. The low generated source voltage will not be sufficient for retention of data. So source voltage is increased by giving supply voltage to substrate (bulk).This will decrease the threshold voltage of NMOS device as can be seen from above Eq (1.6). This generated source voltage will be sufficient for the retention of data.

Equation

$$I = I_0 \exp\left(\frac{(V_{gs} - V_{th})}{nV_T}\right)\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right)$$

$$V_T = kT/q$$

……..1.8

V_{th} = Threshold voltage

V_T = Thermal voltage

Sub threshold current (I_{Sub}) α e^{-Vth}

Source voltage (V_S) α I_{Sub}

Above equations states that the source voltage will be increased by reducing threshold voltage.

III. SIMULATION AND RESULTS

Precharge circuit, write enable control signal and sense amplifier is used for the simulation of conventional 6T SRAM Cell and Proposed 7T SRAM Cell.

Precharge circuit

Precharge circuit is used to charge BL and BL_B to maximum supply voltage in the circuit.

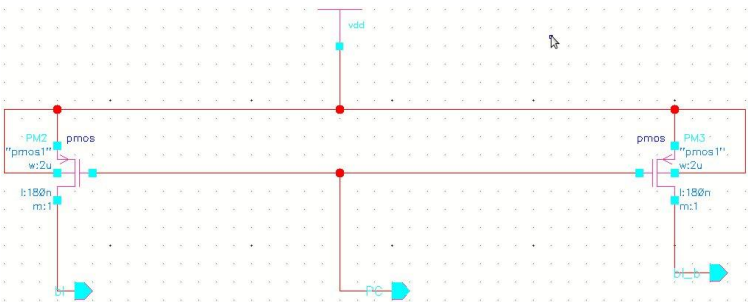

Figure 6: Precharge circuit

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 9, September 2015

The pin PC is used to controls the circuit. PC is enabled before starting of read operation and is disabled during read operation.

Sense Amplifier

Several types of Sense amplifiers are being used in various applications. In this paper differential type of sense amplifier is used. Main function of Sense amplifier is to amplify the voltage difference between BL and BL_B during read operation.

The differential type of sense amplifier is shown in fig.7

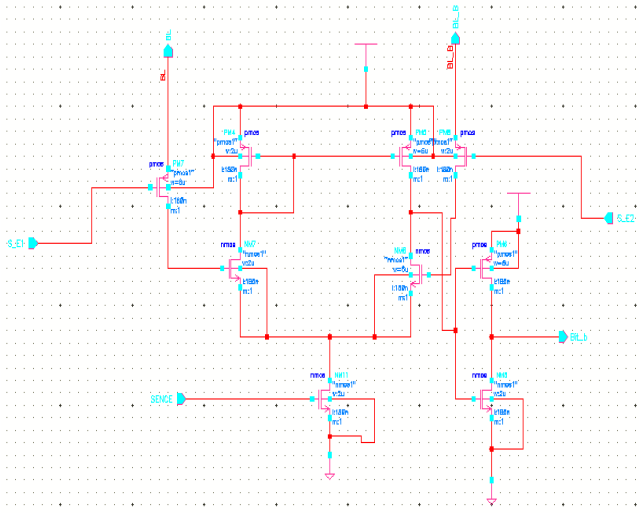

Figure 7: Sense amplifier

The pin Sense is used to controls the sense amplifier. Sense is enabled during read operation and disabled during write mode and hold mode.

Write enabled logic

Two pmos devices are used to write data in to the cell. Write enabled logic is shown in fig.8

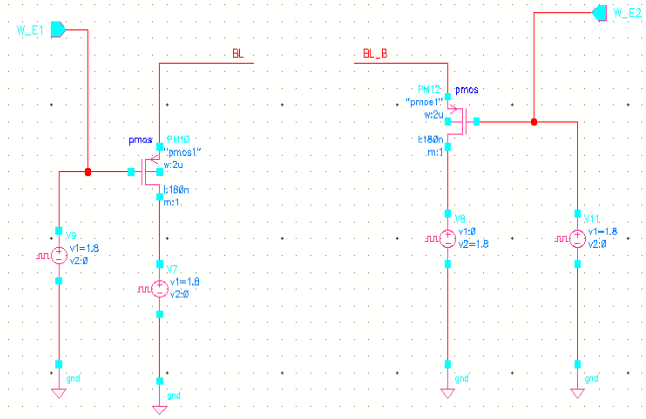

Figure 8 : Write enabled logic

The pins W_E1 and W_E2 are used to write enable or disable the logic. when write enable is logic low data present at the source of pmos will be transmitted to cell.

Simulation of Proposed 7T SRAM Cell

In proposed 7T SRAM Cell condition for cell ratio (CR) and pull up(PR) ratio are adjusted to get read operation wave forms.

The proposed 7T SRAM Cell with Precharge circuit, sense amplifier and write enabled logic is shown in fig.9

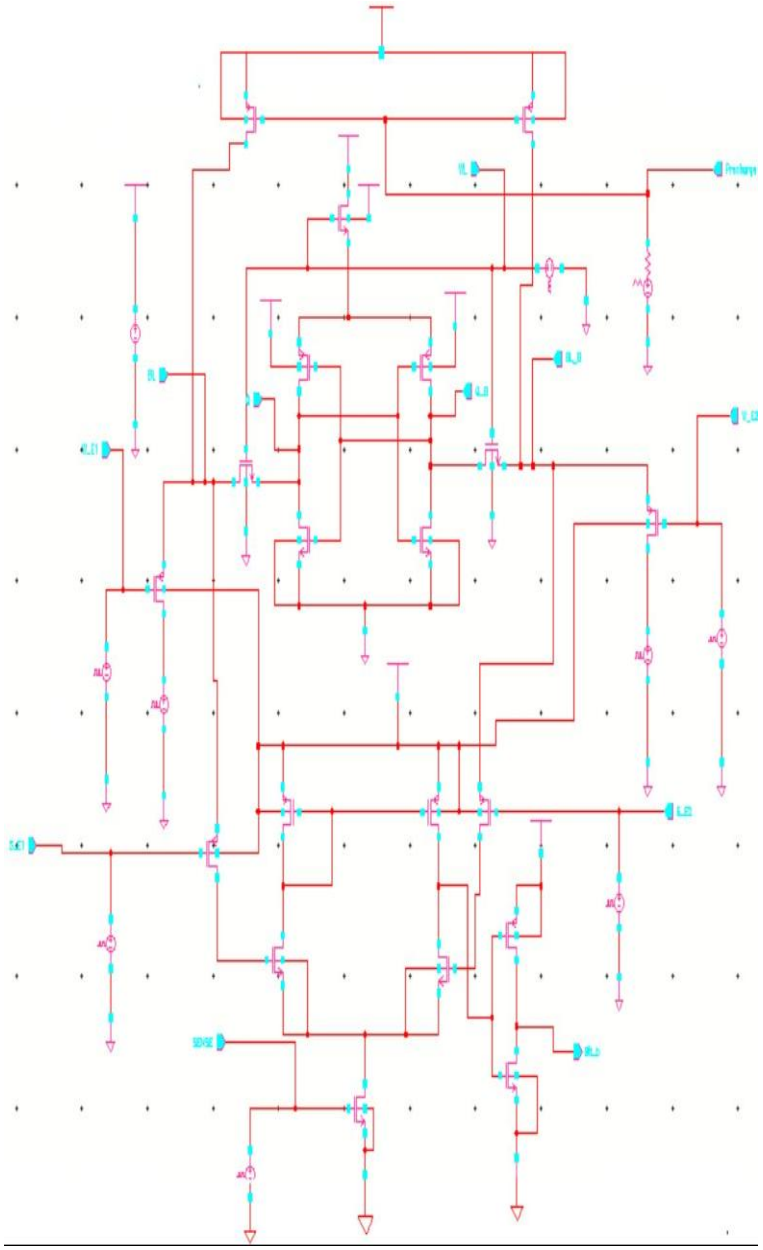

Figure 9 : 7T SRAM for simulation

Figure 10 shows transient analysis waveforms for read write and hold of proposed 7T SRAM Cell.

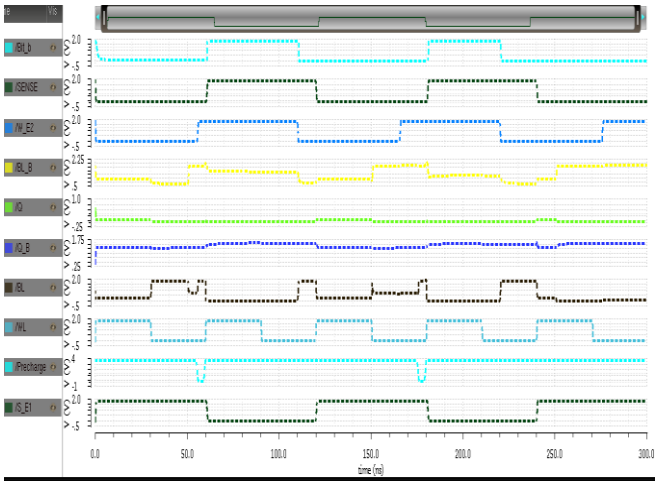

Figure 10 : Transient analysis waveforms

Table 1 shows total power consumption and static power dissipation of conventional 6T SRAM Cell and proposed 7T SRAM Cell.

Device	Total Power Consumption(W)	Static power Dissipation(W)
Conventional 6T SRAM	$2.887x10^{-6}$	$0.873x10^{-9}$
Proposed 7T SRAM Cell	$0.3x10^{-6}$	$0.833x10^{-12}$

Table 1. Static Power dissipation, total power consumption 6T SRAM cell and designed 7T SRAM Cell

IV. CONCLUSION

In this paper, substrate biasing is used to reduce the threshold voltage of extra NMOS for reducing total power consumption of SRAM Cell. This technique is benefited in standby mode as well as active mode of SRAM Cell. The proposed 7T SRAM is operated at 1.8 V power supply and consumes 0.3 mV and dissipates 0.833pW. Approximately 89% power is saved compared to conventional 6T SRAM cell.

REFERENCES

[1] Benton Highsmith Calhoun, Anantha P. Chandrakasan, "256-kb 65-nm Sub-threshold SRAM Design forUltra-Low-Voltage Operation" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 3, MARCH 2007

[2] Fumihiko Tachibana, Hirabayashi, Yasuhisa Takeyama "A 27% Active and 85% Standby Power Reduction In Dual-Power-Supply SRAM Using BL Power Calculator and Digitally Controllable Retention Circuit" IEEE journal of solid-state circuits,vol. 49, no. 1, january 2014

[3] B. S. Amrutur and M. A. Horowitz,"Speed and power scaling of SRAM's", IEEE Journal of Solid-State Circuits, vol. 35, February 2000.

[4] S. S. Rathod, *Member, IEEE, S. Dasgupta, Member, IEEE and A. K. Saxena, Senior Member, IEEE* "Investigation of Stack as a Low Power Design Technique for 6-T SRAM Cell ''

[5] Chua-Chin Wang, Po-Ming Lee, and Kuo-Long Chen "A Read-Static-Noise-Margin-Free SRAM Cell for Low-VDD and High-Speed Applications" IEEE journal of solid-state circuits, vol. 41, no. 1, january 2006

[6] Kaushik Roy "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Sub micrometer CMOS Circuits" proceedings of the IEEE, Vol. 91, NO. 2, Feb.2003

[7] S. Mutoh, "1-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solids-State Circuits, Vol. 30, No. 8, pp. 847-854, August 1995.

[8] Chua-Chin Wang, Po-Ming Lee, and Kuo-Long Chen A "An SRAM Design Using Dual Threshold Voltage Transistors and Low-Power Quenchers" IEEE journal of solid-state circuits, vol. 38, no. 10, October 2003

[9] Prashant Upadhyay, Rajib Kar, Durbadal MandaI, Sakti P GhoshalLow "Power with High Stability 12T MTCMOS Based SRAM Cell for Write Operation" International Conference on Communication and Signal Processing, April 3-5, 2014, India

First Author

Mrs.G.Surekha received the Bachelors degree in ECE from JNTU Hyderabad, India and did Masters degree in VLSI GRIET, Hyderabad, Telangana, India. She is currently working as Associate Professor in the Department of Electronics and Communication Engineering in GRIET and doing Ph.D in JNTU Hyderabad.

Second Author

Dr.N.Balaji received the Bachelors degree in ECE from Andhra university, Vishakhapatnam. He did masters degree and Ph.D in OU Hyderabad. Now he is currently working as Professor in the Department of ECE in JNTUK Vizianagaram, Andhra Pradesh. India

Third Author

Dr.Y.Padma Sai received the Bachelors degree in ECE from Nagarjuna University, She did masters degree and Ph.D in OU Hyderabad. Now She is currently working as Professor, Head of the Department ECE in VNR Vignana Jyothi Institute Of Engineering And Technology. Hyderabad, Telangana, India.

Fourth Author

R.Prashanth kumar received the Bachelor degree in ECE from RRS College of Engineering & Technology, Patancheru, Telangana,India and doing Masters degree in VLSI at Gokaraju Rangaraju Institute Of Engineering & Technology, Hyderabad,Telangana, India