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Design Of 2.4GHz Low Noise Amplifier Bypass Switch With Current Reuse Technique Used For Low Power Applications

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***Abstract*— Low-noise amplifier (LNA) is an amplifier used to amplify possibly weak signals. An LNA is a major component which is placed at the front-end of a receiver circuit. The low noise amplifier bypass switch is proposed. The Common gate (CG)-common source (CS) based cascode topology is used. The current reuse technique is used for low power consumption and high gain. The design emphasizes on low power dissipation for low power applications. Design works for 2.4 GHz frequency. The software tool used for designing the circuit is ADS (Advance Design System). Using 0.13 um CMOS process technology, it shows maximum power gain (*S*21) of 23.46 dB, minimum noise figure of 2.58dB, input return loss (*S*11) less than -10 dB, output return loss (*S*22) is less upto -8 dB and reverse gain of -39dB. Overall stability of circuit is 2.66 and IIP3 is 9.449 dBm. It consumes only 3.24mW of power from 1.2 V supply voltage.**

***Index Terms*—Current Reuse, Low Noise Amplifier, SPDT Switch**

I. INTRODUCTION

The low-noise amplifier is used in RF frontend of a wireless communication receiver system. It dominates the total noise of the receiver. However, it takes the cost of requiring more power for the high-gain LNA. It is more difficult to make tradeoffs between the performance of gain, noise figure, and linearity of the LNA when transistors operate at low power consumption and low supply voltage.

Current reuse is a well known technique to utilize the current in an efficient way. This concept basically consists of using the same current in several components. This literarily means stacking different components instead of cascading. This is very power efficient. The growing demand for low-cost and low-power CMOS radio frequency (RF) transceivers in the application of wireless body sensor networks and RF identification encourages research on low-power and ultralow-power RF circuit design techniques such as current reusing. A typical example of a current-reusing technique is stacking one current-hungry module on top of another to share their dc bias current, thus, the power consumption can be reduced significantly.

In this paper, current reuse technique is used at the common-source transistor of the cascode stage to achieve the high voltage gain. This CMOS LNA will be planned to work 2.4-GHz frequency band. For the design and simulation, the advance design system (ADS) is used. The frequency and technology selected for this design is 2.4 GHz and 0.13um CMOS respectively. The other important parameters of low noise amplifier design are gain, input return loss, output return loss, isolation and stability.

II. LITERATURE REVIEW

Low noise amplifier plays an important role as the first module of receiver [3]. The main effect of LNA is to amplify the faint signal which is received by the antenna. It should provide enough gain, low noise figure, high linearity, great input and output matching with restraint of power consumption [6]. Portable applications such as WLAN transceivers, cell phones and sensors networks strive to meet stringent performance requirement with the lowest power consumption to preserve battery life[1]. The current reuse amplifier used for high gain and low power consumption [8]. Current reuse techniques has been used in many recent LNA topologies to reduce power consumption in mobile device [2]. Low voltage and low power RF circuit design becomes a necessary requirement [5].

There are so many merits to use differential architecture, such as abiding the noise. Millimeter use to eliminate the negative effect of leaking signal. Mean while differential LNA can restrain common mode interference, so the noise of source voltage and under day voltage can also be restrained [6]. Signal ended LNA design needs additional balun circuitry to

converts single ended out put into differential output [7]. The LNA input impedance matching is extremely important as it ensures very weak signal received at antenna to be grouted with very less attenuation and amplifier in LNA. Output impedance provide normal signal flow through receiver [9].

In order to reduce the cost of RF frontend individual chip cost and overall component count must be reduced. This has encouraged many people move towards "system on chip" solution. To realize such goal, there is need for high isolation, high linearity SPDT switch is designed that can be fully integrated with other functional blocks and require no additional external component [10] .

III. PROPOSED LNA DESIGN

The whole schematic is designed in agilent's Advance digital system software (ADS).As it provides the function to choose the parameters automatically for the user, provided that it gives the optimization target. In a word, agilent's ADS are powerful for the circuit design at RF frequency. LNA designing needs to put several aspects into consideration, such as high gain, low noise figure, good input and output matching, stability and linearity. These factors are not independent from each other, and the unconditional stability often need to sacrifice part of the gain as compensation, and high linearity usually require high-current, and minimum noise figure is obtained at a lower current.

The current-reuse technology may provide the best combination of high power gain, low noise figure, and low power consumption, making it a viable candidate for use in LNA designs. This is single ended input and differential output low noise amplifier used in WLAN RF front end.

A Balun is a device which converts balanced impedance to unbalanced and vice versa. Baluns can take many forms and their presence is not always obvious. Sometimes, in the case of transformer baluns, they use magnetic coupling but need not do so. Common-mode chokes are also used as baluns and work by eliminating, rather than ignoring, common mode signals. A Single Pole Double Throw (SPDT) switch is a switch that only has a single input and can connect to and switch between 2 outputs. This means it has one input terminal and two output terminals. The below figure shows block diagram of LNA Bypass switch

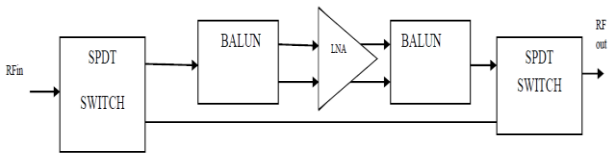

Fig 1. Block Diagram Of LNA Bypass switch

IV. CIRCUIT DIAGRAM

The below fig is the schematic of the LNA Bypass switch which is the integration of switch and differential amplifier designed to put several aspects into consideration, such as high gain, low noise figure, good input and output matching, stability.

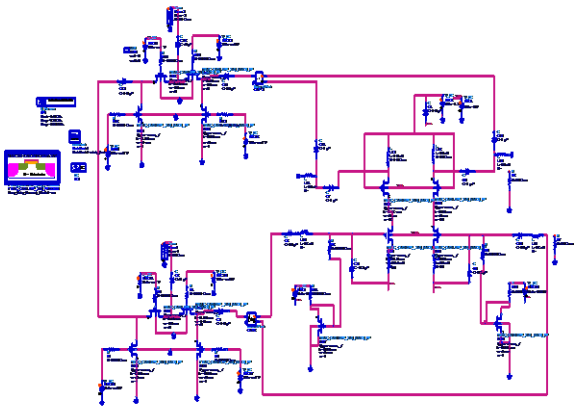

Fig 2. Circuit Diagram Of LNA Bypass Switch

V. SIMULATION RESULTS

A. *Gain versus Frequency plot*

A two-port network is essential in RF design simulations. Gain vs frequency plot shows how much output or signal strength we get at particular frequency. In low noise amplifier, gain and noise figure are important parameters. When the signal received by antenna is weak, which is then transfer to the low noise amplifier which increases the signal strength. This increase signal strength is nothing but the gain of the amplifier. Figure 3 shows *S*21 plot which shows 23.46 dB at 2.4 GHz. Plot shows minimum variation in gain that is flat gain over entire bandwidth.

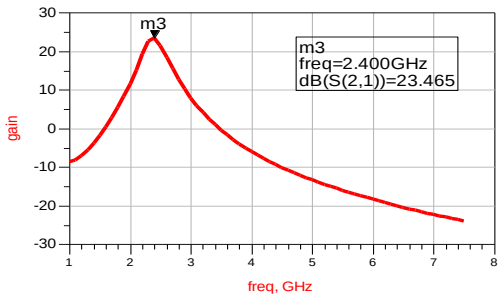

Fig 3. Gain vs. Frequency Plot

A. *Input return loss versus frequency plot*

It is amount of signal reflected back from input port when input is applied at port 1. Ideally it should be zero for no reflection. Figure 4 shows this plot, where *S*11 is -11.18 dB at 2.4 GHz. Result shows input is totally matched.

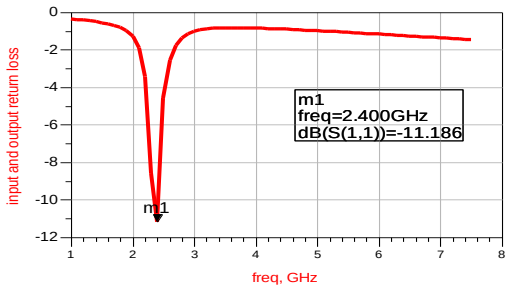

Fig. 4 Input return Loss vs. Frequency Plot

B. *Output Return Loss versus Frequency Plot*

It is amount of signal reflected back at output port when input is applied to it. Figure 5 shows this plot where *S*22 is -9.49 dB at 2.4 GHz.

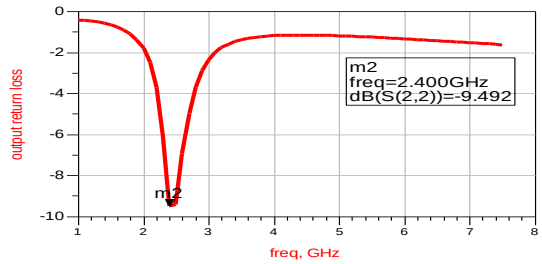

Fig 5. Output return Loss vs. Frequency Plot

C. *Reverse Gain versus frequency plot*

It is opposite to gain parameter. It is input applied at port 2 to output taken at port 1. It should be minimum that is less than zero. Figure 6 shows this, where it shows -39.71 dB at 2.4 GHz.

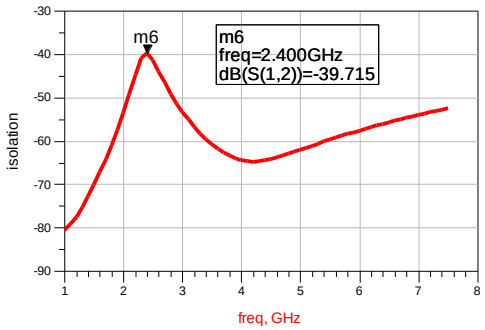

Fig 6. : Reverse gain versus frequency plot.

D. *Noise Figure Analysis*

The noise analysis performs analysis of device-generated noise for the given circuit. When provided with an input source and an output node, the analysis calculates the noise contributions of each device (and each noise generator within the device) to the output node voltage. It also calculates the level of input noise from the specified input source to generate the equivalent output noise.

The noise figure is defined by amount of noise contributed by the circuit. For any LNA design it is ideal to have our noise figure as low as possible. Figure 7 shows this, where it shows 2.586 dB at 2.4 GHz.

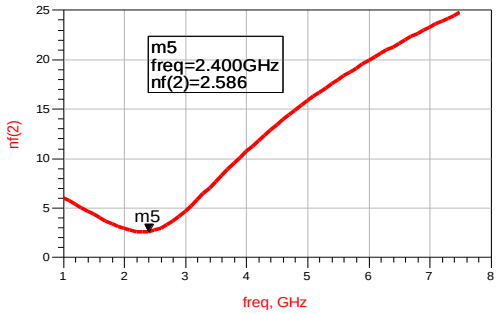

Fig 7. Noise figure versus frequency

E. *Stability Analysis*

Stability should be the next step in LNA design. Unconditional stability of the circuit is the goal of the LNA designer. While designing any amplifier, it is important to check the stability of the device chosen, or the amplifier may function as an oscillator. Unconditional stability means that with any load present to the input or output of the device, the circuit will not become unstable will not oscillate. Instabilities are primarily caused by three phe-nomena: internal feedback of the transistor, external feedback around the transistor caused by external circuit, or excess gain at frequencies outside of the band of operation. S-parameters provided by manufacturer of the transistor will aid in stability analysis: numerical and graphical. Numerical analysis consists of calculating a term called Rollett Stability Factor (K factor).

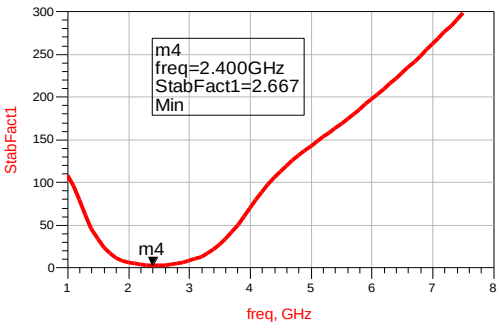

Fig 8. Stability vs. Frequency Plot

Stability Conditions:

Necessary condition:

$$K = \frac{1 - |S_{22}|^2 - |S_{11}|^2 + |\Delta_S|^2}{2|S_{12}S_{21}|} > 1$$

where,

$$\Delta_S = S_{11}S_{22} - S_{12}S_{21}$$

Most common causes for LNA instability are:

1. Insufficient RF decoupling between supply lines of the amplifier bias.
2. Parasitic inductance in GND connections.
3. Excess in-band and/or out-of-band Gain.
4. Electro-Magnetic coupling and Feedback.

F. Third order input intercept point (IIP3) analysis

IIP3 is calculated using following formulas and using 1 dB compression plots. The 1 dB compression point is a measure of the linearity of the receiver and is defined as the input RF power required to increase the conversion loss by 1 dB from ideal. From figure 9, it shows input power versus gain plot where maximum gain is 23.46 dB which is 1 dB compress at -20 dBm input
power. From the figure 10, it shows input power versus output power. It shows -1.051 dBm output power at -20 dBm input power. To plot these two figure, we have used following four equations. Using cubic power series approximation and analytic device model to estimate IIP3 is typically 10 to 15 dB beyond 1-dB compression point.

$$IIP3 = P1dB + 10 \text{ to } 15dBm$$

From the graph, minimum IIP3 calculated is 9.049 dBm which shows device is linear and without third order distortion at 2.4 GHz.

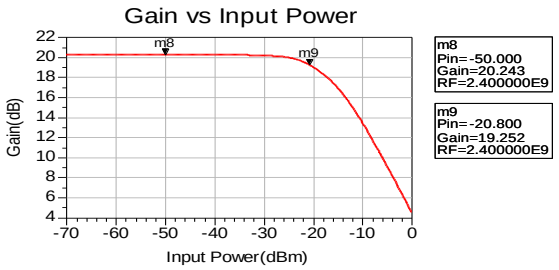

Fig 9. Gain vs Input Power

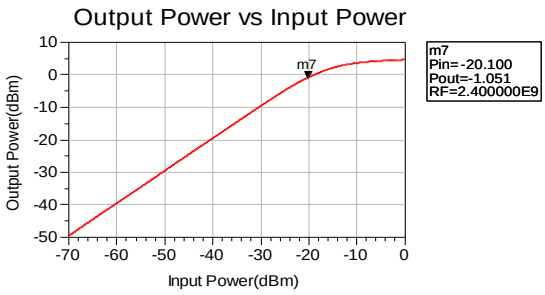

Fig 10. Output power vs. Input Power

Sr No.	Parameters	Measured Value
1.	S (2,1) Gain	23.46 dB
2.	S (1,1) Input Return Loss	-11.18 dB
3.	S (2,2) Output Return Loss	-9.49dB
4.	S(12) Reverse Gain	-39.715dB
5.	Stability	2.66
6.	Noise Figure	2.60 dB
7.	IIP3	9.049
8.	Total Power Consumption	3.24W
9.	Total DC Current	2.59mA

Table 1: LNA PERFORMANCE SUMMERY:

VI. LAYOUT OF THE CIRCUIT

The RF circuit designer must also consider board level variables when designing with an LNA. Designing an LNA on a printed circuit board (PCB) requires balancing a different set of variables that can have a significant effect on LNA performance: PCB layout, bias setting, input/output (impedance) matching, EM shielding, and supply decoupling. Starting with PCB layout, the designer should take care in designing the printed structures between the antenna and the LNA input.

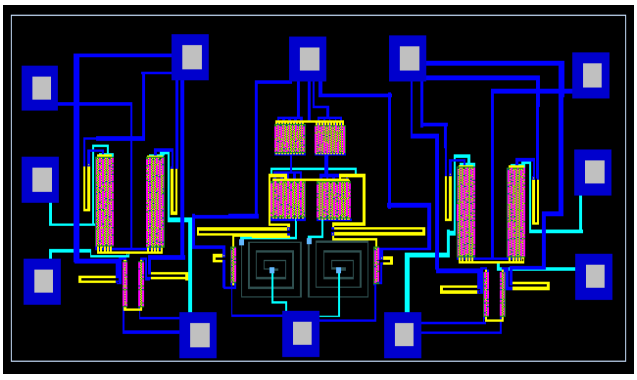

Fig 11. Layout of LNA Bypass switch

VII. CONCLUSION

The results achieved in this thesis are overall quite good. Overall performance for this amplifier shows that there should be possible to design a LNA with reasonable performance in spite of very low power consumption, e.g. it is probably possible to reduce the power consumption when designing an LNA, compared to what is yet published.

The amplifier is demonstrated with excellent gain, noise figure, and input/output return loss. The simulation results show that the integrated circuit can meet the requirements of LNA. Complete LNA schematic is simulated in Agilent's ADS through 0.13µm CMOS technology generates 23.46dB voltage gain (S21), 2.58dB noise figure (NF), -11.18 dB input return loss (S11) and -9.49dB output return loss(S22) also the stability factor is 2.66 at 2.4GHz frequency with voltage supply of 1.2V**.**

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