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Design and Simulation of Programmable Divider Circuit For PLL Based Frequency Synthesizer

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Abstract

In this paper, the divider circuit for PLL based Frequency Synthesizer has been designed. In the divider circuit, three types of counters have been used namely - Prescaler, Main Counter and Swallow Counter. The Divider circuit is a two modulus Divider and it can be used to divide by any value in the range 4635 to 4650 as per the requirement. It uses a two modulus Prescaler and it has two modes of operation. The scope of this PLL based Frequency Synthesizer along with Programmable Divider Circuit is in Enhanced GSM for mobile applications.

1. Introduction

A frequency synthesizer is a circuit design that generates a new frequency from a single stable reference frequency. A crystal oscillator is often used for the reference frequency. The main objective of frequency synthesizer is to recover the signal without phase and frequency error and this process is completed after many iterations inside the system. The fundamental functional blocks of any frequency synthesizer in general are

i) Phase frequency detector (PFD)

ii) Charge Pump (CP)

iii) Low pass filer (LPF)

iv) Voltage Controlled Oscillator (VCO)

v) Multi Modulus Divider (MMD)

The block diagram for Frequency Synthesizer is shown in Figure 1.

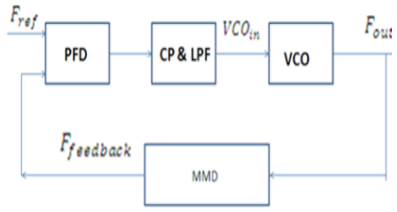

Figure 1 : Frequency Synthesizer Block Diagram

The basic Phase Locked Loop (PLL) consists of a phase detector, charge pump, low pass filter and a voltage controlled oscillator. The phase detector compares the phase of an incoming reference signal with that of the VCO, and produces an output that is some function of the phase difference. The output PFD consists of a dc component superimposed with an ac component. The ac part is undesired as an input to the VCO, hence low pass filter is used to filter out the ac component. The VCO generates a signal whose frequency is some function of the control voltage. It is a negative feedback system as the output of the phase detector drives the VCO frequency in a direction that reduces the phase difference.

Figure 2 below shows the integration of PFD, CP and loop filter. As shown in fig 1.2 , the reference input is given to the one of the PFD while VCO output is given to another input. This implementation senses the transition at the input and output detects phase or frequency difference and activates the charge pump accordingly. When input and output frequencies are sufficiently close , the PFD operates as phase detector, performing phase lock.

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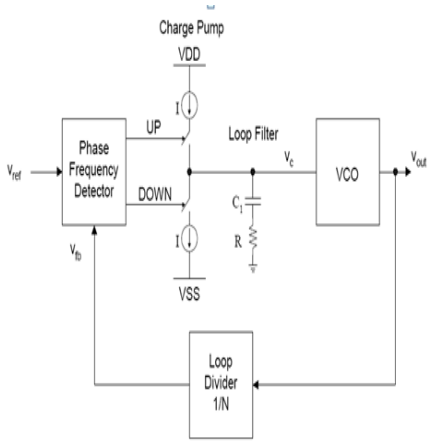

Figure 2 : Simple Charge Pump PLL

2. Frequency Synthesizer Architecture

The description of various blocks of Frequency Synthesizer are as follows:

2.1 Phase Frequency Detector

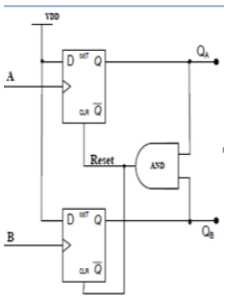

Figure 3 : Phase Frequency Detector

It consists of two edge triggered D flip flops with their D inputs tied together to logical one. Inputs A and B serve as clock of flip flops. If $Q_A = Q_B = 0$ and A goes high, Q_A rises. If this event is followed by a rising transition on B, Q_B also goes high and the AND gate resets both flip flops. In other words, Q_A and Q_B are simultaneously high for a short time but the difference between their average values still represents the input phase or frequency difference correctly.

2.2 The Charge Pump

A charge pump is a three position electronic device switch which is controlled by the three states of a PFD. When switch is set in UP or DOWN position, it delivers a pump voltage $\pm V_P$ or a pump current $\pm I_P$ to the loop filter. When both UP and DOWN of PFD are off , the switch is open thus isolating the loop filter from the charge pump and PFD. The basic charge pump is shown in Figure 3.

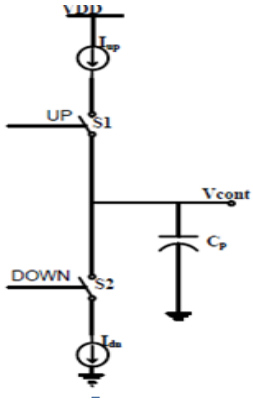

Figure 4 : Basic Charge Pump Architecture

As shown in the fig 4 current sources I_{up} and Idn are identical. Two outputs of PFD are given to the UP and DOWN inputs of charge pump respectively. If Q_A=Q_B=0, then S1 and S2 are off and V_{out} or V_{cont} remains constant. If Q_A is high and Q_B is low, then I_{up} charges Cp. Conversely if Q_A is low and if Q_B is high, then I dn discharges Cp.

2.3 Loop Filter

The output of PFD consists of dc component superimposed with an ac component. The ac part is undesired as an input to VCO. Hence low pass filter is used to filter out ac component. Both passive filter and active filter can be used but a passive filter is usually preferred than an active filter because an active filter results in higher complexity, cost and noise.

2.4 VCO

A VCO is a voltage controlled oscillator whose output frequency is linearly proportional to the control voltage generated by the PFD and Loop Filter

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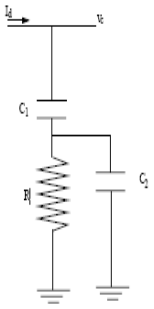

Figure 5 : Second Order Passive Loop Filter

3. System Design

This design generates signals with frequencies from 927 MHz to 930 MHz with Reference Frequency equal to 200KHz. Loop Division Ratio (N_{min}, N_{max}) is obtained as follows:

$N_{min} = f_{min}/\Delta f$
$N_{max}=f_{max}/\Delta f$

Damping factor ξ is set to the value of 0.707.
The natural frequency $w_n = w_{3db}/2.06$.

VCO gain $K_{vco} = 2\pi.(f_{max}-f_{min})$ /voltage.

4. Design of Loop Divider Circuit

The designed frequency synthesizer uses a two modulus divider (figure 5). It consists of pre-scaler, a main counter, a Swallow Counter and a control unit. The Prescaler has two modes of operation- one mode provides an output for every input pulse P and the other mode provides an output for every (P+1) input pulse. Here two Prescalers in the two modulus dividers are divide by 64 and divide by 65 pre-scalers.

4.1 Divide by 64

To divide an input frequency by 64, six D flip flops are required. It consists of a series of D flip flops, where each D flip flop 's inverted output is connected back to its input

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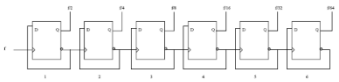

Figure 6 : A Divide By 64 Prescaler

4.2 Divide by 65

To build divide by 65 divider circuit, it is divided into two units. One unit is a divide by 5 circuit and the second one is a divide by 13. The output of first unit will be fed into the second unit and the whole circuit will be a divide by 65 prescaler circuit. Basically, these two circuits are ring counter with the number of states corresponding to the division number. In divide by 5 circuit, the ring counter will have five stages. The number of flip flops required can be found from the number of stages. As such three D flip flops are required for the divide by 5 circuit as it has only five stages. All flip flops are rising edge divide by 13 circuit, the number of flip flops required are four.

4.3 Main Counter

Main counter is also a frequency divider circuit. It divides by 72. The input of the main counter is the output of the pre-scalar unit e.g for the division number of 4365, it takes first 27 pulses of the divide by 65 pre-scaler and remaining 45 pulses of divide by 64 unit and yield only one pulse. This pulse is equal to the output of the VCO divided by 4635. The circuit of main counter first divides the input by 12 and then the second unit divide this output by 6 yielding a total of divide by 72 output. The number of flip flops required can be found from the number of stages. So we need four D flip flops for the divide by 12 circuit as it has 12 stages and 3 D flip flop for divide by 6 circuit.

4.4 Swallow counter

The swallow counter counts down from the loaded number to zero. It is basically a programmable down counter. A number is loaded in the swallow counter (27 to 42 in the present design) to generate 16 different frequencies. Since the maximum value

of A is 42 in this design, therefore six output lines are required for programming the swallow counter. Thus six flip flops are required for this design. Whenever the Main Counter outputs a pulse , the counting sequence needs to begin again.

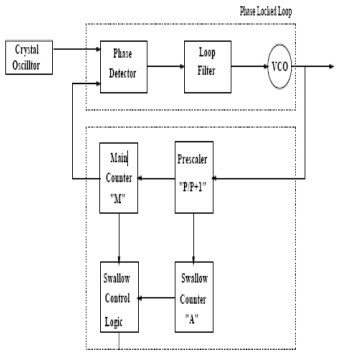

Figure 5 : A Two Modulus Frequency Synthesizer

5. Simulation of Divider Circuits

The simulation of Prescaler, Main Counter and Swallow Counter are performed in the Matlab's SIMULINK toolbox and the results are verified as follows:

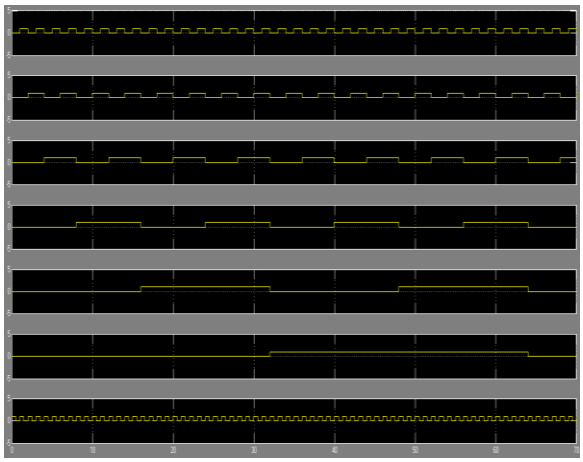

Figure 5 :SIMULINK Result of Prescaler (Divide by 64)

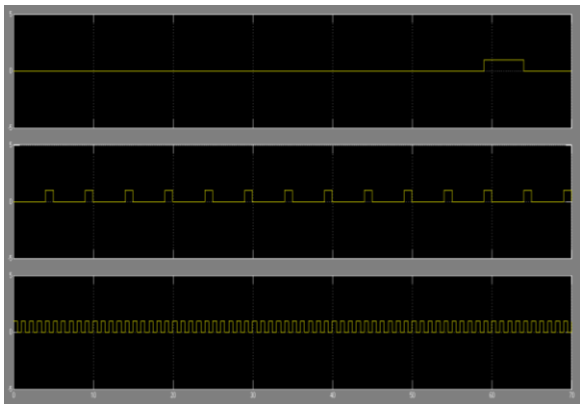

Figure 5 :SIMULINK Result of Prescaler (Divide by65)

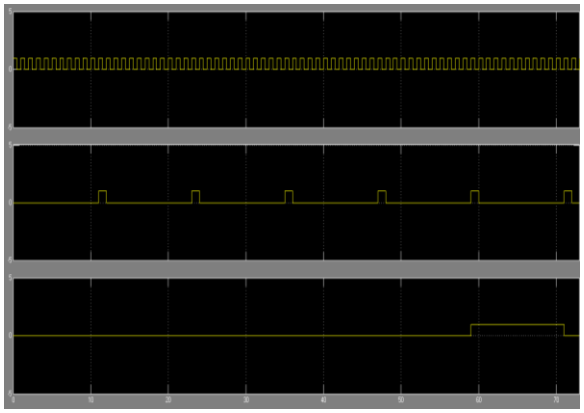

Figure 5 : SIMULINK Result of Main Counter

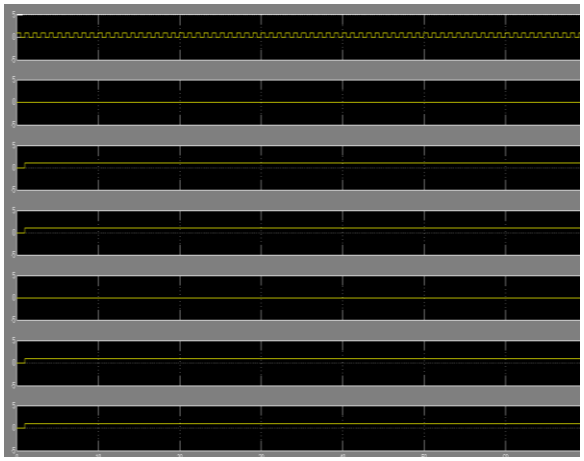

Figure 8 : SIMULINK Results for Swallow Counter (Loading 27)

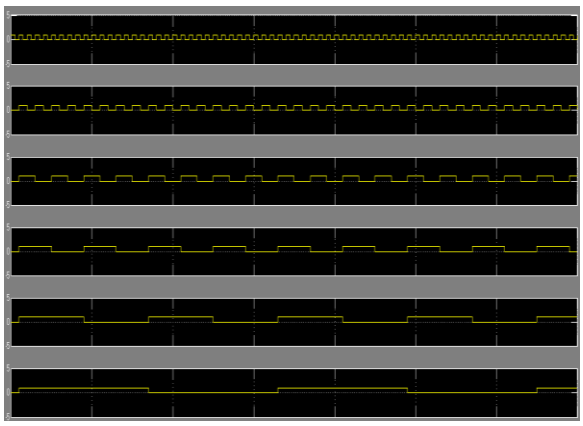

Figure 8 : SIMULINK Results for Swallow Counter

6. Conclusion

The frequency synthesizer using PLL incorporate high speed frequency dividers. By varying the value of swallow counter , a large range of integer value can be obtained and so is the output frequency. The design are simulated in Matlab's simulink.

7. References

1 F Gardner, "Charge Pump Phase Lock Loop"IEEE transactions on Communications, Vol 28, No 11, Nov 1980.

2 Lee Tai-Cheng and Razavi Behzad, "A stabilization Technique for Phase-Locked Frequency Synthesizers", IEEE Journal of Solid State Circuits, Vol. 38, No. 6, June 2003

3 Haijun Gao, Sun Lingling, Cai Chaobo and Zhan Haiting, " Pulse Swallowing Frequency Divider With Low Power And Compact Structure", Journal of Semiconductors, Vol 33, No.11 , Nov 2012.

4 Bozomitu Radu Gabriel, Cehan Vlad, "A New VLSI Implementation of a CMOS Frequency Synthesizer for SRD Applications", IEEE 16th International Symposium for Design and Technology in Electronic Packaging, 2010.

5 Christopher and Razavi Behzad, "A 2.6 GHz/5.2 GHz Frequency Synthesizer in 0.4-µm CMOS Technology", Symposium on VLSI Circuits Digest of Technical Papers, 1999.

6 Razvi Behzad, " Design of Analog CMOS Integrated Circuits", Tata Mc Graw Hill Education Pvt Ltd.

7 Haijun Gao, Sun Lingling, Cai Chaobo and Zhan Haiting, " Pulse Swallowing Frequency Divider With Low Power And Compact Structure", Journal of Semiconductors, Vol 33, No.11 , Nov 2012.

8 Razvi Behzad, " Challenges in the design of Frequency Synthesizers for Wireless Applications", IEEE , Custom Integrated Circuits Conference, 1997.