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QPSK based Low Frequency Trans-Receiver Implementation on FPGA for SDR

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***Abstract*— Software radio's basically a combination of hardware and software. Software radio technology provides the simplest design to complex radio designs in future generation of wireless communications. Software radios are can be reprogrammed to vary functionalities like data rate, modulation, filtering, etc. Hence it is called as reconfigurable device. Usage of SDR in digital communication systems can easily provide compact coding & modulation techniques to reach ever increasing requirements of the wireless communication industries. SDR provides a platform for wireless communication which based on software as well as software. Runtime reconfiguration of components of radio can be achieve by using field programmable architectures platform. Same block can be use for different data rate, modulation and demodulation technique and carrier frequency of signals. This project deals with the design & implementation of low-frequency trans-receiver based on QPSK modulation and demodulation technique on SPARTAN-3AN FPGA kit. Different blocks are design digitally by hardware description language. Implementation of such technique can be on field programmable platform.**

***Index Terms*— FPGA SPARTAN-3AN, VHDL, QPSK**

I. INTRODUCTION

Software-Defined radio (SDR) defines as "radios that provide software control on modulation techniques & communications security functions." In short, software modules running on a general hardware platform of DSPs and general purpose microprocessors can implement radio functions such as modulation/demodulation, signal generation, coding and protocols. This helps in building reconfigurable software radio systems where dynamic selection of parameters is possible. SDR has the ability to work with many different standards and be continuously reprogrammed and also reconfigurable. Multimode implies the ability to process several different kinds of standards. Examples of standards are AM, FM, PM, and CDMA and many more. These modes may be implemented sequentially or simultaneously. Implementation of such technique can be on field programmable platform. The SDR concept promises the main solution of supporting a multitude of wireless communication services in a single infrastructure design. The need to communicate with people using different types of equipment can only be solved using software programmable radios because of its flexible architecture.

II. BACKGROUND

A software-defined radio (SDR) allows for digital communication systems to simply accept more complicated coding and modulation technologies. An SDR has been constructed, using the VHDL i.e. Hardware description language that means various blocks of trans-receiver are designed digitally, and implemented on the SPARTAN-3AN Field Programmable Gate Array (FPGA) development kit. The modulation scheme used in the system is Quadrature Phase-Shift Keying (QPSK). In the first step to realize the whole modulation and demodulation schemes using VHDL coding. The format of a VHDL program is built around the concept of blocks which are the basic building units of a VHDL design. The results showed that the proposed method can greatly improve efficiency, shorten developing period and reduce costs.

III. LITERATURE SURVEY

Title of Paper	Issues Discussed	Outcome	Methodology	Scope
[1] SDR - IMPLEMENTATION OF LOW FREQUENCY TRANSRECEIVER ON FPGA – 2014[1], IEEE	Design and implementation of Low Frequency Trans-Receiver.	low cost, low power SDR solution	Quadrature Phase Shift Keying	Only applicable to QPSK modulation technique
[2] Dynamic Reconfiguration Technologies Based on FPGA in Software Defined Radio System –	Dynamic reconfigurable port	Partial reconfiguration of SDR	DRP and PR reconfiguration technologies	proposed architecture could achieve reductions of 70.4%

2011[2], Springer				
[3] Design of BPSK Transmitter Using FPGA with DAC-2009[3],IEEE	Implementation of BPSK transmitter using ASIC	DAC gives real-time result	Binary phase shift keying	Can be Implement for bandwidth efficient modulation technique

IV. DESIGN AND IMPLEMENTATION ON FPGA

The low frequency trans-receiver design is illustrated in Figure 1. A Pseudo-Random sequence of 32 bits at the rate of 50 KHz is converted from serial to parallel using a demultiplexer to get the In-phase (I) and Quadrature-phase (Q) components and fed to Unipolar to bipolar converter. The respective NRZ streams are shaped using raised cosine filters (roll off = 0.5) then multiplied with cosine and sine Carriers of 1MHz and added to give the modulated signal for transmission. As QPSK modulation requires 2 bits to effect phase changes, the symbol rate becomes 25KHz. The received signal is demodulated by multiplying it with the 1 MHz Carrier, filtered, and given to a decision circuit multiplexer and down sampled to retrieve the demodulated data.

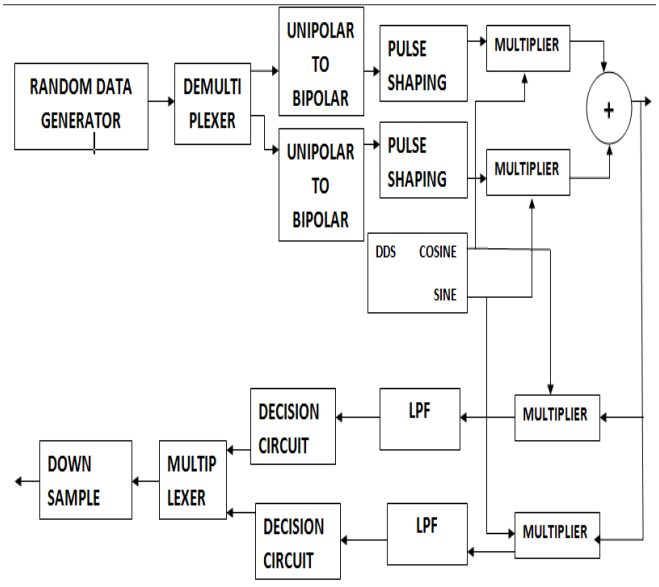

Fig. 1. Schematic of QPSK based Trans-Receiver

In this project, we propose to design an digital trans-receiver based on Quadrature phase shift keying. Here we implement trans-receiver using hardware description language (VHDL) & simulation with the help of Xilinx FPGA. By implementing this technique, several logic gates can be reduced. The aim of this project is to design and implement Low Frequency Trans-Receiver on Spartan-3AN FPGA device. The modulation scheme used in system is Quadrature phase shift keying It provide a suitable platform to achieve reconfigurations of the components of the radio.

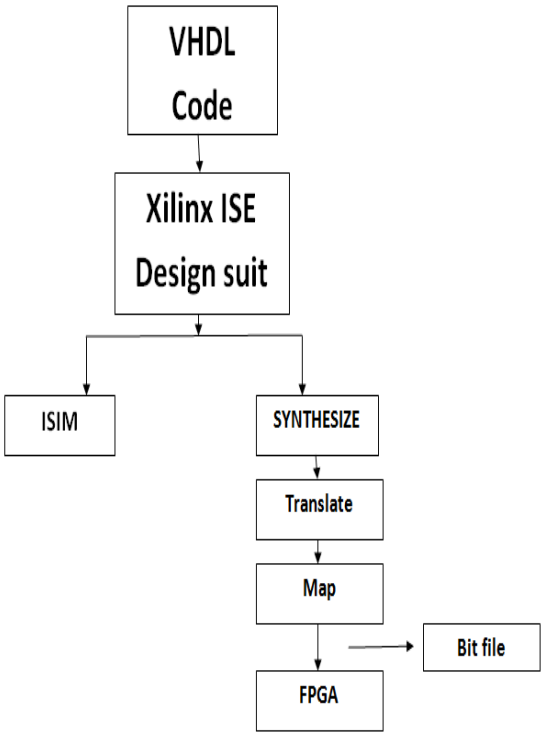

Fig. 2. Design Process Flow

V. RESULTS & DISCUSSION

(i) Fig 3 shows top level, RTL schematic of the implemented design and Fig 4 shows internal schematic of trans-receiver. The device utilization summary of the Spartan_3AN FPGA is shown in Table 2 and Table 3 with comparison as existing and proposed device summary.
(ii) Fig. 5 & 6 shows RTL schematatic of Transmitter & receiver respectively. Results of the Xilinx Isim test bench is as shown in Fig 7,8 & 9. This results shows the output at each block of Trans-receiver.
(iii) Fig. 10 shows the data given to the modulator and data received form the demodulator with a delay as measured by the scope and it exactly matches on FPGA Spartan-3AN kit.

VI. CONCLUSION

Performance in terms of modulation techniques implementation aspects leading to increase

- Power Efficiency
- Bandwidth efficiency

The available resources where reduces by over 50% in

comparison with the existing model. Meanwhile, this design reduces power consumption to some extent, for the power consumption is directly related to the chip area.

VII. FUTURE WORK

The submitting author is responsible for obtaining agreement of all coauthors and any consent required from sponsors before submitting a paper. It is the obligation of the authors to cite relevant prior work.

Authors of rejected papers may revise and resubmit them to the journal again.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	**7547**	**11776**	**64%(*)**
Number of 4 input LUTs	**5587**	**11776**	**47%(*)**
Number of bonded IOBs	**21**	**372**	**5%(*)**

Table 2 Existing Device Summary

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	**1443**	**11776**	**10%**
Number of 4 input LUTs	**3356**	**11776**	**28%**
Number of bonded IOBs	**12**	**372**	**3%**

Table 3 Proposed Device Summary

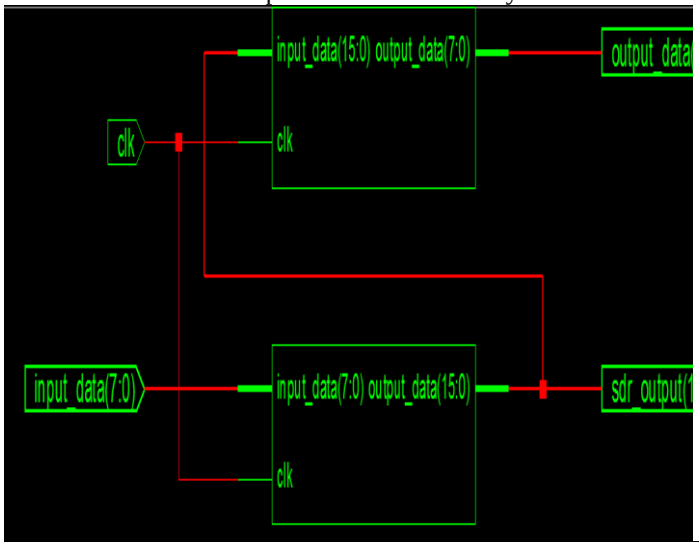

Fig. 3. Internal Schematic

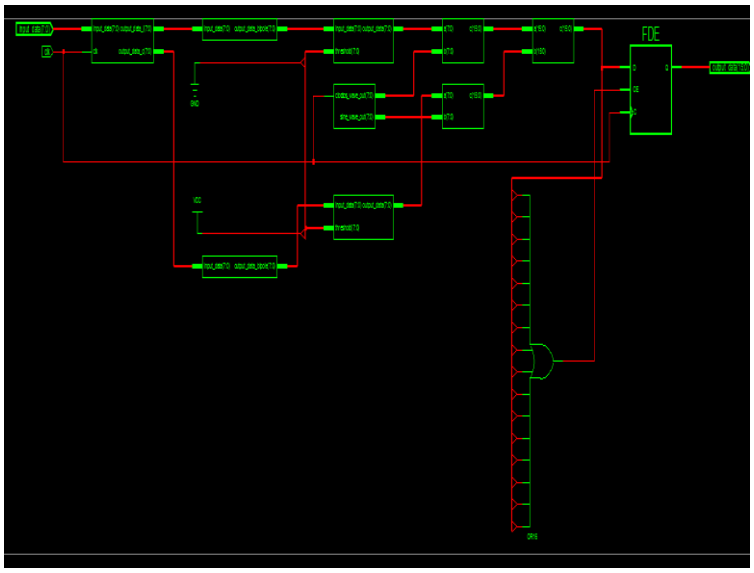

Fig. 4. Transmitter Schematic

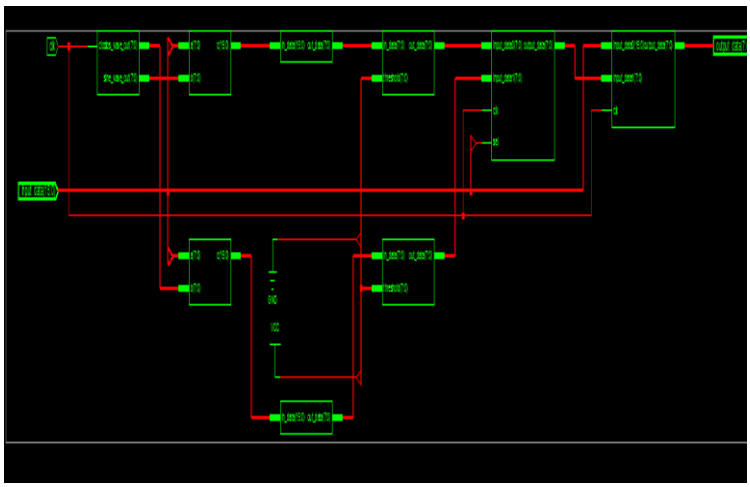

Fig. 5. Receiver Schematic

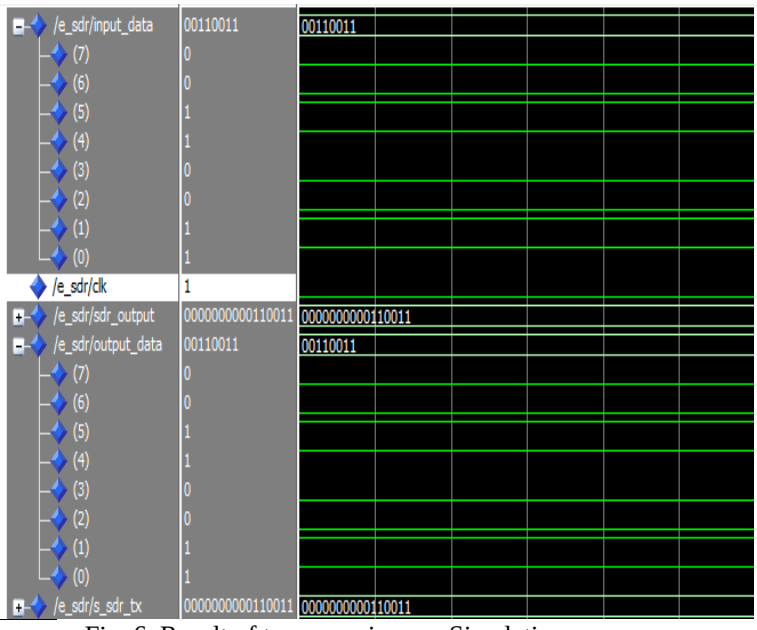

Fig. 6. Result of trans-receiver on Simulation

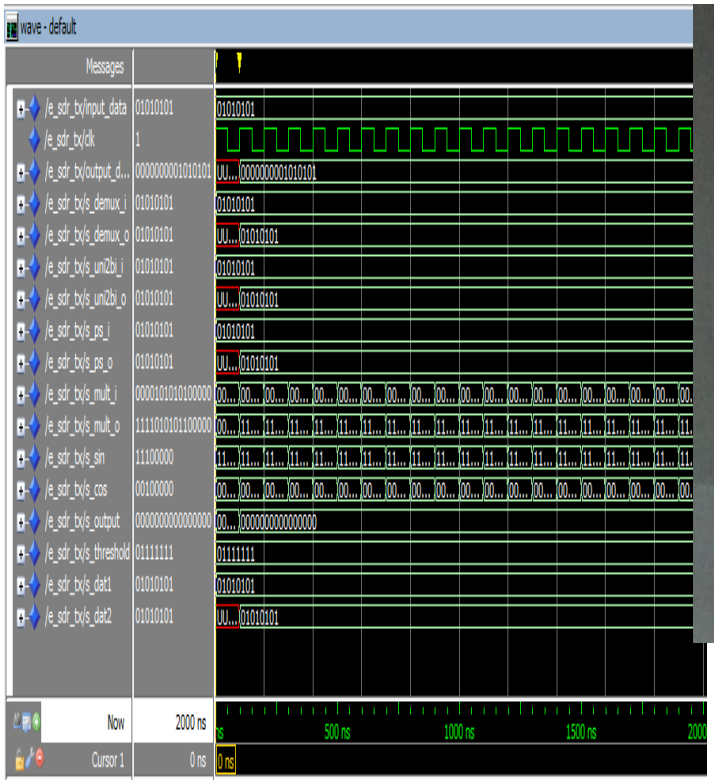

Fig. 7. Results of transmitter on Simulation

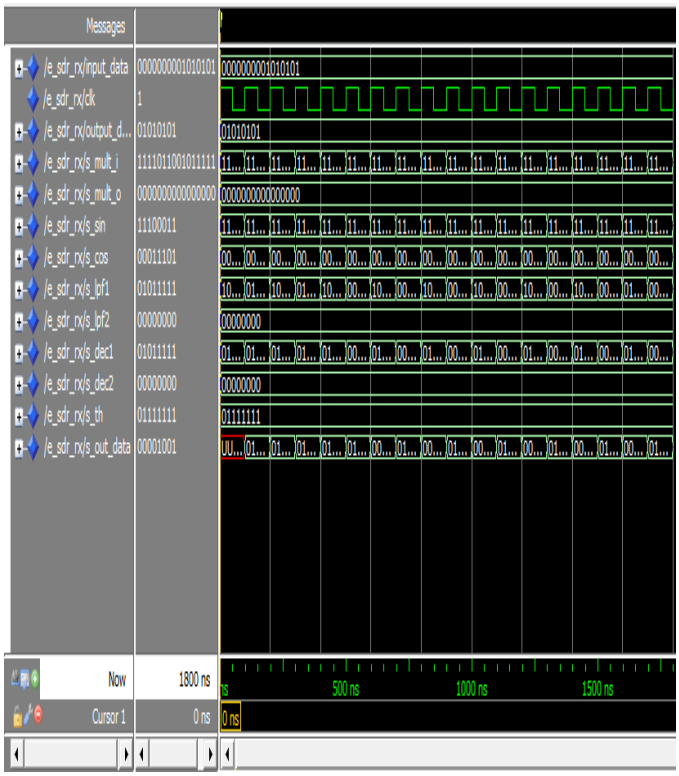

Fig. 8. Results of receiver on Simulation

Fig. 9. Data transmitted and received on FPGA

REFERENCES

[1] International Conference on Signal Processing and Integrated Networks (SPIN) "SDR - IMPLEMENTATION OF LOW FREQUENCY TRANS-RECEIVER ON FPGA", 2014.

[2] Wenmiao Song, Qiongqiong Yao "Design and implement of QPSK modem based on FPGA" 3rd IEEE International Conference on Computer Science and Information Technology (ICCSIT), (Volume:9), 2010.

[3] Teena Sakla, Divya Jain, Sandhya Gautam "Implementation of Digital QPSK Modulator by Using VHDL/MATLAB" International Journal of Engineering and Technology Vol. 2(9), 2010.

[4] Vinod Kumar Venkat Reddy Gari, "*FPGA-based QPSK transceiver design"*, Technical Report, Department of Electrical and Computer Engineering, Bradley University, November 2008.

[5] Chris Dick, Fred Harris, and Michael Rice, "FPGA implementation of carrier synchronization for QAM receivers", Journal of VLSI Signal Processing, Vol. 36, pp. 57-71, Kluwer academic publishers, Netherland, 2004

[6] Hiroshi Harada, Ramjee Prasad, "Simulation and Software Radio for Mobile Communications," Artech House Publishers Bk & CD-Rom edition. pp. 90-93,2002

[7] J. Hwang, B. Milne, N. Shirazi, J. Strommer, "System Level Tools for DSP in FPGAs," Xilinx Inc., 2001

[8] M. L. Welborn, "Direct Waveform Synthesis for Software Radios, "IEEE Wireless Communications and Networking Conference WCNC.1999, vol. 1, pp. 211-215, September 1999.