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Comparative Analysis of GDI based D Flip Flop Circuits using 90nm and 180nm Technology

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***Abstract*— The fast growth of power density in integrated circuits (IC) has made power dissipation, area and delay as the vital design measures. As a result several D flip flop design topologies has been developed and analyzed by the designers for an optimal performance. It is noted that power consumption, delay and area are the major factors that have to be taken into account while designing a circuit. In this paper GDI based D-flip-flop is proposed by using different technologies of VLSI system for making high performance processing element. The evaluation is carried out by tanner tool with 180 nm & 90 nm technology. This DFF design allows reduced power-delay product and area of the circuit, while maintaining low complexity of logic design. Performance comparison is presented with respect to number of transistors, power dissipation and delay.**

***Index Terms*— D flip-flop, Gate-Diffusion-Input (GDI) technique.**

I. INTRODUCTION

Digital logic circuit, in which current state of the output depends not only on the current input values but also upon the sequence of logic values that lead to the current input values, are known as sequential logic circuits. In the sequential logic circuit, the most important memory element is the flip flop, which is made of an assembly of logic gates [2][10]. Even though a logic gate itself, has no storage capability several (logic gates) can be connected together in many ways that permit information to be stored. There are several different gate arrangements that are used to produce these flip flops (abbreviated as FF). Flip flop is used in storage circuit, counter stages, shift registers and many other computer applications. Several flip flop categories are there such as RS flip flop, JK flip flop, D flip flop and T flip flop etc [9][12].
We are considering D flip flop. D flip flop is known as a state holding element (hold its output until next clock pulse). Many D flip flop circuits such as Pass Transistor Logic (PTL), Single Edge Trigger (SET), Double Edge Trigger (DET), Transmission Gate (TG), Hybrid Latch Flip Flop (HLFF), Adaptive Coupling (AC) and Gate Diffusion Input (GDI) techniques have been introduced in order to achieve an optimal design in terms of delay, power consumption and area[6][13].Out of all these configurations, GDI based DFF is widely used [1][3][5][7][8].

II. BASIC GDI FUNCTION

GDI basic cell is similar to the standard CMOS inverter, with little difference that is-

- There are three inputs in the GDI cell: G (input through common gate of nMOS and pMOS), P(input through the source or drain of pMOS),N(input through the source or drain of the nMOS).
- Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter [1].

We use recently developed GDI technique.GDI principal is based on the GDI cell (Fig.1).Basic cell contains-G (common input of nMOS and pMOS), P (the outer diffusion node of the pMOS transistor) and N (the outer diffusion node of the nMOS transistor).For different circuit structures, interpretation of these terminals may also be different (i.e. either input or output).In the GDI cell almost all functions are possible while not all of the functions are possible in the standard CMOS circuit [1][4].
GDI cell can be implemented with simple gates, less transistors and less power dissipation. If we want to increase the bit size of DFF using GDI technique then simply GDI cells can be connected in parallel to fulfill the objective [4][11].

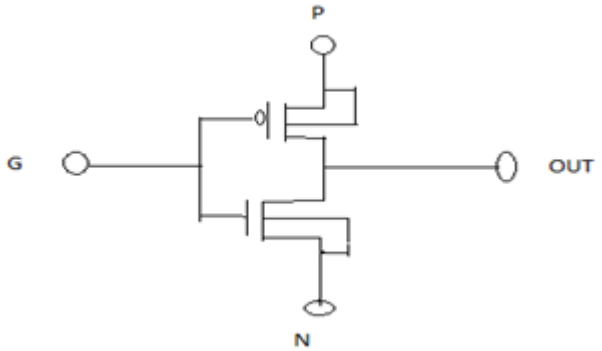

Fig.1 GDI basic cell

In a GDI cell Master Slave principal exists between nMOS and pMOS. At input ‘0’ pMOS will operate (pMOS acts as master and nMOS as slave) and at input ‘1’ nMOS will operate (nMOS acts as master and pMOS as slave).

By changing the input i.e. N, P and G in the basic GDI cell various configurations correspond to different Boolean functions at output (Table I) [1][10][12].

Table I Various Logic Functions of GDI Cell for Different Input Configurations

N	P	G	OUT	FUNCTION
'0'	B	A	A'B	F1
B	'1'	A	A'+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	A'B+AC	MUX
'0'	'1'	A	A'	NOT

III. Related Work

Arkadiy Morgensgtein et al. [1] proposed D flip flop using GDI technique. They used .35 micro meter and .18 micro meter technology to compare the GDI structure with existing alternatives, and showed up to 45% reduction in power delay product in GDI. Their main concern was to reduce the power delay product as compared to other alternatives.

R.Jayagowri and K.S.Gurumurthy [5] tend to decrease the power of combinational circuit. They presented two gating techniques (i.e. double edge triggered and double edge triggered with single latch) to decrease power dissipation due to unnecessary switching of combinational circuit. They increased power saving up to 13%-18.5% by adding their proposed scan flip flop.

N. Vishnu Vardhan Reddy et al. [8] proposed that GDI technique allows reduced power consumption, delay, area of digital circuit by scaling the power supply voltage because power consumption is majorly affected by power supply voltage. They operated the circuit with supply voltage less than threshold voltage i.e. known as sub threshold region.

Aklia M. et al. [10] thought that area and power dissipation are major parameters that have to be considered. They analyzed several flip flop designs and overcome power dissipation in their proposed circuit by reducing the number of transistors.

Other researchers also work in this direction to reduce these parameters to achieve optimization.

IV. Proposed Work

GDI based DFF has been implemented in such a way that it is achieved with the reduced area and propagation delay due to lesser number of transistors. Our main concern is to reduce power consumption, area and propagation delay. Simulation is done using Tanner tool with 90nm and 180nm technology file. Width of nMOS and pMOS also has been taken into account to achieve optimization of our design parameters.

Fig. 2 shows the design of DFF using GDI technique. In this the gates that are controlled by the clock (clk) signal, create two alternative paths (i.e. 0 and 1). When the clk is low, the signals are propagating through pMOS transistors .When the clk signal is high, internal values are maintained due to conduction of the NMOS transistors.

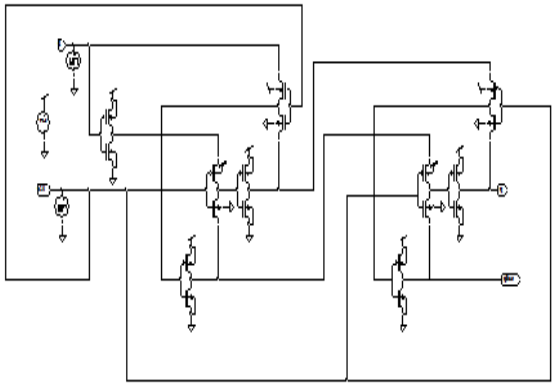

Fig.2 Design of DFF using GDI technique

V. Simulation And Results

For the comparison of proposed work and efficient implementation of D Flip Flop using the GDI technique, two parameters i.e. power consumption and delay has been taken into account. Variation in power dissipation and delay comes due to change in the width of nMOS and pMOS, as a result PDP (Power Delay Product) also change. Results are improved very much by reducing the width of pMOS and nMOS as shown in (Table II).

Table II Comparative Analysis of Power Consumption and Delay with Variable Width for 1-Bit GDI Circuit Using 180nm Technology

Design Style	No. of Tran.	Mini. Length (nm)	Width of nMOS (micro meter)	Width of pMOS (micro meter)	Avg. Power Cons. (w)	Prop. Delay at Q(s)	PDP
1 Bit GDI DFF(Eff. Impl.)	18	180nm	33.1	33.1	151.7e-006	275.0 e-012	41.7 e-015
1 Bit GDI DFF(Prp. work)	18	180nm	30	30	133.2e-006	288.5 e-012	38.3 e-015
			40	40	173.5e-006	262 e-012	45.3 e-015
			50	50	213.5e-006	260 e-012	55.3 e-015
			20	20	926.1e-006	335 e-012	310.2 e-015
			10	10	510.1e-006	448 e-012	228.5 e-015
			27	81	45.9 e-006	55.2 e-012	25.4 e-015

Then GDI based DFF 1bit circuit implemented with 90nm and 180nm technology as shown in (Table III). Number of transistors also reduced from 18 to 16 by replacing two transistors with power supply. Results of power and delay are shown for both 16 as well as 18 transistors. PDP is very large for 18 transistors as compare to 16 transistors.

Table III Comparison of 1 Bit Different D flip flop using 90nm &180nm Technology

Design Style	No. of Tran.	Min. Length (nm)	Width of nMOS (micro meter)	Width of pMOS (micro meter)	Avg. Power Cons. (watt)	Prop. Delay at Q(s)	PDP
1Bit GDI DFF	16	90nm	.14	.41	28e-006	148.2 e-012	4.1e-015
		180nm	.27	.81	42.8e-006	49.1 e-012	21e-015
1Bit GDI DFF	18	90nm	.14	.41	30.5e-006	238.3 e-012	7.2e-015
		180nm	.27	.81	45.9e-006	55.2 e-012	25.4e-015

Similarly GDI based DFF 16 bit circuits is implement by placing 1 bit circuit in parallel. In this case it is observed that the power consumption, area, delay and PDP are less in case of a circuit comprises of 256 transistors as compared to a circuit which comprises of 320 transistors. Results are shown in (Table IV).

Table IV Comparison of 16 Bit Different D flip flop using 90nm &180nm Technology

Design Style	No. of Tran.	Min. Length (nm)	Width of nMOS (micro meter)	Width of pMOS (micro meter)	Avg. Power Cons. (watts)	Prop. Delay at D(s)	PDP
16bit GDI DFF	256	90nm	.14	.41	448.1e-006	148.2 e-012	6.6e-015
		180nm	.27	.81	685e-006	49.1 e-012	33.6e-015
16 bit GDI DFF	320	90nm	.14	.41	571.1e-006	221.2 e-012	12.6e-015
		180nm	.27	.81	856.2e-006	54.6 e-012	46.7e-015

VI. Conclusions And Future Scope

There are many challenges while designing GDI based D flip flop like power consumption, delay, area, number of transistors and speed etc. In proposed work the focus is on power consumption, delay and area. In this work GDI based D flip flop is implemented with 180nm technology and results of power consumption and delay are improved. Similarly same circuit implement with less area and results are recorded for 90nm and 180nm technology. Then implementation of 16 bit circuit is done by placing 1 bit circuits in parallel.

Future research steps may be taken to optimize the parameter like frequency, capacitance, length, width etc. The efforts can be made to decrease the transistor count, as a result power, area and delay will also decrease. This work can be extended by changing the technology file.

Proposed design is suitable for high performance digital design where area and power dissipation are of major concern.

References

[1] Arkadiy Morgenshtein, A. Fish, and I. A. Wagner, "An Efficient Implementation of D Flip Flop using the GDI Technique ," IEEE Trans. on VLSI Systems, volume 4, issue 2, pp 673-676,2004

[2] Imran Ahmed Khan, Dr. Mirza Tariq Beg," Novel Low Power and Low Transistor Count Flip Flop Design with High Performance", Innovative System Design and Engineering, volume 3, issue 11, pp 2222-1727,2012

[3] M. Janaki Rani, S.Malarkann," Leakage Power Reduction and Analysis of CMOS Sequential Circuits", International Design of VLSI design and communication system, volume 3, issue 1, pp 13-23,2012

[4] Priyanka Sharma, Neha Arora, Prof. B.P.Singh," Low Power Different Sense Amplifier based Flip Flop Configuration Implemented using GDI Technique", International Journal of Scientific and Research Publication, volume 2, issue 2, pp 2250-3153,2012

[5] R. Jayagowri and K.S. Gurumurthy," Implementation of Gating Technique with Modified Scan Flip Flop for Low Power Testing of VLSI Chips", Springer Berlin Heidelberg, volume 7373, pp 52-58,2012

[6] Imran Ahmed Khan, Dr. Mirza Tariq Beg,"A New Area and Power Efficient Single Edge Triggered Flip Flop Structure for Low Data Activity and High Frequency Applications," Innovative system Design and Engineering, volume 4, issue 1, pp 2222-1727,2013

[7] Ravi.T, Irudaya Praveen.D, Kannan.v," Design and Analysis of High Performance Double Edge triggered D-Flip Flop", International Journal of Recent Technology and Engineering, volume 1, issue 6, pp 2277-3878,2013

[8] N.Vishnu Vardhan Reddy, C. Leela Mohan, M. Srilakshmi," GDI based Subthreshold Low Power D Flip Flop", International Journal of VLSI and Embedded Systems, volume 4, issue 06112, pp 2249-6556, 2013

[9] M.Arunlakshman, T.DineshKumar, N.Mathan," Performance Evaluation of 6 Transistor D Flip Flop based Shift Registers using GDI Technique", International Journal of Advanced Research in Computer and Communication Engineering, volume 3, issue 3, pp 2278-1021, 2014

[10] Aklia. M, Sathiskumar. M, Sukanya. T,"A Novel Analysis on Low-Power High-Performance Flip Flops", International Journal of Computer Applications, volume 90, issue 16, pp 32-37,2014

[11] Aditi Mehta, Riya Jain, Vaishali Yadav," Low Power Design for D Flip Flop", International Journal on Recent and Innovation Trends in Computing and Communication, Volume 2, Issue 7, pp 2321-8169,2014

[12] Sadhana Patil, Prof. Anil Wanare ," Review on Low Power Pulse Triggered Flip Flops", International Journal of Advanced Research in Computer Science and Software Engineering, volume 5, issue 1, pp 647-650, 2015

[13] Hardeep Kaur, Swarnjeet Singh, Sukhdeep Kaur," Design and Analysis of D Flip Flop using Different Technology", International Journal of Innovative Research in Computer and Communication Engineering, volume 3, issue 7, pp 2320-9801,2015