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REVIEW OF CARRY SELECT ADDER BY USING BRENT KUNG ADDER

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***Abstract*— In order to perform the addition of two numbers adder is used. Adder also form the integral part of ALU. Besides this application of adder in computer, it is also employed to calculate address and indices and also operation codes. Different algorithm in Digital Signal Processing such as FIR and IIR are also employed using adder. What all matter is speed and so it is the most important constraint. The important areas of VLSI areas are low power, high speed and data logic design. In Carry Select adder the possible value of input carry are 0 and 1. So in advance, the result can be calculated. Further we have the multiplexer stage, for calculating the result in its advanced stage. The conventional design is the use of dual Ripple Carry Adders (RCAs) and then there is a multiplexer stage. Here, one RCA (Cin=l) is replaced by Brent kung adder. As, RCA (for Cin=O) and Brent Kung adder (for Cin=l) consume more chip area, so an add-one scheme i.e., Binary to Excess-l converter is introduced. Also the square root adder architectures of CSA are designed using Brent Kung adder in order to reduce the power and delay of adder.**

***Index Terms*— Brent Kung Adder, Carry Select Adder, Delay, Area.**

I. INTRODUCTION

Adder is the important element present in computer and others digital devices. It not performs addition of any given of numbers but it is also utilized to calculate the addresses and indices or the operation codes. Convention In this paper, Carry Select Adder (CSA) architectures are designed using Brent Kung adders. Instead of using Brent Kung (BK) adder is used to design Regular Linear CSA. The square root adder architectures of CSA are designed using Brent Kung adder in order to reduce the power and delay of adder. This paper Modified Square Root Carry select Adder (MSRCSA) using Brent Kung adder is proposed using single BK, BEC and MUX in order to reduce the power Consumption with small penalty in speed, carry select adder.

II. LITERATURE REVIEW

In this paper, the logic behind operations involved in regular carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA are analyzed to studied the data dependence and to identify redundant logical operations [1]. They have eliminated all the redundant logic techniques used in the regular CSLA and proposed a new logic formulation for CSLA. In the proposed method, the carry select (CS) operation is scheduled before the theoretical calculation of *final-sum*, which is different from the conventional approach value. Bit patterns of two anticipating carry words (similar *c*in = 0 and 1) and fixed bits *c*in are used for logical techniques of Carry select and generated units. An better CSLA design is obtained using logic units. The proposed CSLA design involves significantly efficient area and delay than the recently proposed BEC-based CSLA. Due to the efficient carry-output delay, the proposed CSLA design is a very good candidate for square-root (SQRT) CSLA. A theoretical and practically estimate shows that the proposed Area of SQRT-CSLA involves nearly 35% less area–delay–product than the BEC-based SQRT-CSLA, which is best among value of the existing SQRT-CSLA designs, on average, for different bit-widths.

In this paper, carry Select Adder (CSLA) is the fastest adders used in many computer data-processing processors to perform fast arithmetic functions [2]. From the structure of the CSLA, it is cleared that there is scope for efficient the area and power consume in the CSLA. This work used a simplest and efficient transistor level modification in BEC-1 converter to significantly efficient the area and power of the CSLA. Based on this modification 16-b structure of square-root CSLA (SQRT CSLA) architecture have been design and compared with the SQRT CSLA architecture design using ordinary BEC-1 converter. The proposed design has efficient area and power as compared with the SQRT CSLA used ordinary BEC-1 converter with only a slight increased in the delay.

In this paper carry Select Adder (CSLA) is one of the good adders used in many computer data-processing processors to perform fast arithmetic functions [3]. From the structure of the CSLA, it is clear that there is scope for efficient the area and power consumed in the CSLA. This work used a simple and efficient gate-level modification to significantly efficient the area and power of the CSLA. Based on this modified 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture design has been developed and compared with the regular SQRT CSLA design architecture. The proposed design has reduced efficient area and power as compared with the regular SQRT CSLA with only a slight increased in the delay. This work evaluates the performance of the proposed implemented of designs in terms of delay, area, power. layout in 180-n CMOS process technology. The results analysis shows the proposed CSLA structure is much good than the regular SQRT CSLA.

In this Paper Carry Select Adder (CSA) is known to be the fastest adder among the conventional adder structures [4]. It is used in many processor for realizing faster arithmetic operations. In this paper, present an innovative CSA architecture. It employed a novel incremental circuit in the interim stages of the CSA. The proposed designed is done

through designed and implemented of 16, 32 and 64-bit adder circuits. Comparisons with existing paper conventional fast adder design architectures have been made to prove its efficiency. The performance analysis shows that the architecture achieves three folded advantages in terms of delay, area efficient power.

In this paper investigates four types of adder PPA's (Kogge Stone Adder (KSA), Spanning Tree Adder (STA), Brent Kung Adder (BKA) and Sparse Kogge Stone Adder (SKA)) [5]. Additionally Ripple Carry Adder (RCA), Carry Look ahead Adder (CLA) and Carry Skip Adder (CSA) are also investigated. These adders are implemented in Very-log Hardware Description Language (HDL) using Xilinx technology Integrated Software Environment (ISE) 13.2 Designed Suite. These designed are implemented in Xilinx technology Vertex 5 Field Programmable Gate Arrays (FPGA) kit and delays are measured using Agilent 1692A logic analyzed and all these adder's delay, efficient power and area are investigated and compared finally.

In this paper Carry Select Adder (CSLA) is one of the fastest adders used in processors to perform fast arithmetic functions [6]. From the structure of the CSLA, it is clear that there is scope for efficient the area and power consumption in the CSLA. This worked uses a simpler and sufficient transistor level modification to significantly efficient the area and power of the CSLA. Based on this modification 4-bit design CSLA architecture have been developed and compared with the regulated CSLA architecture design. The proposed worked design has reduced power efficient area as compared with the regular CSLA with only a slightly increased in the delay. This work evaluated the performance of the proposed worked designs in terms of delay, area, efficient power, and their products by hand with logical effort and through custom design and layout in 180-nm CMOS technology file.

III. PARALLEL PREFIX ADDERS

These are used to take up the binary additions because of their flexibility. Carry Look Ahead Adder's (CLA) structure is utilized in order to get the parallel prefix adders . Tree structures algorithm are used to increase the speed of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation. The construction of parallel prefix Adder [10] involves three stages:

1. Pre- processing stage
2. Carry generation Process
3. Post processing stage

Pre-possessing stage:-

Generate and propagate signals to each pair of the inputs A and B are computed in this stage. These signals are given by the,

Following equations:

Pi=Ai xor Bi (1)

Gi=Ai and Bi (2)

Carry generation network:-

In this stage, carries equivalent to each bit is calculated.

All these operations are implemented and carried out in parallel. Carries in parallel are segmented into smaller pieces after the implementation of the stage. Carry propagate and generate are used as intermediate signals which are given by the logic equations3& 4:

CPi:j=Pi:k+l and Pk:j (3)

CGi:j=Gi:k+l or (Pi:k+l and Gk:j) (4)

The operations involved in fig. 1 are given as:

CPO=Pi and Pj (3(i))

CGO=(Pi and Gj) or Gi (3(ii))

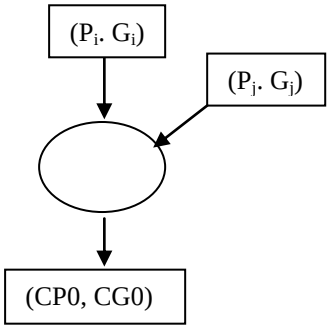

Figure1: Carry Network

Post processing Stage:-

This is the concluding step to compute the summation of input bits. It is similar for all the adders and then sum bits are computed by logic equation 4& 5:

Ci-1= (Pi and Cin) or (4)

Si=Pi xor Ci-1 (5)

Brent-Kung Adder:-

Brent-Kung adder [10] is a very popular and widely used adder. It actually gives an excellent number of stages from input to all outputs but with asymmetric loading of Intermediate stages. It is one of the parallel prefix adders.

It is one of the parallel prefix adders where these adders are the ultimate class of adders that are based on the use of generate and propagate signals. In case of Brent kung adders along with the cost, the wiring complexity is also less. But the gate level depth of Brent-Kung adders [11] is 0 (log2 (n)), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Fig. 2.

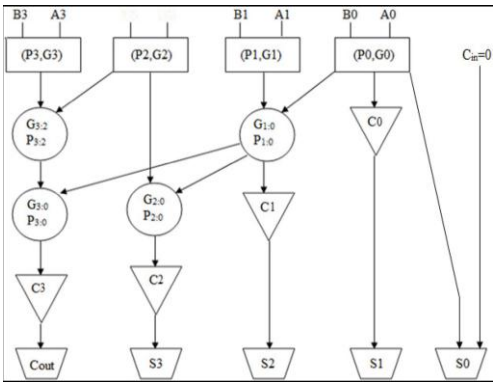

Figure 2: (4 –bit Brent Kung Adder)

IV. REGULAR LINEAR BRENT KUNG CARRY SELECT ADDER

Conventional Carry Select Adder consists of dual Ripple Carry Adders and a multiplexer. Brent Kung Adder [9] has reduced delay as compared to Ripple Carry Adder. So,

Regular Linear BK CSA is designed using Brent Kung Adder. Regular Linear KS CSA consists of a single Brent Kung adder for Cin=O and a Ripple Carry Adder for Cin=1. It has four groups of same size. Each group consists of single Brent Kung adder, single RCA and multiplexer. We use tree structure form in Brent Kung adder to increase the speed of arithmetic operation. The schematic diagram of Regular Linear BK CSA is shown in Fig. 3.

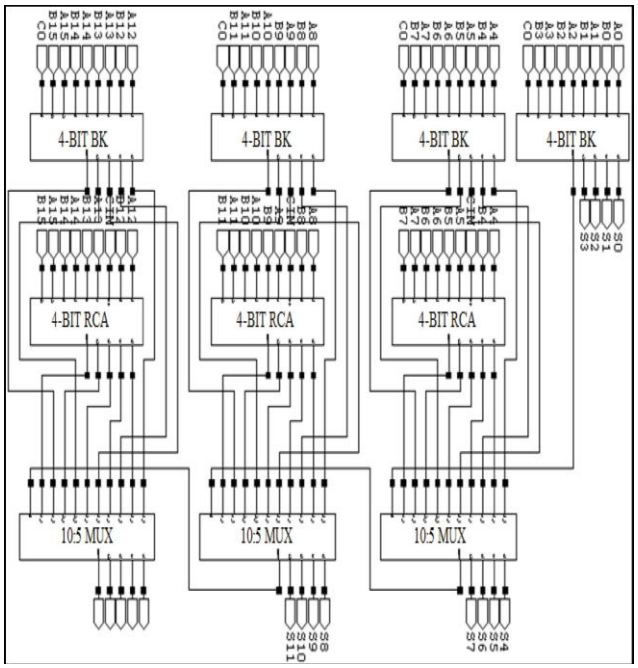

Figure 3 : Schematic Diagram of BK adder

V. MODIFIED LINEAR BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung Carry Select Adder uses single Ripple Carry Adder (RCA) for Cin=O and Brent Kung adder for Cin=l and so it consumes more area. To solve this problem add-one schemes like Binary to Excess- 1 Converter (BEC) have been introduced. Using BEC, Regular Linear BK CSA is modified in order to obtain a reduced area and power consumption. Binary to Excess-l converter is used to add 1 to the input numbers. So, here Brent Kung adder with Cin=1 will be replaced by BEC because it require less number of logic gates for its implementation so the area of circuit is less. A circuit of4-bit BEC and truth table is shown in Figure 4 and 5.

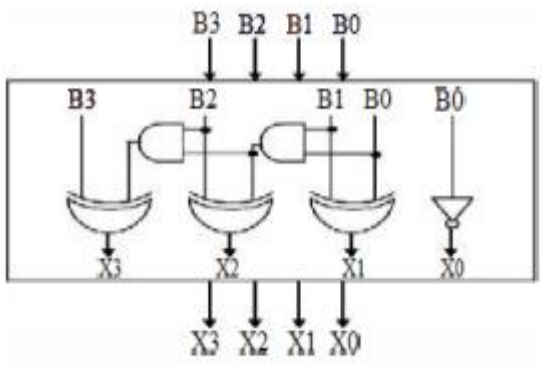

Figure 4 : (4 bit Binary to Excess-1 convertor.)

The Boolean expressions of 4-bit BEC are listed below,
XO = -BO
Xl = BO (l)/\Bl
X2 = B2 /\ (BO &Bl)
X3 = B3 /\ (BO & B 1 & B2)

Binary Logic $B_0 B_1 B_2 B_3$	Excess-1 Logic $X_0 X_1 X_2 X_3$
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

Figure 5 : truth table of 4-bit binary to excess-I converter

Linear Modified BK CSA is designed using Brent Kung adder for Cin=O and Binary to Excess-l Converter for Cin=l in order to reduce the area and power consumption. Linear Modified BK CSA consists of 4 groups .Each group consists of single BK adder, BEC and multiplexer. The block diagram of Linear Modified BK CSA is shown in Fig. 6

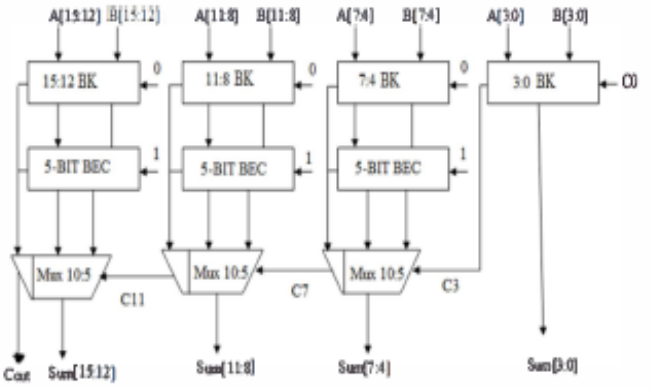

Fig.6 block Diagram of 16-bit Linear Modified BK Carry Select Adder

VI. REGULAR SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung Carry Select Adder consumes large area and to reduce its delay a new design of adder is used i.e. Regular Square Root Brent Kung Carry Select Adder. Regular Square Root BK CSA has 5 groups of different size Brent Kung adder. Each group contains single BK for Cin=O, BEC and MUX. The block diagram of the 16-bit regular SQRT BK CSA is shown in Fig. 8. High area usage and high time delay are the two main disadvantages of Linear Carry Select Adder. These disadvantages of linear carry select adder can be rectified by SQRT CSA . It is an improved version of linear CSA. The time delay of the linear adder reduces. This is called a Square Root Carry Select Adder.

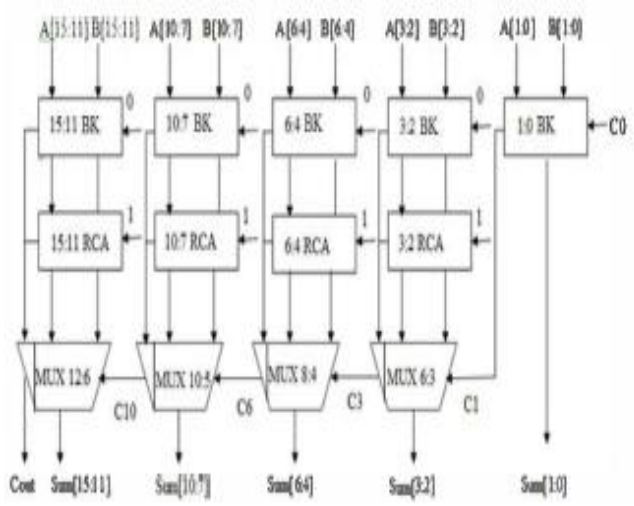

Figure 7: Block Diagram of l6-bit Regular Square Root BK Carry Select Adder

VII. Modified Square Root Brent Kung Carry Select Adder

Modified Square Root Brent Kung Carry Select Adder has been designed using Brent kung adder for Cin=O and BEC for Cin=l and then there is a multiplexer stage. It has 5 groups of different size brent kung adder and Binary to Excess-l Converter (BEC). BEC is used to add 1 to the input numbers. Less number of logic gates are used to design BEC as compared to RCA therefore it consumes less area. The block diagram of the 16-bit modified Square Root BK Carry Select Adder is shown in Figure 8.

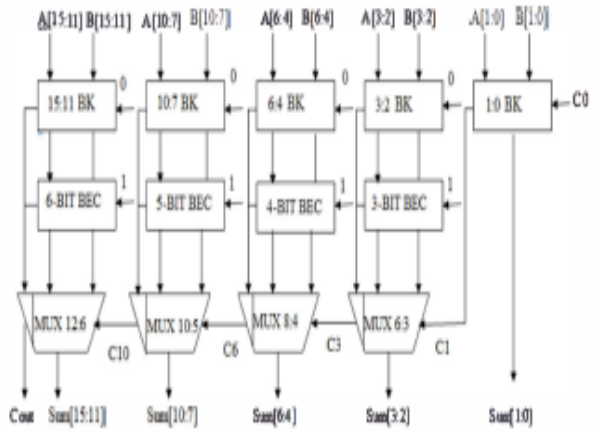

Figure 8: Block Diagram of 16-bit Modified SQRT BK CSA

VIII. Problem Formulation

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used arithmetic logic unit, as-well-as other parts of the processor, where they are used to calculate addresses, table indices, and same operations. Adders are used in multipliers, in DSP to execute various algorithms like FFT, FIR and IIR. Millions of instructions per second are performed in microprocessors using adders. So, speed of operation is the most important in BK Adder. Design of low power, high speed data path logic systems are one of the most essential parameter Modified Square Root Carry select Adder using Brent Kung adder is proposed using single BK and BEC instead of dual RCAs in order to reduce the power consumption with small efficient in speed.

IX. Proposed Work

A] Adaptive Scaling of the Supply Voltage

By changing the supply voltage on static gates, we can change the performance and energy in both directions. In other words, while the whole system is on the lower supply like 1.1V, changing the static gates' supply toward 1.1V reduces the power and pushing it toward 1.3V enhances the circuit speed.

B] Leakage Power Reduction another task which is mostly done by power aware software's is to position the circuit blocks in sleep mode during their inactivity periods to avoid leakage power dissipation. Using sleep mode transistors, adaptive body biasing and applying specific sleep vectors are some common techniques for leakage power reduction during idle times. The dual supply adder dissipates more leakage energy than the conventional one during the recharge condition, because the PMOS transistors in the static gates are not completely on. Therefore, one method for leakage energy reduction during idle times could be applying body bias to PMOS transistors in the static gates to increase their threshold voltage.

X. Summary

In this work, a Modified Square Root BK Carry Select Adder is proposed which is designed using single Brent kung adder and Binary to Excess-l Converter instead of using single Brent kung adder for Cin=O and Ripple Carry Adder for Cin=l in order to reduce the delay and power consumption of the circuit. Here, the adder architectures like Regular Linear BK CSA, Modified Linear BK CSA, Regular SQRT BK CSA and Modified SQRT BK CSA are designed for 16-Bit word size only. This work can be extended for higher number of bits also. By using parallel prefix adder, delay and power consumption of different adder architectures is reduced. As, parallel prefix adders derive fast results therefore Brent kung adder is used. The synthesized results show that power consumption of Modified SQRT BK CSA is reduced in comparison to Regular Linear CSA but with small speed penalty. The calculated results conclude that Modified Square Root BK Carry Select Adder is better in terms of power consumption when compared with other adder architectures and can be used in different applications of adders like in multipliers, to execute different algorithms of Digital Signal Processing like Finite Impulse Response, Infinite Impulse Response etc.

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