ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 11, November 2015

Design And Analysis Of Implicit Pulsed Double Edge Triggered Clocked Latch For Low Power Applications

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***Abstract* –In this paper, a new technique for implementing double edge triggered flip flop is introduced. The technique is used to reduce number of clocked transistors in the design. The effective methodology of the double edge triggered paradigm and n-MOS transistor logic of the new proposed implicit pulsed double edge triggered flip-flop (PIPDETFF) is proposed. The power aware technique of the sleep and sleep-bar is used to the clocked latch of the paradigm to present the circuit in idle mode and reduced the power consumption. The power consumption of clocked latch is lower than that of the clocking distribution network. The design can be implemented in DSCH and MICROWIND 3.1 CMOS layout tool. Analysis of the performance parameters shows that performance of PIPDETFF is superior compared to the conventional flip flop. A 6.52% to 22.11% reduction of power can be achieved in proposed implicit pulsed double edge triggered flip -flop (PIPDETFF).**

***Key words*: CMOS, Double Edge Clocking, Register Elements (flip –flops), Low Power**

I.INTRODUCTION

A System on Chip (SOC) is an Integrated Circuit(IC) that integrates all components of a electronics system into a single chip. In the past the major concerns for the VLSI designers was performance, cost and area. Power consideration was the secondary concerned. Now this trend was changed and the power consumption is considered as one of the major concerns in VLSI circuit design [1].one reason is that the enhancement of chip scale of integration and the improvement of the operating frequency has made power consumption as a major concern in VLSI circuit design. Power dissipation has a direct impact of the packaging cost of the chip and coding cost of the system [2, 3]. All the factors to drive the VLSI system designers to consider the power dissipations as a major issue and to reduce the circuit power dissipation. The clocking system is one of the major power consuming components in VLSI system [4,5]. The total power dissipation of the system accounts for 30% to 60% of power consumption [6]. Section II presents techniques for low power design of clocking system. Section III presents Analysis of Conventional Flip-Flops architecture (CFF). Section IV presents proposed implicit pulsed double edge triggered Flip Flop (PIPDETFF). Section V presents simulation results. Section VI concludes the paper

.II. TECHNIQUES OF FLIP-FLOPS FOR LOW POWER SYSTEM

A. *Reducing capacity of clocked load:* One effective way for clocking system of low power design is to reduce the capacity of clocked load by minimizing the number of clocked transistors. The clocked transistor is referred as clocked load. The power consumptions of clocked transistors is higher than that of un-clocked transistor.

B. *Double edge triggering:* This method can be used to save the half of the power on the clock distribution network. It uses the half frequency on the clocks distribution network by cutting the frequency of the clock by one half will halves the power consumption on the clock distribution network.

C. *Low Swing Voltage:* Using low swing voltage on the clock distribution network can reduce the clocking power consumption. The low swing method reduces the power consumption by decreasing voltage in power equation. The low swing clock may leads to performance

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degradation .To prevent the performance degradation due to low swing clock, transistors with low V_t are used for the clocked transistors.

D. Reducing the Switching activity: There are two ways to reduce the switching activity:-

a. *Clock Gating:* When a certain block is Idle, we can disable the clock signal to that block by providing the gate. It saves the power.

b. *ConditionalOperation:* Conditional operation eliminates redundant data transition. When input stays at logic 1 the internal node kept charging and discharging without performing any useful computation. It is referred as redundant data transition.

E. Reducing Short Current Power :The short current power can be reduced by split path technique since n-MOS and p-MOS are driven by separate signals.

III. ANALYSIS OF CONVENTIONAL FLIP-FLOPS ARCHITECTURE

1) *CLOCK BRANCH SHARING _IMPLICIT PULSE (CBS_IP):*CBS_IP is a double edge triggered flip-flop [9]. CBS_IP consists of 21 numbers of transistors. CBS_IP uses 8 clocked transistors and 13 un-clocked transistors. Here P_1, P_2 are pre-charging transistors. CBS_IP has two stages. (N1, N3) (N2, N4) are shared by the First stage and second stage note that a split path which is used to ensure correct functioning after merging. D $_{Input}$ as given in first stage .The Q and Q $_{Bar}$ output are obtained in the second stage.

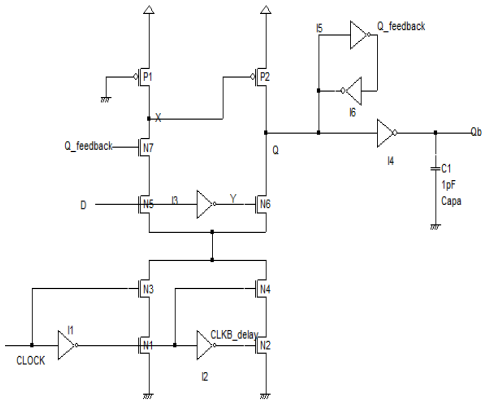

Fig.1 Clock Branch Sharing _Implicit Pulsed Flip-Flop (CBS_IP) (Total of 21 Transistors Including 8 Clocked Transistors).

The double edge triggering operation of the flip flop is as follows. P1 is a pseudo n-MOS. The pseudo n-MOS is always ON p-MOS P1. The pseudo n-MOS in CBS_IP gives advantage of the D and Q $_{Bar}$ have inversed polarity results from conditional discharging technique. It is provide protection from direct noise coupling. Q $_{Feedback}$ is used to control N7.

The first stage operation is follows, when clock rises (clock=1) clock Bar will stay high (clock bar=1) for a small interval of time equal to one inverter delay. In this duration time period, the clock branch (N1 and N3) turn on the flip flop will get in the evaluation period. The other clock branch (N2and N4) is disconnected. When clock falls (clock=0) clock Bar will rise (clock bar=1) and clock bar_ delay will stay high for one inverter delay. In this duration time period, the clock branch (N2 and N4) turn on the flip flop will get in the evaluation period. The other clock branch (N1and N3) is disconnected.

The first stage is responsible for capturing input transitions in the design. The input transition of D goes to 0->1 the internal node X will be discharge causes the outputs Q=HIGH and Q $_{Bar}$=LOW. If the input D stays high, the first stage is disconnected from ground in the evaluation period X is experiencing redundant switching activity. The second stage is capturing the 1->0 input transitions.

In this case the input transition is falling on the pull down network of the second stage to be ON and output nodes Q=0, Q $_{Bar}$=1, respectively. The CBS_IP is using a split path in P2 is driven by X and N6 is driven by Y.

To further reduces the latency, clocked inverters I1 and I2 are placed to driven bottom clocked transistors N1 and N2, respectively. The clocked transistors have a 100% activity factor and consume a large amount of power.

2) CONDITIONAL DATA MAPPING FLIP- FLOP (CDMFF):

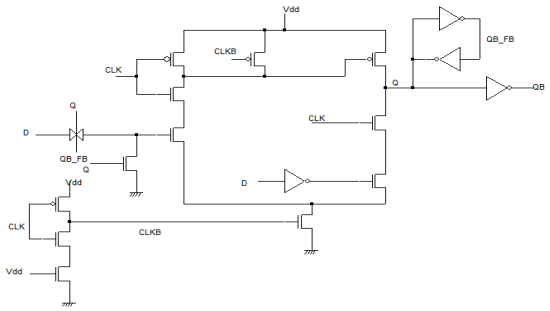

Fig.2 Conditional Data Mapping Flip-Flop(Total of 22 transistors including 7 clocked transistors.)

CDMFF is a double edge triggered flip-flop [10]. It consists of 22 numbers of transistors. It

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uses 7 clocked transistors and 15 un-clocked transistors. Here P_1, P_2 are pre-charging transistors. It has two stages. First stage consists of P_1, N_1, N_2 transistors. The second stage consists of P_3, N_3, N_4 transistors. Data D_{Input} as given in first stage .The Q and Q_{Bar} output are obtained in the second stage. When Data remains 0 or 1 the pre-charging transistors P_1 and P_2 keep switching without useful computation and results in redundant clocking. It is necessary to reduce the redundant power consumption here. Further CDMFF has a floating node on critical path because its first stage is dynamic.

When a clock signal CLOCK transits from 0 to 1, CLOCK-B will stay 1 for a short mean while time. It produces an implicit pulse window for evaluation. If D transits from 0 to 1, the pull down network will be disconnected by N_2 using data mapping scheme (N_5 turns off N_2).If D is 0, the pull down network is disconnected from GND too.

Hence internal node A is not connected with V_{DD} or GND during most pulse windows, it is essentially floating periodically. The dynamic node is un-driven node so it is more prone to noise interruption. If a nearby noise discharges the node A, p-MOS transistor P_3 will be partially on and a glitch will appear on output node Q.

Hence CDMFF could not be used in noise intensive environment. Finally it is difficult to apply the low power techniques introduced in the previous section to CDMFF(for example the clock structure with pre-charging transistors P_1, P_2 in CDMFF makes it difficult to apply double edge triggering.

3)DUAL DYNAMIC NODE HYBRID FLIP-FLOP (DDFF)

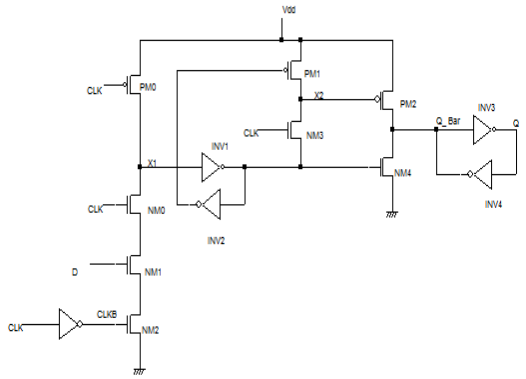

Fig 3.Dual Dynamic node hybrid Flip Flop(Total number of transistor 18 including 6 clocked transistors)

DDFF is a double edge triggered flip flop[10]. DDFF consists of 18 numbers of transistors. DDFF uses 6 clocked transistors and 12 un-clocked transistors. The node X1 is pseudo-dynamic, with a weak inverter acts as a keeper and X2 is purely dynamic. The operation of flip flop can be divided into two phases: 1.evaluation phase, when clock=1 and 2.pre-charge phase, when clock=0.

During the actual latching, 1-1 over-lap of clock and clock _bar in the evaluation period. If D is high prior to this over-lap period, the node X1 is discharged through NM0-NM2. The cross coupled inverter pair INV1-INV2 node X1B to go high and output Q_ Bar to discharge throughout NM4. The node X1 is retained at the low level, by the inverter pair INV1-INV2 for the rest of the evaluation phase where no latching occurs. The node X2 is high through the evaluation phase by the p-MOS transistor PM1. The circuit enters the pre-charge phase, when the clock falls low and the node X1 is pulled high.

If D is zero prior to the over-lap period, the node X1 high and the node X2 is pulled low through NM3 as the clock goes high. Thus the node Q_ Bar is charged high throughout PM2 and NM4 is turned OFF. The end of the evaluation period, the clock falls low, the node X1 high and X2 stores the charge dynamically. The DDFF has many branch paths so the circuit consumes large power.

4)IMPLICIT PULSED DOUBLE EDGE TRIGGERED FLIP FLOP(IPDETFF)

IPDETFF is a double edge triggered flip flop[11]. IPDETFF consists of 23 numbers of transistors. IPDETFF uses 8 clocked transistors and 15 un-clocked transistors. The clock branch sharing topology is constructed by the two pairs of transistors (N5, N7) and (N6, N8). The clock pair (N3, N4) is replaced by the clock allocation tree (N5, N6, N7, N8) to design the implicit pulsed double edge triggered flip flop. The clock branch (N5, N6, N7, N8) is shared by both first stage and second stage of the flip-flop.

The clock branch sharing schemes, less numbers of transistors are used to construct the clock allocation tree for the design and reduce the total power consumption. This is the main advantage of the sharing schemes. The split path technique is one of the most effective power reduction methods. The transistor N2 is presented in the output discharge path. The node Y is drives the n-MOS discharge transistor N2. The node X is only drives the p-MOS transistor P2 of the second stage. The p-MOS and n-

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MOS transistor drives by the separate signals and reduces short circuit power dissipation.

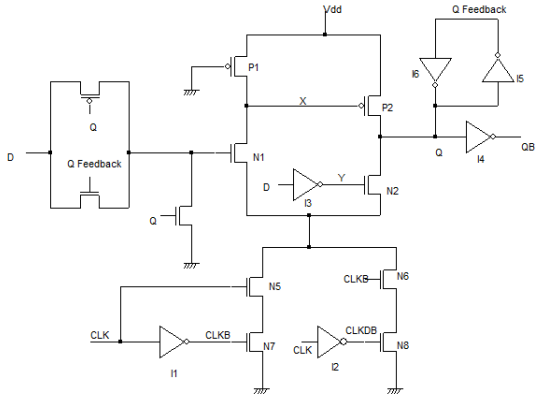

Fig 4.Implicit Pulsed Double Edge Triggered Flip Flop (Total numbers of transistors 23 including 8 clocked transistors)

The first stage of the p-MOS transistor P1 is pseudo n-MOS transistor. The P1 is always on and the internal node X is charged from the power supply VDD through the P1 transistor. The inverter I3 is placed after Q and providing protection from the noise coupling. The operation of the Implicit Pulsed Double Edge Triggered Flip Flop is as follows.

$Q_{Feedback}$ is used to control N4. When clock rises (clock=1), then the clock-bar will stay high for a small internal time which is equal to one inverter delay. During this time period the clock branch (N5 and N7) turns ON at that time remaining clock branch (N6 and N8) is disconnected. When clock falls (clock=0), then the clock-bar is high and clock-D _bar will stay high for one inverter delay. During this time period the clock branch (N6 and N8) turns ON at that time remaining clock branch (N5 and N7) is disconnected. The first latching stage is 0 to 1 data input transition. The internal node X will discharge and outputs Q=1, QB=0.The transistors N4 turns off and the $Q_{Feed-back}$ is equal to 0.

If the D input stays high the latching stage is disconnected from the ground to prevent the switching activity. The second latching stage is 1 to 0 data input transition, the pull down network is ON and outputs Q=0, QB=1. It has floating node problem

IV. PROPOSED IMPLICIT PULSED DOUBLE EDGE TRIGGERED FLIP FLOP (PIPDETFF):

Proposed implicit pulsed double edge triggered flip-flop (PIPDETFF) is a double edge triggered flip –flop. PIPDETFF consists of 22 numbers of transistors. PIPDETFF uses 6 clocked transistors and 16 un-clocked transistors. PIPDETFF has two stages. The data D_{input} as given in the first stage. The Q and Q_B outputs are obtained in the second stage.

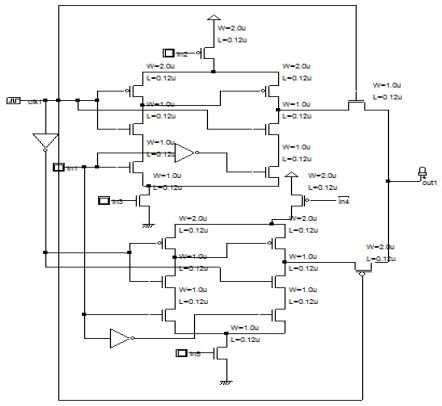

Fig.5 Proposed Implicit Pulsed Double Edge Triggered Flip Flop (total number of transistors 22 including 6 clocked transistors)

The effective methodology of the double edge triggered paradigm and n-MOS transistor logic of the new proposed implicit pulsed double edge triggered flip-flop (PIPDETFF) is proposed. PIPDETFF has power aware technique. The power aware technique is sleep, sleep-bar. The power technique is used which is the part is not working it is goes to idle mode. The power aware technique is reduced power consumption.

The paradigm is consists of the positive edge triggered clocked latch and negative edge triggered clocked latch. The positive edge triggered clocked latch is working when the input D=1, CLOCK=1, Q=1 and negative edge triggered clocked latch goes to idle mode by using sleep, sleep-bar technique.

The negative edge triggered clocked latch is working when the input D=1, CLOCK=0, Q=1 and positive edge triggered clocked latch goes to idle mode by using sleep, sleep-bar technique.

The positive edge triggered and negative edge triggered outputs are going to the second stage of the n-MOS transistor logic. The n-MOS transistor logic is consists of p-transistor and n-transistor. The n-MOS transistor logic is producing the output. The n-MOS transistor logic gate is connecting to the clock. The clock input is HIGH n-transistor is ON, and the

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clock input is LOW p-transistor is ON. The proposed double edge triggered flip flop operations is explained in fig.7, fig.8, fig.9, fig.10.

V .SIMULATION RESULTS:

The simulation results were obtained from DSCH & MICROWIND3.1 simulations in 0.12µm CMOS technology at room temperature. V_{DD} is 1.8 V. A clock frequency of 250 MHz is used. Performance parameters such as Area and Power are obtained from layout simulation.

The TABLE I: shows a comparison of the flip-flop characteristics in terms of power and area. Fig 6: shows the layout of our proposed double edge triggered flip-flop.

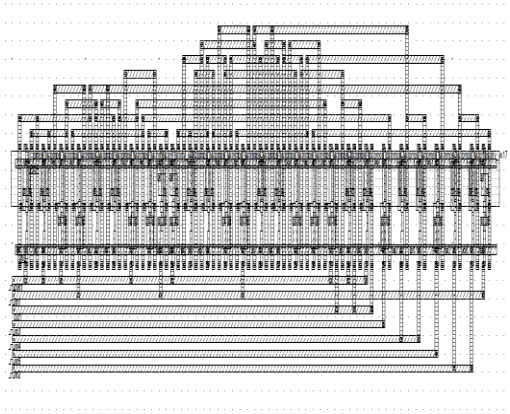

Fig 6: physical layout of proposed implicit pulsed double edge triggered flip flop (Area=576µm^2)

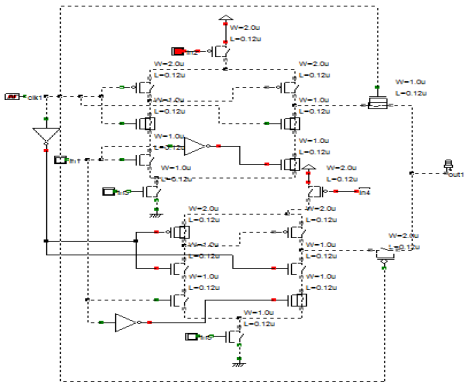

Fig 7: Operation-1: (input data D=0, clock=1, clock _bar=0; output Q=0, Q_{Bar}=1)

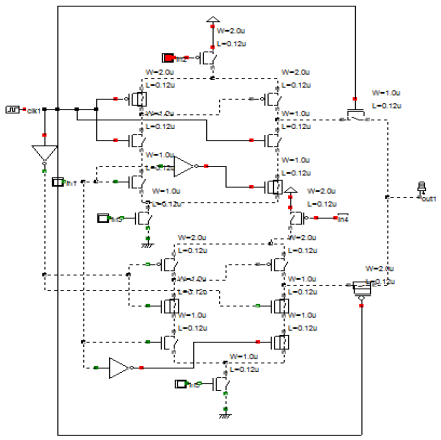

Fig 8: Operation-2: : (input data D=0, clock=0, clock _bar=1; output Q=0, Q_{Bar}=1)

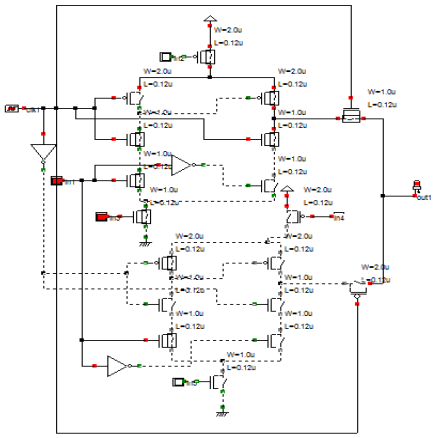

Fig 9: Operation-3: (input data D=1, clock=1, clock _bar=0; output Q=1, Q_{Bar}=0)

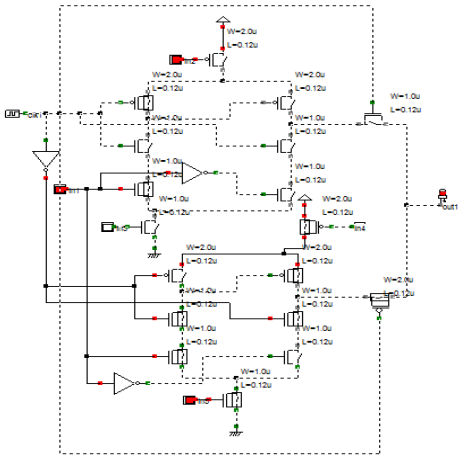

Fig 10: Operation - 4: (input data D=1, clock=0, clock _bar=1; output Q=1, Q_{Bar}=0)

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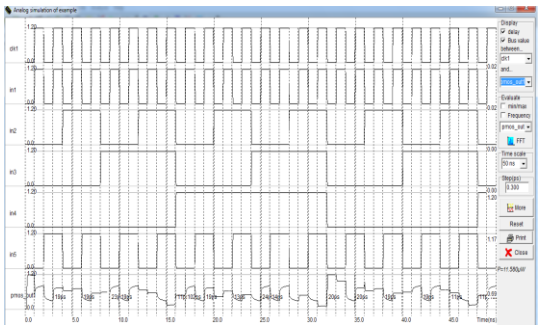

Fig 11: output waveform of Proposed implicit pulsed Double Edge Triggered Flip Flop (power consumption=11.580µw)

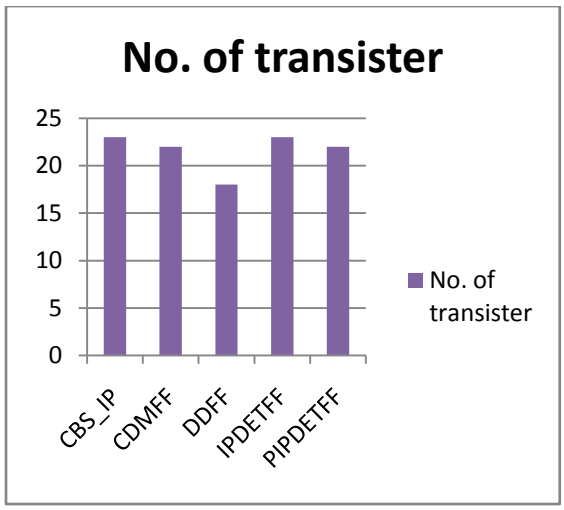

Fig 12: Comparison of no. of transistors

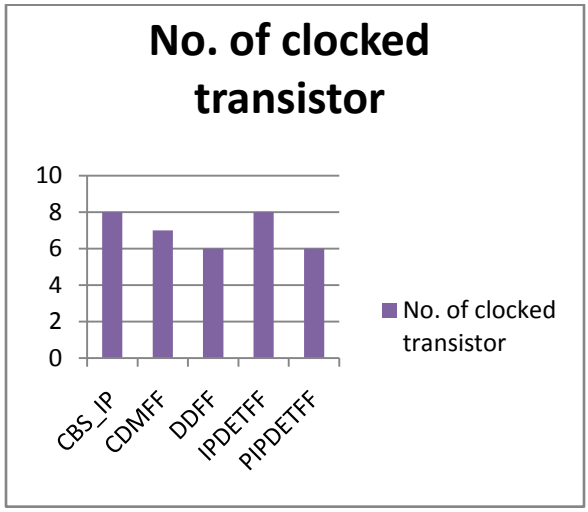

Fig 13: Comparison Of Clocked Transistors

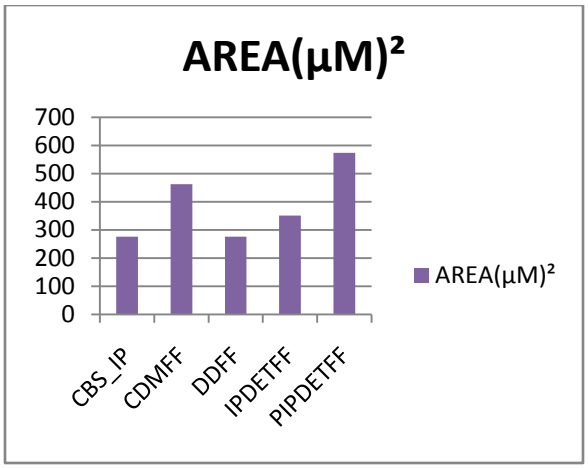

Fig 14: Comparison Of Area

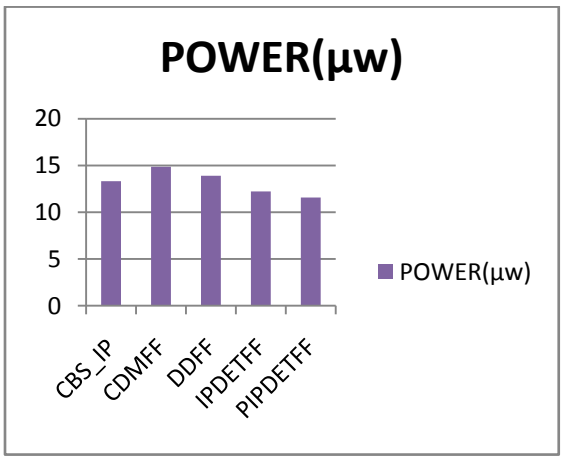

Fig 15:Comparison Of Power

Table 1: Comparison Of Flip-Flop Performance

Flip-flop	No. of transistor	No. of clocked transistor	Area(µm)^2	Power (µw)
CBS_IP	23	8	276	13.306
CDMFF	22	7	462	14.867
DDFF	18	6	276	13.897
IPDETFF	23	8	351	12.226
PIPDETFF	22	6	574	11.580

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VI. CONCLUSION

In this paper some design techniques for clocked latches are reviewed[7]-[8] and [12]-[13]. One effective method, reducing the power and number of clocked transistor by introducing the double edge triggered clocked flip-flop. By following the approach, the effective methodologies such as double edge triggered paradigm and n-MOS transistor logic the new IPDETFF is proposed. This proposed design consumes less power and achieves 6.52% to 22.11%. The power reduction compared with the conventional flip-flop.

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