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A Novel VLSI Architecture for FDMA-MIMO Detector

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***Abstract*- Now- a- days, the communication industry field is mainly focused on high data transfer and more channel capacity in mobile communication and to improve the spectrum efficiency, capacity of wireless network and reliability of the link. The area efficient architecture of 4×4 16-QAM Multiple Input Multiple Output (MIMO) detectors are mainly used for the wireless communication. An area-efficient symbol detector is proposed for MIMO communication systems with reduced buffer memory architecture. To design SC-FDMA MIMO received signal detector architecture using Euclidean distance technique. In this paper the internal MIMO detector get modified architecture and to improve the performance level. Proposed system is to increase throughput value, reduce the latency level and to reduce the power consumption level for channel allocation process.**

Index Terms- Euclidean distance, (MMSE) Minimum Mean Square Error, Space Time Block Code (STBC), Log Likelihood Ratio (LLR).

I. INTRODUCTION

Wireless communication is important domain were it requirements get enlarged day to day. Multiple Input Multiple Output it has two domains such as diversity and multiplexing. In diversity dual array provides diversity at both transmitters and receiver side. Here Maximal ratio combining method is used. MIMO used multi path effect as a positive feature. We are using two way sorting approach bit error rate get reduced. A detection scheme is proposed for MIMO SC-FDMA system to reduce the complexity especially for large constellation sizes.

[3]ASIC design for high-throughput data detection in single carrier frequency division multiple access (SC-FDMA)-based large-scale MIMO systems, such as systems building on future 3GPP LTE-Advanced standards. To reduce the complexity of soft-output data detection in systems having many numbers of antennas at the Base Station (BS), the proposed detector builds upon a truncated Neumann series expansion to compute the necessary matrix inverse to reduce complexity. This technology provides improvements in spectral efficiency, link reliability, and coverage over conventional (small-scale) MIMO systems.

Single-carrier[1] frequency-division multiple access (SCFDMA), a modified form of orthogonal frequency-division multiple access (OFDMA), is a technique for high data rate uplink communications in future cellular systems. When compared with OFDMA, SC-FDMA has similar throughput and essentially the same overall complexity. An advantage of SC-FDMA is very low peak-to average power ratio (PAPR), than OFDMA and suitable for uplink. SC-FDE is suitable for high data rate transmission. Nonlinear time domain equalizers and DFE are having good performance and complexity tradeoffs.

[8]Two minimum mean square error (MMSE)-based multiuser detectors, called the combined MMSE and Maximum Likelihood (MMSE-ML) multiuser detector and the combined MMSE and Successive Interference Cancellation (MMSE-SIC) multiuser detector, for an uplink space-time block coded orthogonal frequency division multiplexing (STBC-OFDM) system. Both detectors provide significantly improved bit error rate (BER) over the conventional MMSE multiuser detector while requiring the same complexity order. Moreover, the combined MMSE-ML detector exhibits better BER than the combined MMSE-SIC, particularly, in a system with a small number of users. It can reduce the computational complexity of linear soft-output detection, the size of the architecture consumes more power.

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In this paper, the system uses single-carrier frequency division-multiple access (SC-FDMA) for multiple-input multiple-output (MIMO) detector. This technique is to optimize the symbol detector circuit complex level using two- way sorting approach. The proposed 4×4 MIMO detector is synthesized and simulated using the maximum mean square error detection algorithm. This algorithm is to reduce the hardware complexity.

II. . BASIC BLOCK DIAGRAM

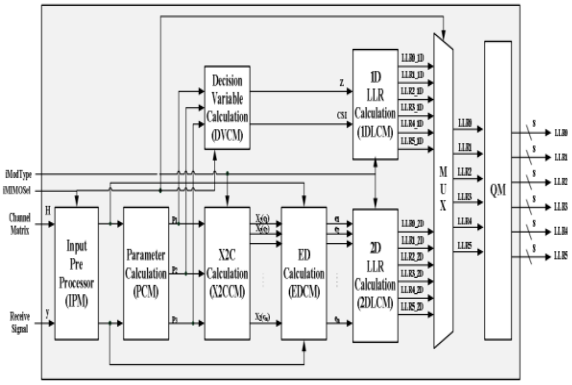


Fig.1.Block diagram of MIMO detector.

The signal which is from detector circuit is passed through IPM block. In Parameter Calculation Module received signal from IPM get integrated. Identification the signal process also takes place. ED calculation module the function level gets checked and ED distance level also calculated. In LLR calculation the energy level of the message signal is identified.

A. . DETECTOR FUNCTION:

8-bit MIMO detector architecture is used to the collect the signal into receiver side. MIMO detector architecture is placed in channel receiver section and this section is consisting of more number of internal sub modules arte place in signal detection process. So we implement the more number of techniques to reduce the circuit complexity.

B. INPUT PREPROCESSING MODULE(IPM)

The Input Pre-Processing architecture is consisting two type of channel matrixes and to select the channel type due to signal detection process.The STBC and non-STBC channel type are used to detection work. The Space Time Block Code(STBC) channel is used to store the received date and to transfer the next module.Space time wireless technique required multiple antenna in both transmitter and recevier side in order to improve wireless performance.The non- STBC channel is used to directly passing the detecting received signal level. The controller block is to direct the signal based on energy levels. Channel matrix get passed through STBC and Non-STBC block.

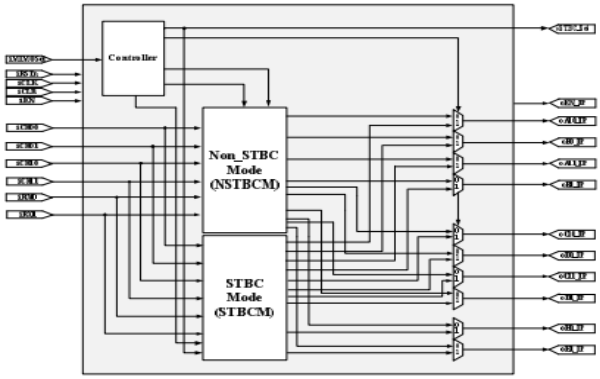


Fig.2. Block diagram of IPM.

C. .PARAMETER CALCULATION MODULE

This parameter module is to optimize the circuit complexity level based on multiplication and square block architecture. The parameter calculation module is to identify the received signal parameter final output values. Here the detected signal gets integrated by using complex multiplier for the carrier signal, and square adder is for the received signal. XOR gate is to analysis the minimum and maximum strength of the signal. The analyzed value of the signal gets stored in register. Three parameters get analyzed the circuit.

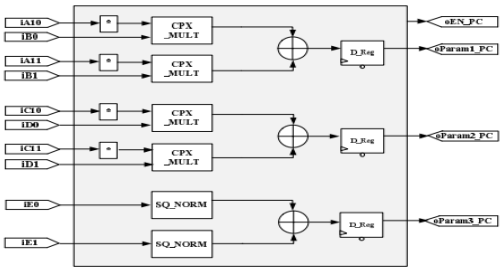


Fig.3. Block diagram of Parameter Calculation Module.

D. ED WITH SORTER MODULE:

The parameter signal is passed through the Euclidean distance calculation process. Here symbol identification process takes place. In order to check minimum and maximum function level. After analyzing the energy level of the received signal, all minimum valued signals get combined by the sorter module section. This subset can be efficiently selected using the complex Schnorr Euchner (SE) enumeration technique, which is an on-demand technique to enumerate the constellation points in the order of non-decreasing ED values. To produce the initial estimate and first symbol MMSE output value can be rounded to the nearest value. The Bit Error Rate (BER) performance loss is negligible.

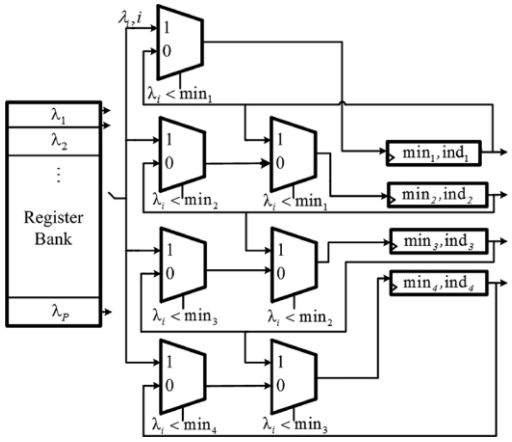


Fig.4. The detailed structure of Sorter Module.

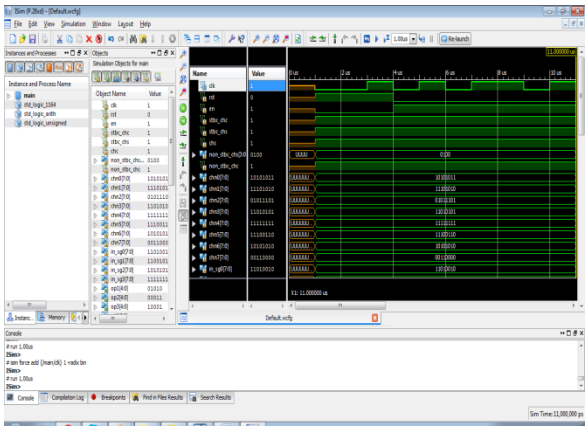
E. . LLR CALCULATION MODULE:

The log-likelihood ratios (LLR) value is calculating the MIMO detector architecture. The LLR calculation value is used to identify the energy level in received detection signal. The MIMO detector will have to generate a soft decision based on the transmitted symbols. The architecture performs the detection process in clock cycles. Since clock cycles are required to produce the EP metrics and their corresponding constellation points along with indices indicating the symbols selected as the erroneous symbols. The register banks have the value of the initial estimation. The comparator blocks compare the initial estimate and eventually the final decisions will be stored in the register bank.

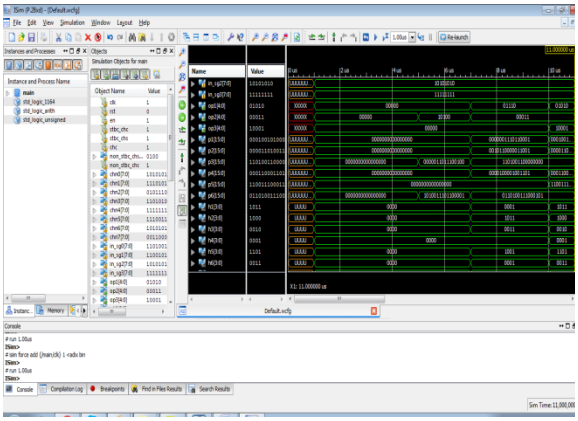
III. . SIMULATION RESULT

Parameter's calculated.	16-QAM Soft value	
	Previous system	Proposed system
Nr LUT's	2475	764
Nr Slice Registers	5871	1120
Delay time(ns)	6.9	5.7
Throughput(Mbps)	576	1403.5
Clock frequency[MHz]	144	173.503
Power[mW]	115.4	99

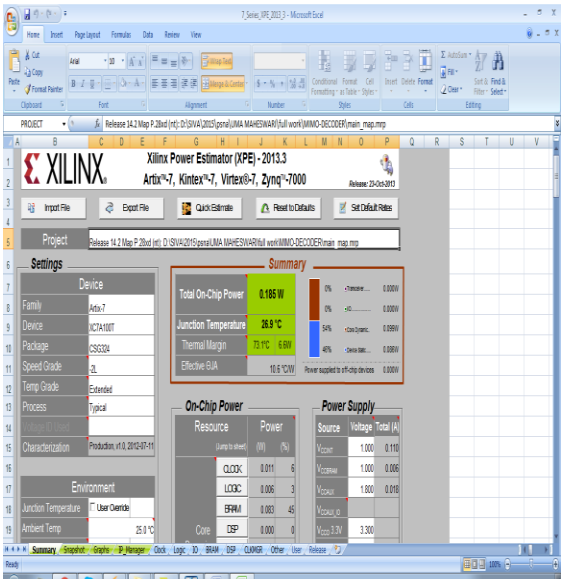
Tab.1 Comparison of parameters.



According to the simulation results, that larger values result in a better MMSE performance. It's computational value complexity is SNR dependent. Several simulations were performed to determine the fixed point effect of the variables on the overall design performance.



IV. . POWER CALCULATION:



V. . CONCLUSION

In this paper, the proposed system performs efficient data detection process by increased throughput up to 1403.5 Mbps. And area occupied by the circuit also reduced by the number of elements gets reduced. And it also leads to saving hardware cost. The delay time also get reduced to 5.7 ns. This work is to optimize the circuit complexity level in communication domain.

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