ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 4, Issue 11, November 2015

CPLD Based Design and Implementation of Pipelined 32-bit RISC Processor with Floating Point Unit

B.NAGARAJU[1], J. VIJAY KUMAR[1], M. VASUBABU[2] & T. RAMANJAPPA[3]

Abstract — **This paper presents design and implementation of CPLD (Complex Programmable Logic Device) based 32-bit RISC processor with floating point unit and pipelined architecture. This system architecture is able to prevent pipelining from flushing when branch instruction occurs and able to provide halt support. Through this the speed of the operation as well as overall performance can be improved. The necessary code is written in the hardware description language Verilog HDL. The CPLD used in the present work is XC9572 manufactured by Xilinx. The software tools used for building and testing the modules in the present work is Xilinx ISE 9.1i and Modelsim software tool is used for analyzing simulation results. This system performs certain operations like addition, subtraction, multiplication and division.**

***Index Terms*— RISC processor, XC9572, ISE 9.1i, Modelsim and ADM board.**

I INTRODUCTION

RISC is a microprocessor design approach using simple instructions. Though it may seem less effective for a computational task to be executed with many simple instructions rather than a few complex instructions, the simple instructions take fairly the same amount of time for execution, making them ideal for pipelining [1]. Now-a-days, computer and mobile phone are indispensable tools for most of everyday activities. This places an increasing burden on the embedded microprocessor to provide high performance while retaining low power consumption and small die size, which increases the complexity of the device. However, as products grow in complexity, more processing power is required while the expectation on battery life also increases. The trend in the recent past shows the RISC processors clearly outsmarting the earlier CISC processor architecture. One advantage of RISC is that they can execute their instructions very fast because the instructions are so simple [2]. RISC is a type of microprocessor that has a relatively limited number of instructions and is designed to perform millions of instructions per second. This paper describes a CPLD based 32-bit general purpose 4 stage pipelined processor with floating point unit. It has a complete instruction set, program and data memories, general purpose registers and a simple Arithmetic and Logical Unit with single precision floating point arithmetic operations. In this design most instructions are of uniform length and similar structure, arithmetic operations are performed and the resultant value is stored in the memory and retrieved back from memory when required.

The other elements that define a RISC processor [3] are the following:

- ❖ Single-cycle operation aids in fast execution of simple functions
- ❖ Store architecture implemented due to the desired single-cycle operation
- ❖ Hardwired control provides for the fastest possible single-cycle operation
- ❖ Relatively few instructions and addressing modes make it easy for the control unit to interpret instructions
- ❖ Fixed instruction format makes decoding of instructions fast and easy
- ❖ More compile-time effort offers opportunity to explicitly move static run-time complexity into compiler

II HARDWARE DETAILS

A. Base board details

The ADM Base Board acts as a universal CPLD/ FPGA/µP reconfigurable implementation platform to allow rapid and interactive prototype development [4]. The board houses a plug-in daughter board containing a target FPGA/CPLD/µP device. Daughter boards can be easily swapped to provide support for multi-vendor devices available in DIL, PLCC, TQFP, PQFP packages up to 240 pins. Fig.1(a) & Fig.1(b) show the photographs of the CPLD base board and daughter board respectively used for the present work.

Fig.1 Photograph of the CPLD base board

B.Nagaraju, S.K University College of Engineeringg. & Technology. S.K.University, Anantapur,India.
J. Vijay Kumar, S.K University College of Engineering. & Technology. S.K.University, Anantapur,India.
M.. Vasubabu, Dept. of Applied Sciences, St. Ann's College of Engineering. & Technology Chirala, India.
T.Ramanjappa, Dept. of Physics, S.K.University, Anantapur, India.

Fig.1(b) Photograph of the daughter board

B. Daughter Board Details

The Daughter board contains Xilinx CPLD (XC9572), which can be plugged on to the base board [5]. XC9572 device supports serial configurations, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the slave parallel mode. It also has four sets of 20x2 female berg connector for plugging on to the base board and JTAG pins for in-circuit programming.

The XC9572 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration [6]. It is comprised of eight 36V18 function blocks, providing 1,600 usable gates with propagation delays of 7.5ns. Power dissipation can be reduced in the XC9572 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

III ARCHITECTURE OF THE DESIGN

RISC is designed using the Hardware Description Language Verilog HDL. Machine instructions are implemented directly in hardware. The architecture of 32-bit pipelined RISC processor consists of instruction fetch, branch prediction, instruction decode, execute, memory read/write back, instruction set and floating point unit. Pipelining technique allows for simulations execution of parts or stages of instructions more efficiently. With a RISC processor, one instruction is executed while the following instruction is being fetched. By overlapping these operations, the CPU executes one instruction per clock cycle, even though each instruction requires three cycles to be fetched, decoded, and executed [7]. 32-bit pipelined RISC processor with Floating Point Unit is shown in Fig.2.

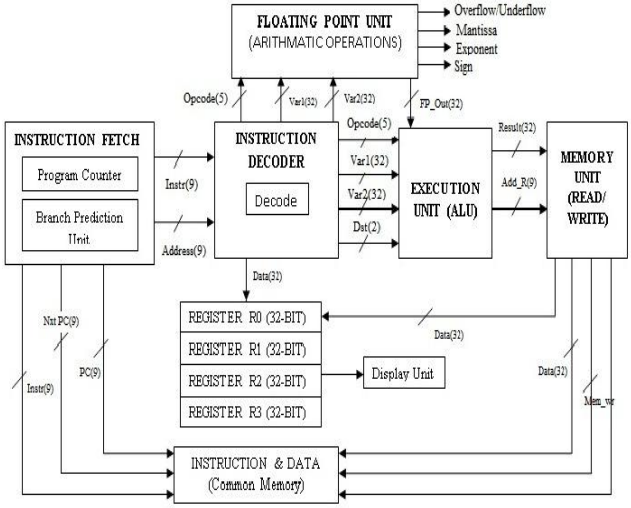

Fig.2 Architecture of 32-bit RISC Processor with FPU

The pipeline stages for different type of instructions are processed as follows, in the fetch stage; instructions are fetched at every cycle from the instruction memory whose address is pointed by the program counter (PC). During the decode stage, the registers are read from the register file and the opcode is passed to the control unit which asserts the required control signals. Sign extension is also done for the calculation of effective address. In the execute stage, for register type instruction, the ALU operation and also floating point arithmetic operations are performed. The load and store instructions write to and read from the data memory in the memory stage while the ALU results and the data read from the data memory are written in to the register file by the register type and load instructions respectively in the write-back stage. There are basically three types of instructions namely arithmetic & logical instructions with floating point unit instructions, Load/Store instructions and Branch Prediction instructions.

VI FLOATING POINT UNIT

Floating point computational logic has long been a mandatory component of high performance computer systems as well as embedded systems and mobile applications. The advantage of floating point representation over fixed-point and integer representation is that it can support a much wider range of values. In the present work 32-bit FPU is incorporated, which supports single precision IEEE-754 format. The IEEE-754 standard defines a single as 1 bit for sign, 8 bits for exponent and 23 bits for mantissa [8]. Most of today's computers are equipped with specialized hardware that performs floating-point arithmetic with no special programming required. The CPLD implementation of 32-bit single precision floating point unit provides addition, subtraction, multiplication and division operations for any two operands of the same format. The destination format shall be at least as wide as the operands format.

V SIMULATION RESULTS

The simulation results of instruction fetch unit, instruction decode unit, execution unit, floating point unit and 32-bit RISC processor have been verified by using Modelsim. The simulation waveforms of all the units are shown in Fig.3 to 7.

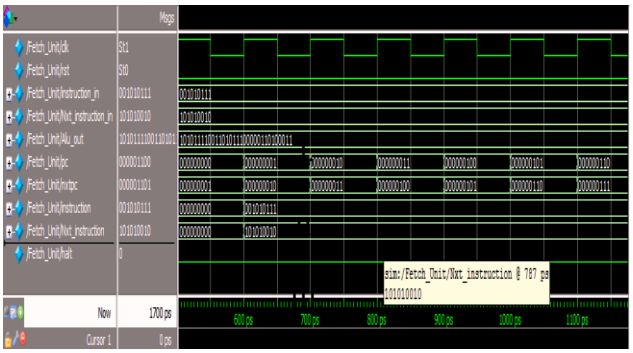

Fig.4 Simulation Waveform of Instruction Fetch Unit

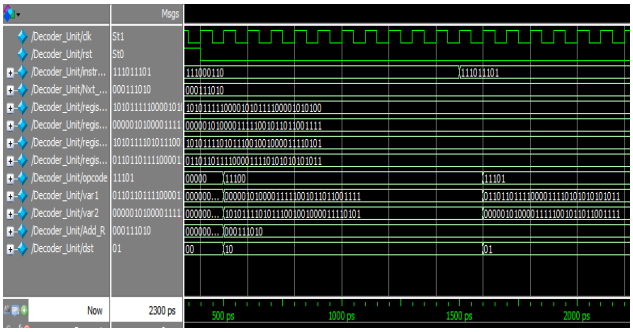

Fig.5 Simulation Waveform of Instruction Decoder Unit

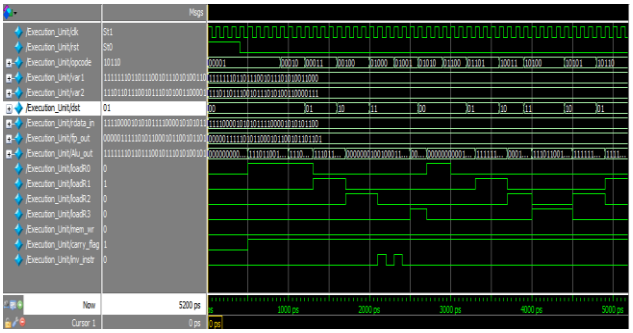

Fig. 6 Simulation Waveform of Execution Unit

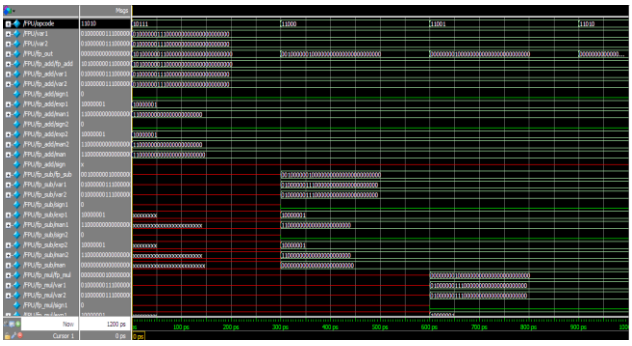

Fig. 8 Simulation Waveform of 32-bit Floating point unit

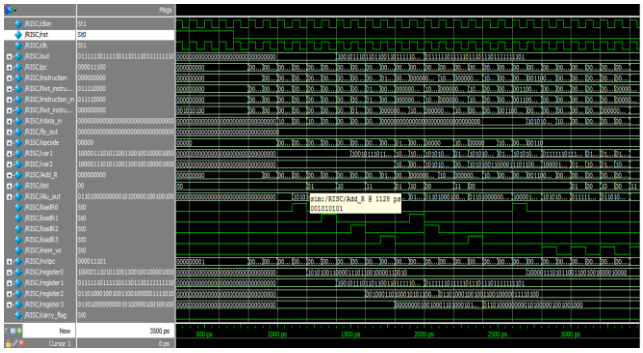

Fig.9 Simulation Waveform of 32-bit RISC Processor

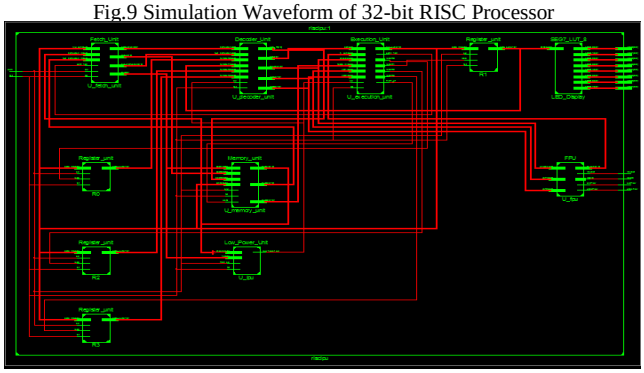

Fig.10 RTL Schematic view of Proposed Processor

VI CONCLUSION

CPLD based pipelined 32-bit RISC processor with Single Precision Floating Point Unit is designed and implemented on Xilinx XC9572. On which Arithmetic operations, Branch operations, Logical functions and Floating Point Arithmetic Operations are verified. Pipelining would not flush when branch instruction occurs as it is implemented using dynamic branch prediction. This will increase flow in instruction pipeline and it results in high effective performance. This architecture has become indispensable and increasingly important in many applications like signal processing, graphics and medical

VII REFERENCES

[1] C. Hamacher, Z. Vranesic, and S. Zaky, *Computer Organization fifth edition*. Boston: McGraw-Hill Publishing, 2002.

[2] J. Poornima, G.V.Ganesh, M. Jyothi, M. Shanti and A.Jhansi Rani,"Design and implementation of pipelined 32-bit Advanced RISC processor for various D.S.P Applications", Proceedings of International Journal of Computer Science and Information Technology, ISSN: 3208-3213, Vol-3(1), June-2012.

[3] R.P. Colwell, C.Y. Hitchcock III, E.D. Jensen, H.M. Brinkley Sprung, and C.P. Kollar, "Instruction sets and beyond: computers, complexity, and controversy," *IEEE Computer*, 1986..

[4] Spartan-3 FPGA Family: Complete Data Sheet DS099, 2009.

[5] ADM TKB108 User Manual-XC95xx D-Board, Applied Digital Microsystems, Mumbai, http://www.admlindia.com.

[6] XC9572 In-System Programmable CPLD DS065, 2006. http://www.xilinx.com/support/documentation/data_sheets/ds065.

[7] Preetam Bhosle, Hari Krishna Moorthy," FPGA Implementation of Low Power Pipelined 32-bit RISC Processor", Proceedings of International Journal of Innovative Technology and Exploring Engineering , ISSN: 2278-3075, Vol-1, Issue-3, August 2012.

[8] http//en.wikipedia.org/wiki/single-precision_floating-point_format