

## DESIGN OF CMOS BASED ADC FOR LOW POWER CONSUMPTION

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**Abstract:** Successive Approximation analog-to-digital converter (ADC) implemented in a conventional 90nm CMOS technology with low power consumption. In modern era, VLSI design is one of the paradigms to have high speed, less power consumption, effective use of space, easily available productivity and mobility. Low power high speeds ADC can be design using VLSI. ADCs are key design blocks in modern microelectronic digital communication systems. With the fast advancement of CMOS technology, more & more signal processing functions are implemented in the digital domain for low cost, low power consumption, higher yield, & higher reconfigurability. This design is suitable for standard CMOS technology with low power low-cost VLSI implementation. The power consumption of the ADC is 2.59 mW at 1.2V supply. The sampling frequency of the ADC IS 2.1GHz. CMOS layout and simulation is drawn by using Microwind 3.1 software.

**Keywords:** CMOS, Comparator, SAR, Low Power Consumption.

### I. INTRODUCTION

An Analog-to-Digital Converter (ADC) is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude. The conversion involves quantization of the input, so it necessarily introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result is a sequence of digital values that have converted a continuous-time and continuous-amplitude analog\_signal to a discrete-time and discrete-amplitude digital\_signal.

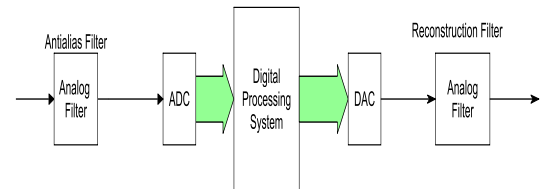


Fig.1: Analog to Digital Converter

The electronic filter placed before an ADC is called antialias filter. It is used to remove the frequency components above one half of the sampling rate that would alias during the sampling. The electronic filter placed after a DAC is called reconstruction filter. It also eliminates the frequency above the Nyquist rate.

In this, a brief overview of SAR ADC is provided to be effectively used in communication domain. Basically the objective of this project is to design the high speed ADC and which consume low power. So, the proposed work is to design such type of ADC.i.e.SAR ADC with high speed and low power consumption.

### II. RELATED WORK

In [1] A 10-bit SAR ADC for biomedical application was presented. The proposed SAR ADC achieves rail-to-rail input range and low power consumption. A Digital-to-Analog Converter (DAC) using C-2C capacitor array and dynamic comparator was used for low power consumption. It was realized in 0.18um standard CMOS technology. In [2] the design and implementation of 4-bit time interleaved SAR ADC for UWB application. They implemented the ADC in 0.18um CMOS technology and had total power consumption of 23.3mw. In [3] SAR ADC implemented in a conventional 0.18um CMOS technology with low voltage. The SAR composite of sample-and-hold dummy switch compensation was employed,

comparator is low voltage latched and realized. In [5] A 10-bit dual-channel pipelined flash-successive approximation register (SAR) analog-to-digital converter (ADC) for high speed application was presented. The prototype ADC fabricated with two channels for high operating speed, and each channel adopts pipeline flash-SAR architecture for low power and small area.

### III. SYSTEM ARCHITECTURE

A successive approximation ADC is a type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion. The successive-approximation A/D converter consists of three main components an analog comparator, a DAC, and a successive-approximation register (SAR) all of which are connected in a feedback arrangement shown in Fig.2

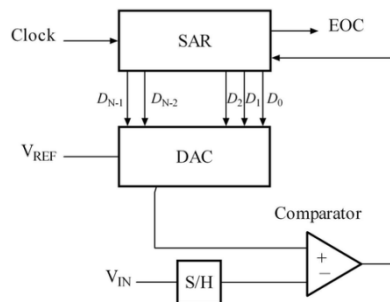


Fig.2: SAR ADC

#### A. Successive Approximation Algorithm

SAR ADC employs a successive approximation algorithm to convert analog input to a digital code successively. In other word, one bit is determined in each clock cycle using binary search algorithm.

For the operation of SAR ADC, consider a 4-bit ADC as shown in fig.3. In the first clock cycle DAC voltage is set to half of  $V_{ref}$  by setting the code to 1000, then the input voltage is compared to  $V_{ref} / 2$  and based on the comparison result, MSB is defined. If the  $V_{in} > V_{ref} / 2$  the MSB will not be

changed and will remain at one. In the next clock cycle the DAC input is set to 1100 and again  $V_{in}$  is compared to  $3V_{ref}/4$ .  $D_2$  retains its value since  $V_{in} > 3V_{ref}/4$ . For the next bit the DAC input is set to 1110. Based on comparison,  $D_1$  is reset to zero since  $V_{in} < 7V_{ref}/8$  and finally for defining LSB, the DAC input is set to 1101.  $D_0$  is one because  $V_{in} > 13V_{ref}/16$ . Therefore, the analog input is converted to the digital code 1101 in four clock cycles.

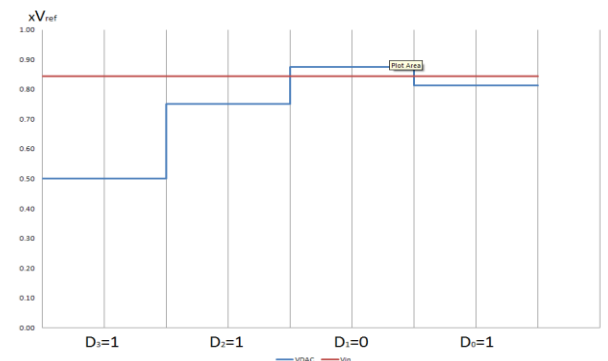


Fig 3: 4-bit SAR ADC Operation

#### B. Sample and Hold Circuit

In general, Sample and hold circuit (SHC) contains a switch and a capacitor. In the tracking mode, when the sampling signal is high and the switch is connected, it tracks the analog input signal. Then, it holds the value when the sampling signal turns to low in the hold mode.

Sample and hold circuit (SHC) mainly used in ADC. It samples analog input signal & holds value between clock cycles. Stable input is required in many ADC topologies, which is provided by sample and hold circuit. it reduces ADC-error caused by internal ADC delay variations. Sometimes, it referred as Track and Hold (T/H). The important parameters of S/H circuit are: hold step, signal isolation in hold mode, input signal tracking speed in sample mode, droop rate in hold mode, aperture jitter. The basic schematic of sample and hold circuit is as shown in fig.6.8.

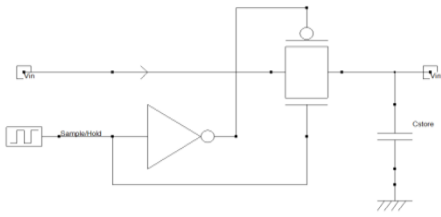


Fig.4: Sample and Hold Circuit

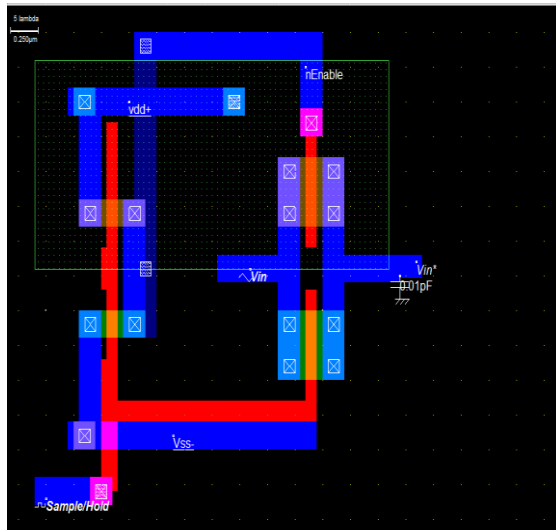


Fig.5: CMOS layout of Sample and Hold Circuit

### C. Comparator

Comparator is the only analog block of a SAR ADC and performs the actual conversion. It compares the analog sampled input to the analog output of the DAC and generates digital output of '0' or '1' which will be used in the SAR logic. Accuracy and speed of the comparator are two important factors. The comparator need to resolve voltages with small differences. The offset voltage of the comparator employed in SAR ADC is translated to the transfer characteristic of the ADC thus will not affect the linearity of ADC.

The requirements of the comparator are speed and accuracy. Comparator offset does not affect overall linearity as it appears as an offset in the overall transfer characteristic. In addition, offset-cancellation techniques are usually applied to reduce the comparator offset. Noise, however, is a

concern, and the comparator is usually designed to have input-referred noise less than 1 LSB. Additionally, the comparator needs to resolve voltages within the accuracy of the overall system. It needs to be as accurate as the overall system. The basic schematic of comparator is as shown in figure 8:

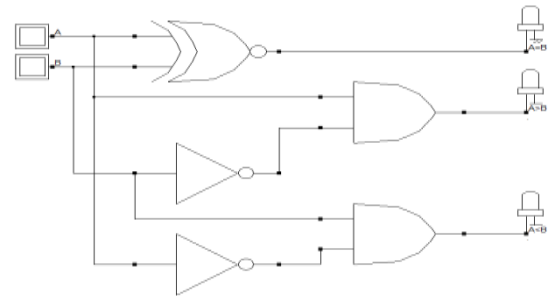


Fig.6: Basic schematic of Comparator

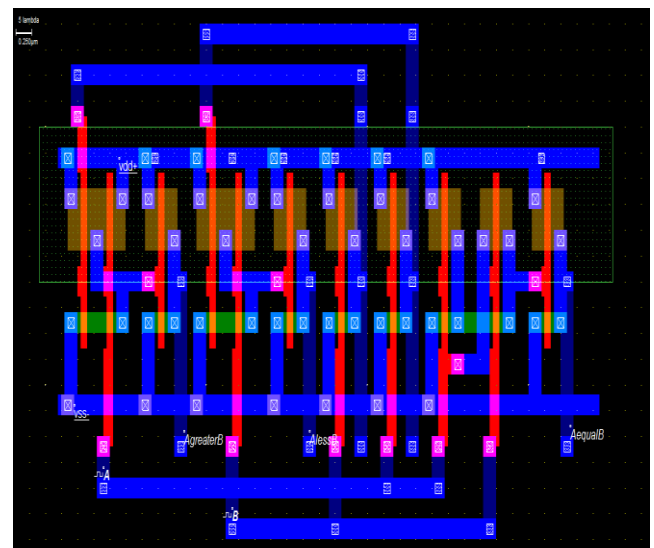


Fig.7: CMOS layout of Comparator

### D. Successive Approximation Register(SAR)

Successive Approximation Register (SAR) control logic determines each bit successively. The SA register contains N bit for an N-bit ADC. There are 3 possibilities for each bit, it can be set to '1', reset to '0' or keeps its value.

In the first step, MSB is set to '1' and other bits are reset to '0', the digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared to the sampled input.

Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output of the DAC, the MSB remains at ‘1’, otherwise it is reset to ‘0’. The rest of bits are determined in the same manner. In the last cycle, the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+1 clock cycles to perform a conversion.

SAR is a combination of counter and combinational logic.

*Counter*

Counters are sequential circuits that cycle through some states. They can be implemented using flip-flops.

*a. Ring Counter:*

Ring counter formed by the feedback connection in a ring. Ring counter are implemented using shift registers. It is essentially a circulating shift register connected so that the last flip-flop shifts its value into the first flip-flop. There is usually only a single 1 circulating in the register, as long as clock pulses are applied. (Starts 1000->0100->0010->0001 repeat)

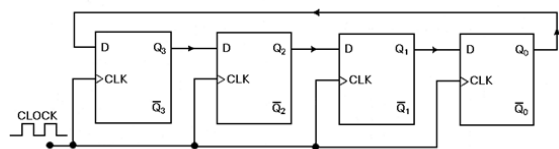


Fig.8: Ring counter

*b. Pass Transistor:*

When an nmos and pmos is used alone as an imperfect switch, we sometimes call it a Pass transistor. By combining an nmos and a pmos transistor in parallel we obtain a switch that turns on when a ‘1’ is applied to g in which ‘0’s and ‘1’s are both passed in acceptable fashion. it is term as a transmission gate or pass gat. When used as a pass transistor the device may conduct current in either direction.

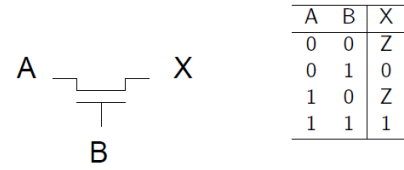


Fig.9: Pass transistor and its truth table

*E. Digital to Analog Converter (DAC):*

An R–2R Ladder is a simple and inexpensive way to perform digital to analog conversion, using repetitive arrangements of precise resistor networks in a ladder like configuration. A resistor ladder is an electrical circuit made from repeating units of resistors.

A basic R–2R resistor ladder network is shown in Figure.... Bit  $a_{n-1}$  (most significant bit, MSB) through bit  $a_0$  (least significant bit, LSB) are driven from digital logic gates. Ideally, the bit inputs are switched between  $V = 0$  (logic 0) and  $V = V_{ref}$  (logic 1). The R-2R network causes these digital bits to be weighted in their contribution to the output voltage  $V_{out}$ . Depending on which bits are set to 1 and which to 0, the output voltage ( $V_{out}$ ) will have a corresponding stepped value between 0 and  $V_{ref}$  minus the value of the minimal step, corresponding to bit 0. The actual value of  $V_{ref}$  (and the voltage of logic 0) will depend on the type of technology used to generate the digital signals.

For a digital value VAL, of a R–2R DAC with  $N$  bits and 0  $V/V_{ref}$  logic levels, the output voltage  $V_{out}$  is:

$$V_{out} = V_{ref} \times VAL / 2^N.$$

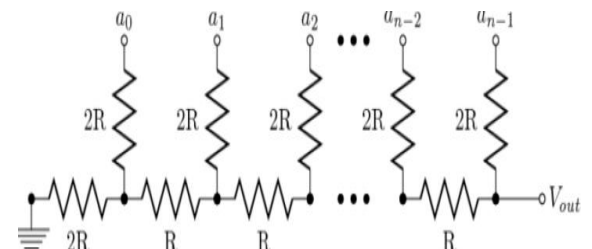


Fig.10: n-bit R-2R ladder network

*F. CMOS Layout of SAR ADC:*

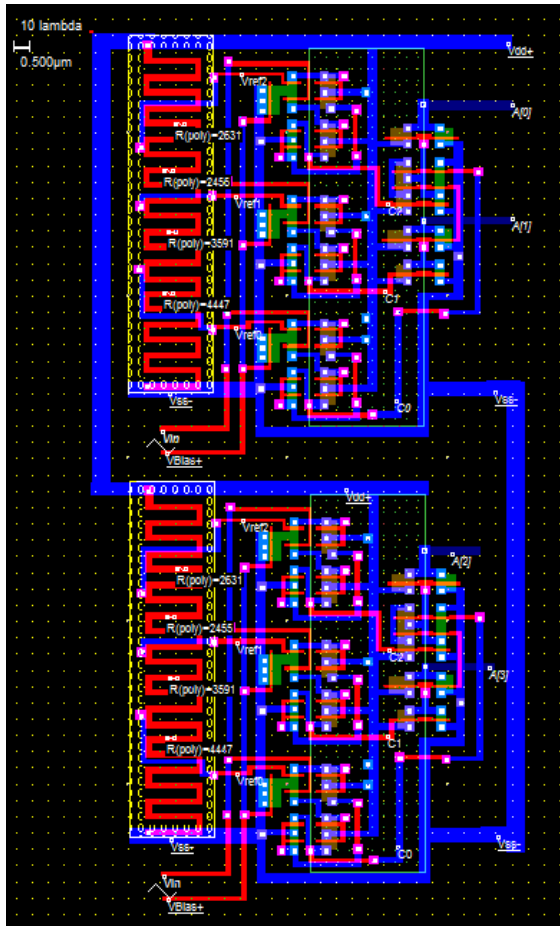


Fig.11: CMOS layout of SAR ADC

IV.RESULT & DISSCUSSION

The simulation result includes the output waveform of the various block of system. Microwind 3.1 simulation tool is used to design the layout and simulate the layout with respect to various parameters. The simulation result for the various blocks of successive approximation ADC is given below:

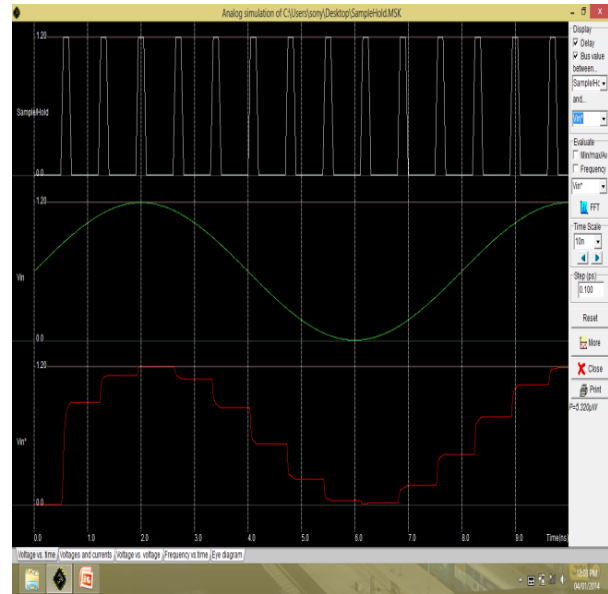


Fig.12: Simulation result for Sample and Hold circuit

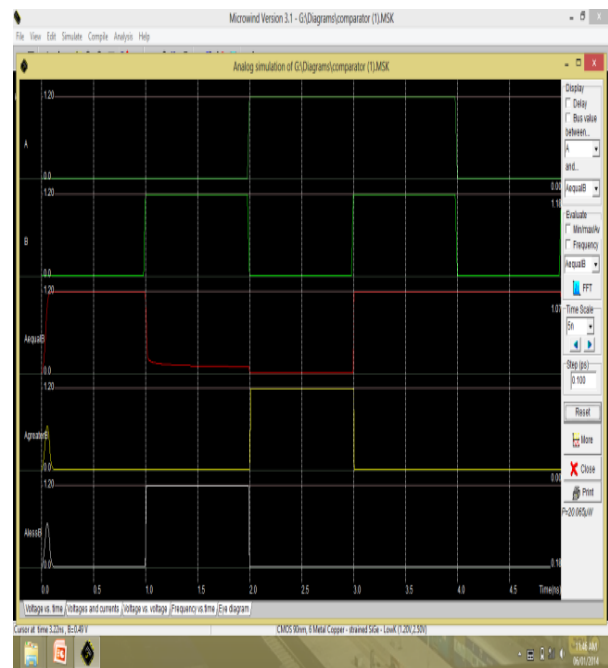


Fig.13: Simulation result for Comparator

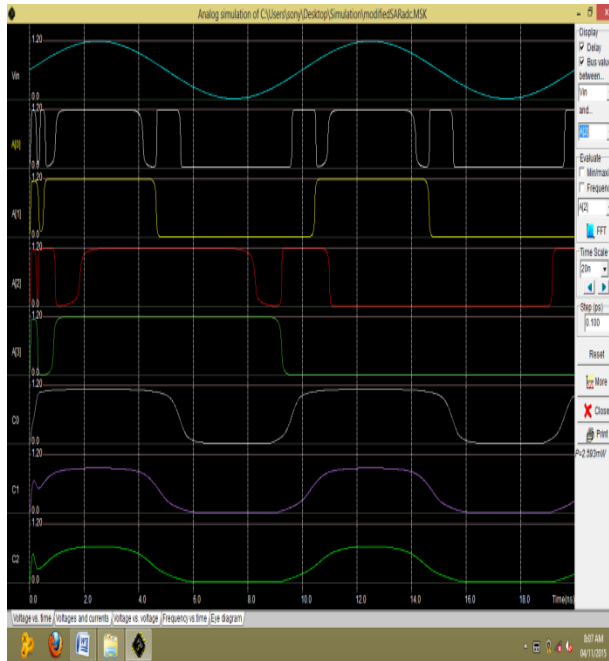


Fig.15: Simulation result for SAR ADC

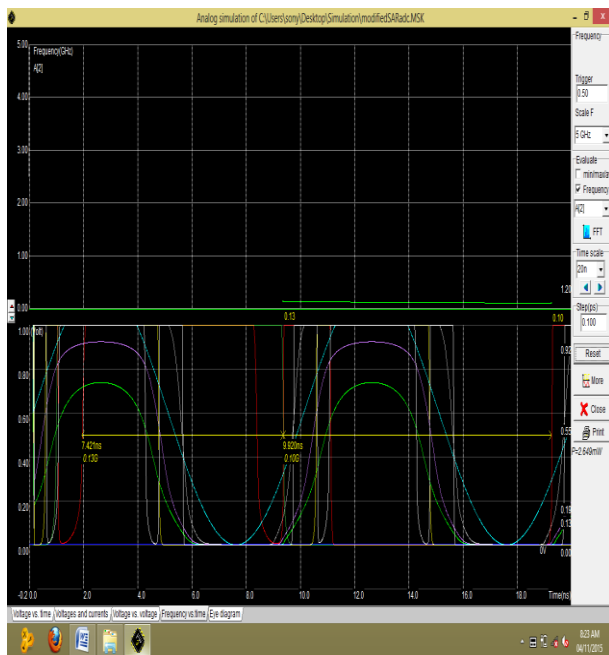


Fig.16: Simulation result for SAR ADC (Frequency &amp; Time)

Table 1. Performance Summary and Comparison

Parameters	[2]	[3]	Proposed Work
Architecture	SAR	SAR	SAR
CMOS Technology	130nm	0.18 $\mu$ m	90nm
Resolution (bits)	6	4	4
Min. Supply (V)	1.2	1.8	1.2
Power Cons.(mW)	32	23.3	2.593
Sampling Frequency	1250MHz	710MHz	2.16GHz
Area	..	..	362.46 $\mu$ m <sup>2</sup>

## V.CONCLUSION

A Successive approximation converter suitable for operating at low supply voltage is designed in a standard 90nm technology. The results indicate that the circuit achieves 4-bit conversion at medium speed with sampling frequency 2.1GHz and power consumption of 2.593 mW. Test results indicate that the circuit is well suited for operation for 1.2V.

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