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HIGH SPEED REVERSE CONVERSION PROCESS USING PARALLEL PREFIX ADDERS IN RNS SYSTEM

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Abstract— ***The implementation of residue number system reverse converters based on well-known regular and hybrid modular parallel prefix excess-one adder (HMPE) is analyzed. The VLSI implementation results show a significant delay reduction and area improvements, all this at the cost of higher power consumption, which is the main reason preventing the use of parallel-prefix adders to achieve high-speed reverse converters in recent systems. Hence, to solve the high power consumption problem, novel specific hybrid modular parallel prefix excess-one (HMPE) based adder components that provide better trade-off between delay and power consumption are herein presented to design reverse converters. We propose hybrid modular parallel prefix excess-one adder (HMPE) in Reverse Converter to increase the system performance.***

***Index Terms*— parallel-prefix adder (PPX), residue number system (RNS), hybrid modular parallel prefix excess-one adder (HMPE), reverse converter.**

I. INTRODUCTION

One of the elemental operations in electronic circuits is Binary Addition. Several fashionable circuits contain many adder units for applications like arithmetic logic unit; thus, there's a substantial interest to style less advanced and better speed and adder architectures. Within the past few decades, numerous architectures of adders are planned to optimize the delay of the adder, examples embrace, carry-look ahead, ripple carry and parallel prefix adder. The parallel prefix adder is one in all the foremost in style architectures and offers sensible compromise among power, space and speed. This sort of adder implements a logic performs to see whether or not every bit position kills the carry or propagates it or generates it. Then these generate and propagate/not kill functions are hierarchically combined to cipher the carry into every bit position forming a carry tree. The ultimate stage computes add at as position using exclusive or (XOR) gates [1].

The efficient design of Residue Number System (RNS) reverse converter based on hybrid modular parallel prefix excess-one adder (HMPE) and Chinese Remainder Theorem is used. In now a day's system, to achieve high speed reverse converter by the use of hybrid modular parallel prefix excess-one adder (HMPE) and also the hybrid modular

parallel prefix excess-one based adder components is used to solve the high power consumption problem and provide better tradeoff between power consumption and delay. The parallel prefix adder structure can implement by interconnecting excess-one unit.

II. EXISTING SYSTEM

In order to calculate the carries earlier with less delay and less complexness we have a tendency to use parallel prefix adders. Three operations are often outlined to explain standing of carry (a) Propagate: Previous carry is propagated to next bit (b) Generate: Generate a carry bit (c) Kill: Kill the previous carry.

A. STRUCTURE OF PARALLEL-PREFIX ADDER

PPA's primarily consists of 3 stages: 1. Pre computation.2 Prefix stage.3. Final computation

a. Pre computation

In pre computation stage, propagates and generates are computed for given inputs.

b. Prefix stage

In the prefix stage, group generate/propagate signals are computed at each bit using the given equations. The black cell (BC) generates the ordered pair, the gray cell (GC) generates only left signal.

$$G_{i:k} = G_{i:j} + P_{i:j}.G_{j-1:k}$$
$$P_{i:k} = P_{i:j}.P_{j-1:k}$$

More practically, the equations can be expressed using a symbol "o "denoted by Brent and Kung. Its function is exactly the same as that of a black cell i.e.

$$G_{i:k} : P_{i:k} = (G_{i:j} : P_{i:j}) 0 (G_{j-1:k} : P_{j-1:k})$$

The "o" operation can facilitate create the foundations of building prefix structures.

c. Final computation

In the final computation, the total and carryout are the ultimate outputs.

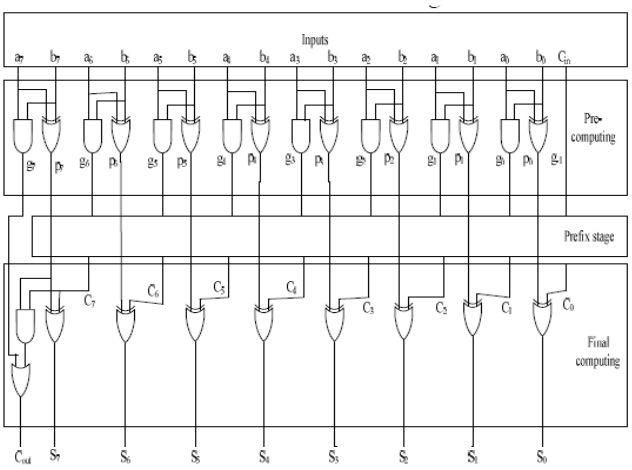

Fig.1 Parallel-Prefix Structure

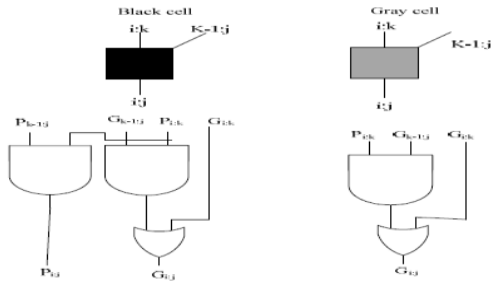

Fig.2 Black Cell and Gray Cell Configurations

$$S_i = P_i.G_{i-1:-1}$$
$$C_{out} = G_{n:-1}$$

Where "-1" is that the position of carry-input.

III. PROPOSED SYSTEM

A. REVERSE CONVERTER IN RNS SYSTEM

The forward converter, modulo arithmetic units, and reverse converter are the main parts of the RNS. In contrast to other parts, reverse converter consists of a complex and non modular structure. Therefore, more attention should be directed to its design to prevent slow operation and compromise the benefits of the RNS. Both the characteristics of the moduli set and conversion algorithm have significant effects on the reverse converter performance. Hence, distinct moduli sets have been introduced. In addition to the moduli set, hardware components selection is key to the RNS performance. For instance, parallel-prefix adders are known as unsuitable structures for complex reverse converters because of their high power consumption. However, parallel-prefix adders with its high-speed feature have been used in the RNS modular arithmetic channels [2].

Usually, one regular binary addition is required in reverse converter structures to achieve the final binary representation. This final addition has an important effect in the total delay of the converter due to the large bit-length of the operands. A thorough assessment of this final regular addition in recent converter designs shows that one of the operands has some constant bits with value 1 as highlighted by the following lemma, which applies to a class of converters [3].

Modulo Adder

Modulo addition is the easiest modulo addition operation in the residue domain because it does not require any extra overhead compared to the conventional addition. Modulo addition of any two numbers and , each of bits, is done by adding the two numbers using a conventional adder. The result is an bit output, where the most significant bit is the carryout. The residue is the first lowest significant bits, and the final carry-out is neglected. Therefore, modulo addition is the most efficient modulo addition operation in the residue domain. The main reason for the high power consumption and area overhead of these adders is the recursive effect of generating and propagating signals at each prefix level. An optimized approach is proposed in, which uses an extra prefix level to add the output carry. However, this method suffers from high fan-out, which can make it usable only for small width operands. However, we could address this problem by eliminating the additional prefix level and using a modified excess-one unit instead. In contrast to the BEC, this modified unit is able to perform a conditional increment based on control signals as shown in below Fig and the resulted hybrid modular parallel-prefix Fig. 3 Modified excess-one unit. Fig. 4 HMPE structure. excess-one (HMPE) adder is depicted in Fig. 4.

The HMPE consists of two parts
1) A regular prefix adder
2) A modified excess one unit

First, two operands are added using the prefix adder, and the result is conditionally incremented afterward based on control signals generated by the prefix section so as to assure the single zero representation. Summarizing, the HMPE is highly flexible, since it can be used with every prefix networks. Hence, the circuit performance metrics such as area, delay, and power-consumption can be adjusted by selecting the desired prefix structure. On the other hand, the HRPX avoids the usage of a large size parallel-prefix adder with high power consumption, and also does not have the penalty of using the long carry-propagation chain of a RCA.

B. REVERSE CONVERSION FROM RNS TO BINARY REPRESENTATION

Reverse conversion algorithms in the literature are all based on either Chinese Remainder Theorem (CRT) or Mixed-Radix Conversion (MRC). The MRC is an inherently sequential approach. On the other hand, the CRT can be implemented in parallel. The main drawback of the CRT based R/B reverse converter, is the need of a large modulo adder in the last stage. All the converters proposed in the literature have this problem. The reverse conversion is one of the most difficult RNS operations and has been a major, if not the major, limiting factor to a wider use of RNS. In general, the realization of a VLSI implementation of R/B converters is still complex and costly. Here, we derive the mathematical foundations of the CRT and the MRC, and then we present possible implementations of these methods in reverse conversion [5].

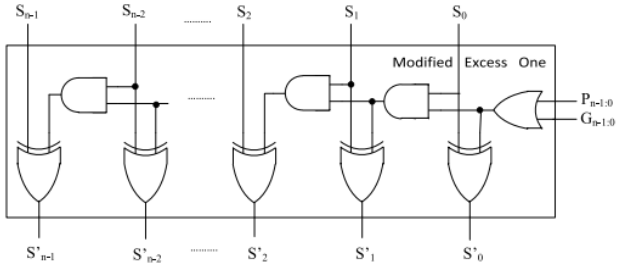

Fig. 3 Modified excess-one unit

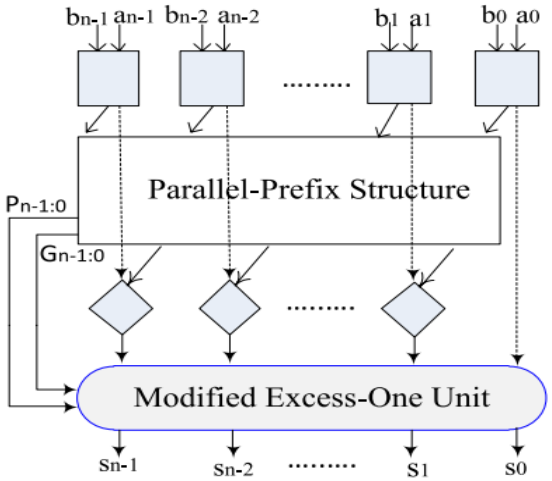

Fig. 4 HMPE structure

C. METHODOLOGY OF REVERSE CONVERTION

In proposed methodology of reverse converter design is described. In the following, a method employing distinct components in the architecture of the reverse converter will be presented. Several reverse converters for different moduli sets have been introduced, which can be classified into three classes. The first class consists of converters with a tree of CSAs with EAC followed by a two-operand modulo 2k-1 CPA. A second class includes more complex reverse converters, which have several CSAs and CPAs with EACs followed by a final regular subtractor with two operands of different size. The implementation of this subtractor using regular binary-adder results in one operand with some constant bits. The third class covers the reverse converters that have been designed for moduli sets with moduli other than the popular 2n and 2n ± 1.

Here we describe a methodology for designing reverse converters in the first and second classes. The suggested method for applying the HMPE and HRPX in the reverse converter is shown in Fig. 4. First of all, it is relevant to decide about the required performance metrics based on the specified application. If it is just important to achieve the least power consumption and hardware cost without considering speed, no prefix adder is needed.

On the other hand, if high speed is the designer goal, the CPAs with EAC and the regular CPAs should be replaced by traditional parallel prefix modulo 2n − 1 adders and regular parallel-prefix adders, respectively. However, for the VLSI designers, a suitable tradeoff between speed, power, and area is often more important. In this case, first, CPAs with the EAC can be replaced by the HMPEs. Then, if the converter contains a regular CPA where one of its operands has a string of constant bits with the value of one, it can be replaced with the HRPX [4].

IV. RESULTS

MODELSIM OUTPUT:

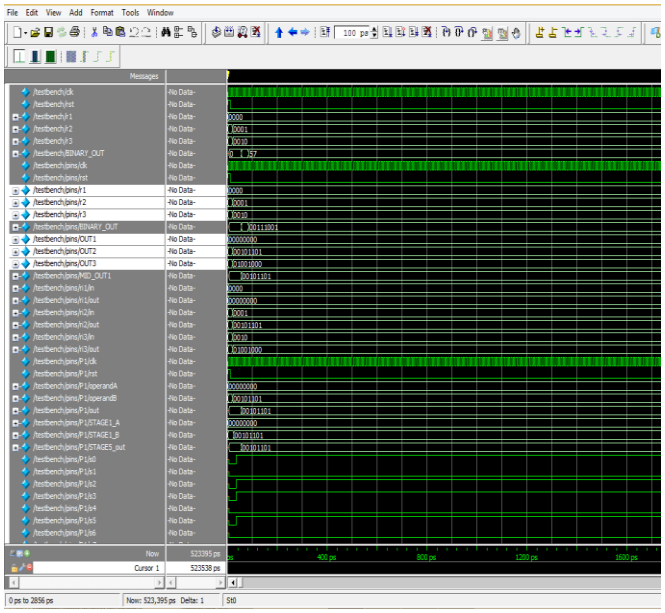

Fig.5 Reverse converter Simulated output

AREA UTILIZATION REPORT:

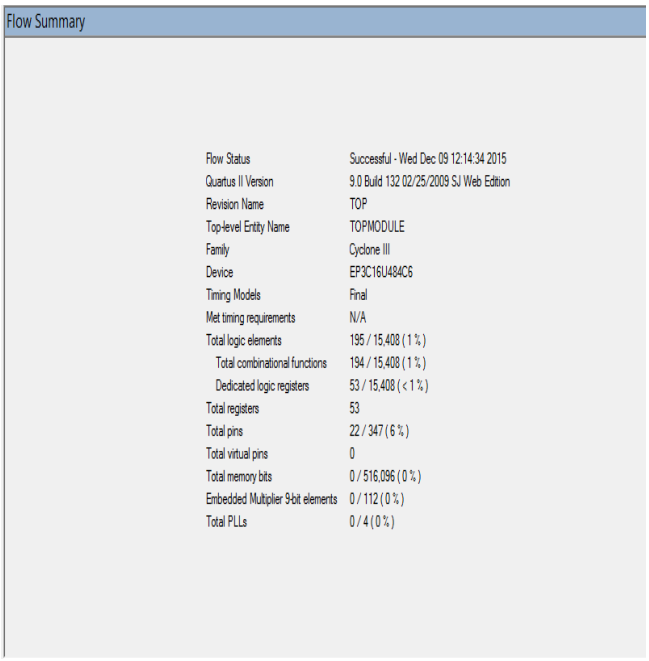

Fig.6 Flow summary report

PERFORMANCE REPORT:

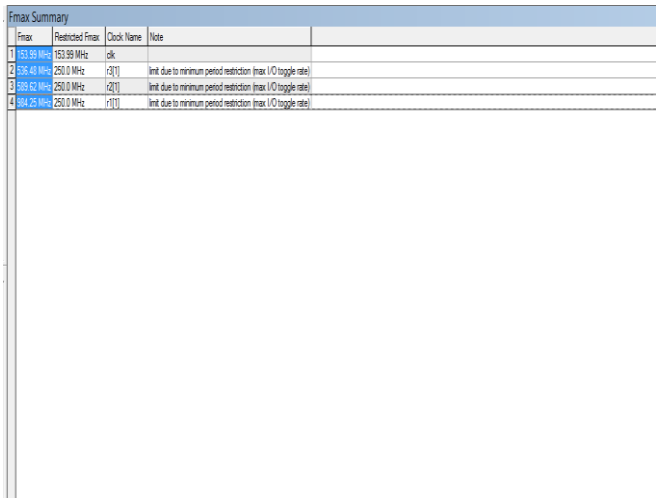

Fig.7 F_{max} summary report for slow corner

SYNTHESIS REPORT:

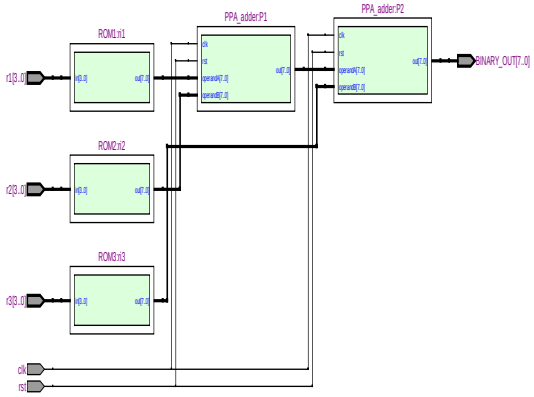

Fig.8 RTL Schematic report

POWER REPORT:

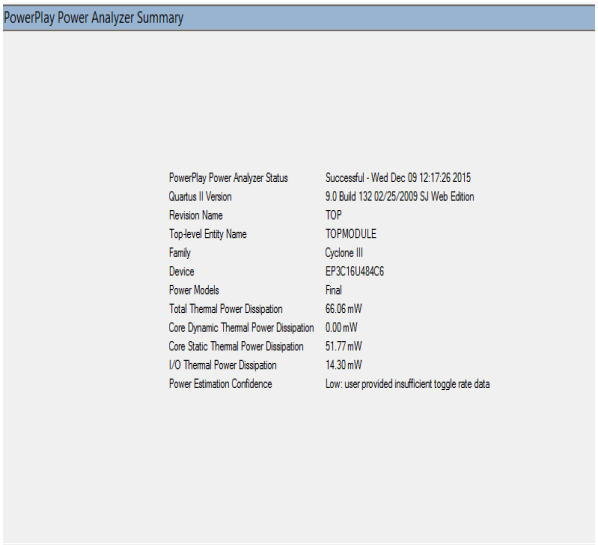

Fig.9 power dissipation report

TABLE I Trade off analyzes of adders with QUARTUS II hardware synthesis using CYCLONE III family (EP3C16U484C6)

ADDER type	AREA	SPEED
CLA	133	265.25 MHz
CSA	81	236.35 MHz
RCA	79	176.15 MHz
PPA	79	372.02 MHz

CONCLUSION AND FUTURE WORK

In this paper we proved the efficiency of hybrid modular parallel prefix excess-one adder (HMPE) in reverse conversion method and it is verified through modelsim based exhaustive simulation to propose it for high-speed application. Verification of design network with pre-computed residues which allows to compared to the previous approaches. An extensive synthesis report of QUARTUS II and cyclone III implementation results shows that proposed adders outperforms previously developed traditional, non-parallel adders. Our reverse converter shows improvements with the highest speed, low power and area.

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