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Design and Analysis of Modified Doherty Power Amplifier for High Data Rate Applications

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Abstract— **In today's generation ,the wireless communication system is developing rapidly, due to which new standards like WIMAX and 4G Long Term Evaluating(LTE) with a purpose of achieving high data rate result in high end applications such as high speed internet, video conferences and broadband width. These applications require mobile base stations at the transmitter as well as at receiver (T/R) to support features like multiple bands, multiple modes, higher BW and less power consumption. The design and implementation of multi-standard transceivers for wireless mobile system is very complex task. In this paper we discuss the design of a wider band Doherty Amplifier, which operational frequency of 3 GHz to 3.75 GHz. The development of proposed DPA is based on techniques of inserting wider band compensators along with second and third harmonic tuning at the output of the GaN HEMT main and peak amplifier. In this work ,the basic constraints in the basic DPA is λ/4 transformer has been eliminated with the help of Branch Line Coupler(BLC). The designed amplifier gives the drain efficiency 70% - 75% at about 46-43 dBm output power and gain around 12 dB in the desired band.**

Index Terms -**Doherty Power Amplifier (DPA),GaN field effect transistors(FET),Wider-Band BLC, Compensators**.

I. Introduction

Today's wireless communications demands to increase the transmitted data per hertz in order to utilize the spectrum effectively. In order to increase the data per hertz, a signal with high Peak to Average Power Ratio(PAPR) is required .In reality, RF power amplifier with high PAPR will reduce the backup efficiency. So far, two techniques have been developed to increase the efficiency, they are Envelope elimination and restoration (ERR) and Doherty Power Amplifier(DPA).Among these two DPA has been accepted for adaptation since it is easy to implement.

Due to high back efficiency the DPA has been widely used in base stations. BATICHI[9] and QUARESHI[8] work reveals that the DPA suffers the disadvantage that the bandwidth limitations due to quarter wave impedance transformer in the output capacitance of the transistor .Therefore the DPA works in single band (narrowband) and they do not satisfy the multi standard and multiband to suit the requirement of modern wireless communications. On the other hand, the efforts have been made to design a new techniques to increase the Bandwidth of DPA[22-24].This efforts are not successful as expected due to wide operation is not constant over a band ,but some of the good efforts has been done in [8] ,a 20% fractional bandwidth extension achieved by modifying conventional DPA by driver module to properly and separately feed the main and peak stages. By exploiting wideband filters, a 35% fractional bandwidth has been increased in[9] in this work a standard topology has been adopted but Doherty behavior is not clearly demonstrated and the power utilization factor is not constant in the desired band. In[10],by using frequency reconfigurable matching network with additional external controls, which enables 20% fractional bandwidth .Focus on output combining stages has been done in order to increase the wider-band has been shown by broadband matching real frequency technique in[12]. The work in[13] focuses on input direct coupling of main and peak branches and wide-band ,output matching to improve the wideband. Finally, GaN HEMT Doherty amplifier has been designed based on a simple technique based on wide-band compensators inserted at the output of peak and main amplifiers in [21].

In this paper the proposed wideband PA designed for 3.1 -3.75GHz frequency range. Adapting simple techniques based on wide-band components at the output of main and peak amplifier along with second harmonic tuning has been implemented at the upper bandwidth to help gain equalization versus desired frequency. The basic feature has been adapted in this design by eliminating IIN and ITN with the help of the wideband BLC and also eliminating phase shifter at the input of the peak amplifier

The following table shows the comparison of different wideband Doherty PA designed so far

Reference	Frequency[GHz]	Output power[Watts]
[8]	1.72-2.0 GHz	20 W
[9]	1,5-2.1 GHz	20W
[11]	1.6-2.75GHz	20W
[12]	2.1-2.9 GHz	13W
[21]	3-3.6GHz	20W
This work	3.1-3.75 GHz	37W

This paper organizes the section II deals with the design of proposed DPA and Section III presents and discusses the carried out simulation results and final section draws the conclusions

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II. DESIGN STRATEGY

A. The block diagram of the proposed DPA is as follows in fig (a)

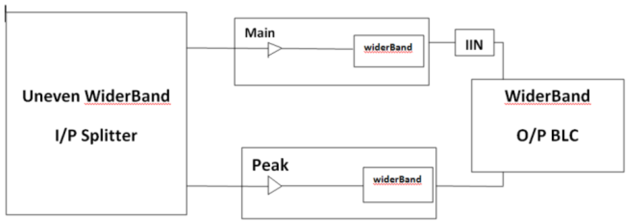

Fig (a)

B. The following design strategies are used to improve the bandwidth in the proposed DPA

- Load modulation for required bandwidth
- Tuning at the output of amplifiers for improving gain
- Implementation of Impedance Inverter Network[IIN] and Impedance Transformer Network[ITN] with the help of wide band BLC

-Load Modulation for required bandwidth: The conventional DPA is well suited for narrowband amplifier, due to the presence of λ/4[Quarter-Wavelength] as a impedance transformer and output capacitance of the transistor.

The reactance of output capacitances of transistor has been reduced by inserting designed circuit, such that it will reduce the output reactance of the gain HEMT transistor for the given bandwidth. This has been clearly demonstrated in [21] such circuits are called wide-band compensators, which are designed such that reflection co-efficient of at the input **transistor is equal to the reflection co-efficient of at the output** of wide-band compensators on the whole-band

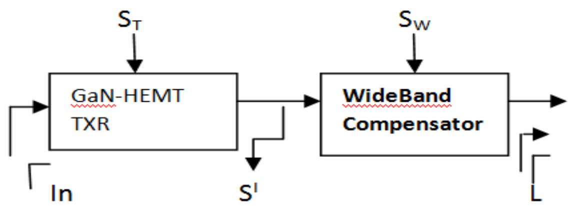

Fig b

By transmission line theory , in order to get ⌈in = ⌈L ,the following equations are satisfied

$$S^1 = \begin{vmatrix} 0 & \pm 1 \\ \pm 1 & 0 \end{vmatrix} \quad \text{.........eq(1)}$$

$$\Gamma_{IN} = \frac{S^1_{11} + S^1_{21} S^1_{12} \Gamma_L}{1 - S^1_{22} \Gamma_L} \Rightarrow \Gamma_{IN} = \Gamma_L \quad \text{...eq(2)}$$

$$S^1_{11} = S^1_{22} = 0 \text{............eq(3)}$$

$$|S^1 21| = |S12| = L \text{.....eq(4)}$$

-Tuning at the output of amplifiers for improving gain: The characteristics of the basic DPA is high gain at one frequency (narrow band). At this work the basic objective is to increase the bandwidth in the range of 3.1GHz to 3.75GHz. Equally we need to increase the power gain over the designed bandwidth. To achieve this requirement the tuning frequency has been set around 3.45GHz and optimizing the length of the output offset lines of the main and peak amplifiers in such a way that the second and third harmonic will be tuned to the fundamental and hence this can be interpreted as tuning for second and third harmonic at the output of peak and main amplifier. Due to which the main amplifier behaves as a tune load stage at the lower portion of the band and gradually becomes second harmonic are obtained through the gate and drain bias network . Which can be achieved by using quarter wave which behaves as open circuit at fundamentals. In generally, we can observe the load impedance is larger at high frequency consisting with second harmonic tuning

-Impedance Inverter: The Conventional DPA operating principle is based on the idea to modulate the output load of a main active device by using the current generated by an auxiliary active device , which is termed as active load modulation. To realize, a λ/4 transformer has been inserted between the main device and the load. The quarter wave transmission line (λ/4) is called Impedance Inverter Network ,since it transform the load of main device from higher to lower due to the current generated by auxiliary and along with Impedance Transformer Network[ITN].

At this work, the Impedance Inverter Network[ITN] has been implemented in such a way that the output (current) from main and peak device together we have 90^0 phase shift, which can be achieved by optimizing the offset lines after wide-band compensators and it will fed to the ports of output BLC.

Therefore, load modulation can be achieved with the help of output BLC.

-ITN and Output: The Impedance Transformer Network[ITN] is used in the conventional DPA to standard output termination, usually 50Ω.This will be implemented through λ/4 transmission line along with output resistance $R_{L.}$ At this work , the ITN function will be implemented in the output BLC and also which has been optimized such that it will give required bandwidth.

-Input Splitter: The wider-band branch line coupler are used as input splitter to split unequal power division with equal impedance. The unequal power division is required to feed more current to operate auxiliary amplifier. It automatically allows the phase between the two amplifier paths by 90^0 i.e driving condition to ensure that I_M lags I_A by 90^0,which is basic requirement in conventional DPA ,due to which phase compensator has been incorporated in conventional DPA..Therefore, phase compensators has been avoided in this work . Finally it was optimized to allow the required band.

III. EXPERIMENTAL RESULTS OF REALIZED PROPOSED DPA

The active device i.e., amplifier used in the realized DPA is commercial packages CGH40025F packed GaN HEMT form CREE Inc., with a 25W output power at 28V drain biass. The DPA is characterized in DC,large signal model from 3.1 to 3.75 GHz with 50 MHz steps The schematic diagram of proposed DPA is shown in Fig (c).

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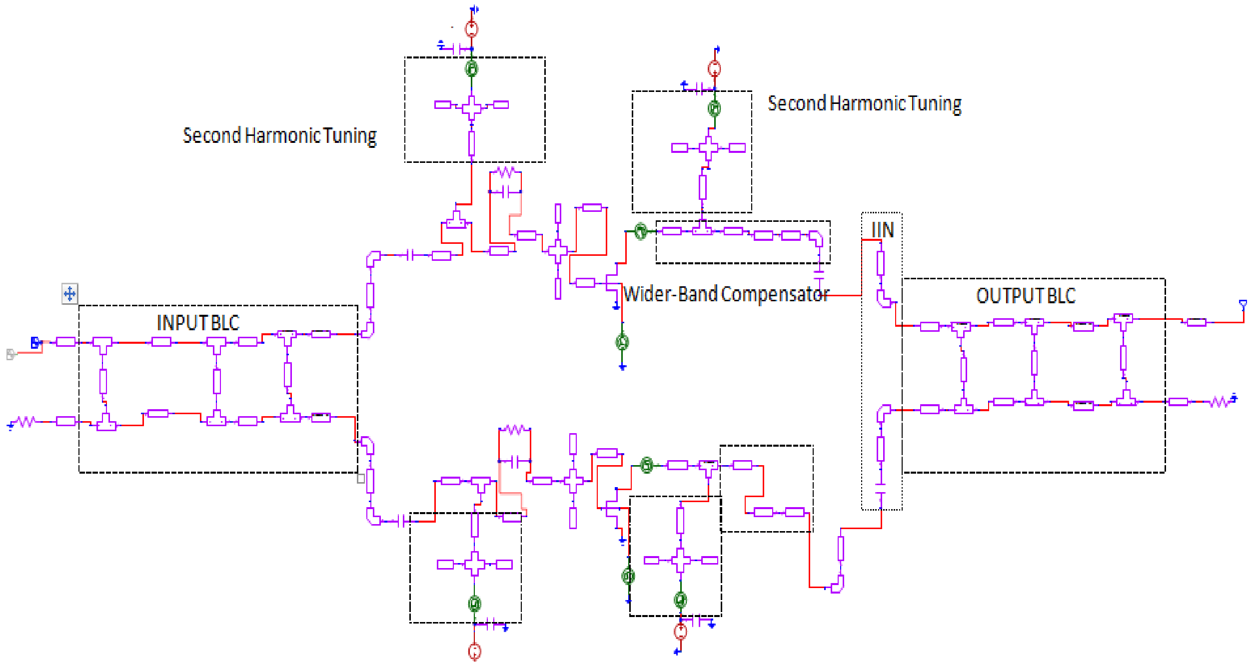

Fig. (c)-Complete Schematic Diagram of the Proposed DPA

The fig(d) shows the simulated result of S11 and S(2,2) and s(2,1) in the desired band at V_{DS}=28V and Vgs=-2.88V($I_{DS=}$238 milliamp) for the main and V_{DS} =28V and Vgs =-10V for the peak amplifier. The return loss of the proposed DPA exhibit a good magnitude, which has been achieved due to electromagnetic simulation exploited for the most critical microstrip structures example junction between strips very different width

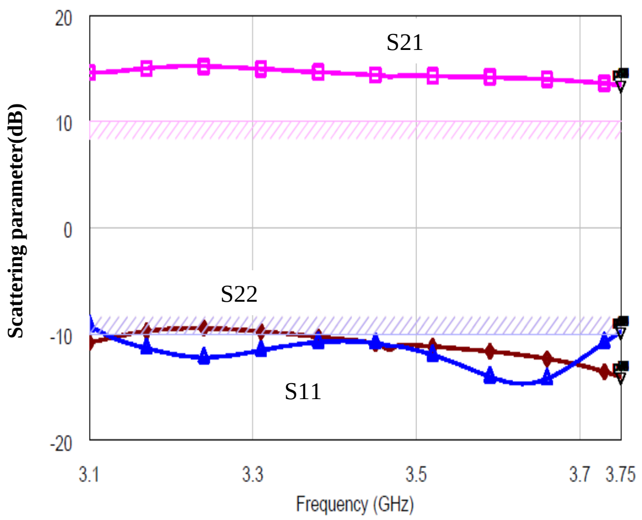

Fig (d)-Return Loss of DPA in the band 3.1 -3.75GHz

The drain efficiency of the DPA as a function of output power is as shown in fig(e) for the 3.1,3.45 and 3.75GHz excitations.From this graph we can observe the typical Doherty high efficiency region from maximum output power exceeding from 44 dBm to 6 dB back off at all simulator frequency.

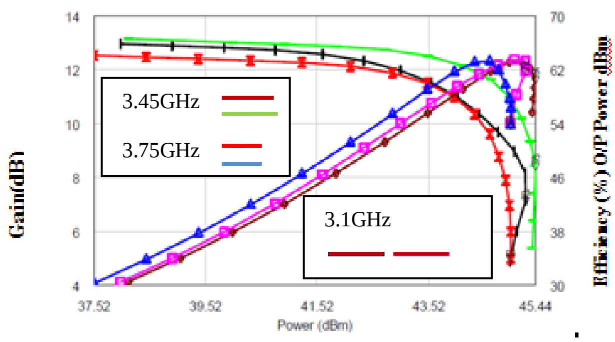

Fig (e)-Single tone characterization at 3.1,3.45 and 3.75 GHz

From the fig(f) and fig(g) ,the maximum output power together with efficiency and gain respectively ,both at maximum output power and at 6 dB back-off vs the excitation frequency.The maximum output power higher than the 46 dBm over the wholeband power corresponding to the maximum power utilization factor of the devices and the gain at 6 dB back-off power will equalize around 13 dB. Regarding the efficiency it has found to be between 70% to 75% at saturation, at 6dB back-off,it is between 60%-65%

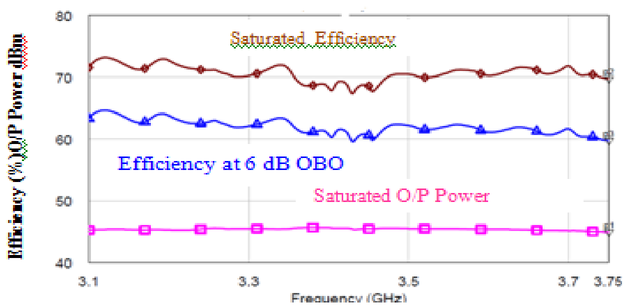

Fig f-DPA characterized varying excitation frequency. Efficiency at 6 dB DBO and in saturations and saturation output power vs input power

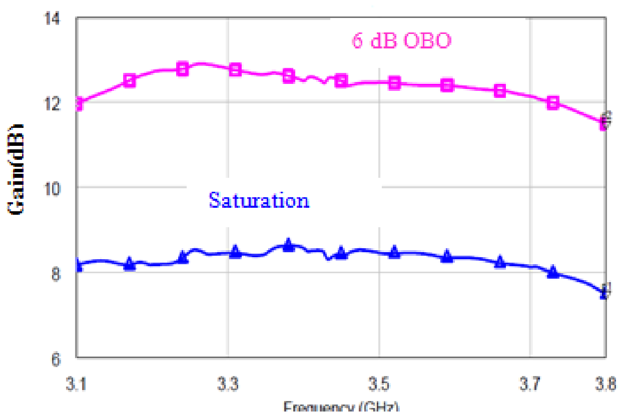

Fig g-Power Gain at 6 dB OBO and in saturation power

The simulated results exhibit a small signal gain higher than 13 dB which is as shown in the fig(g)

IV. CONCLUSION

The wideband GaN-HEMT Doherty amplifier has been designed for the frequency 3.1-3.75 GHz which is designed using wider-band BLC at the input and output along with wide-band matching with wide-band compensators. Second-harmonic to improve efficiency and to achieve gain equalization over frequency. An output power exceeding 46dBm with saturated efficiency over 70% and over 60% at 6 dB back- off..The results of the designed DPA compares the DPA's specified in the literature.

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