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# Design of transmission gate base on low power & area- efficient 16-bit carry selected adder using Xilinx

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***Abstract*—This paper proposes on the logic operations in conventional carry select adder (CSLA). Arithmetic operations are heart of computational units and data path logic system. High performance power efficient adder occupying less chip area necessary in battery powered portable devices. In this work modification and compare in CSLA terms of delay, area, power and power delay in using three techniques RCA ( ripple carry adder) , BEC(binary to excess-1 converter), CSA( carry save adder). Result analysis show that the proposed modified design in 16 bit adder.**

***Index Terms*—Adder, BEC, RCA, Arithmetic unit, Area-Delay design**

## I. INTRODUCTION

Whenever we draw a block diagram or circuit diagram we define an input or output. However fast hardware is the gates or other things we've within the circuit there would have been a finite delay in the transmission of a signals this time is defined as propagation delay, needless to say is dependent upon the size of the signal path when the gates start switches transmission starts. When we should design the fast circuit or fast system naturally we've to go for some solutions. By reducing the road of the transmission. if were reduce the road so that individuals can reduce the delay and can increase the operation of the circuit. For the given technology we should maximize the speed then we should choose this kind of scheme by cutting the short length. In the full adder circuit carry has traveling from state to state. Previous states carry need to require for today's state to accomplish the operation. So, naturally when we increase how many bits the propagation delay and the delay of every stage increases. Now when we don't have to be determined by the transmission of the carry we can predict the carry of every stage. Now per day our computers speed is fast high in terms of GHz. So conceptually we have to enhance the speed for the give design by decreasing several number of stage or gates. SSB Carry Select Adder (CSLA) has a more balanced delay, and requires lower power and area [1], [6], [10]. The fundamental idea of the work is to utilize Binary to Excess-1 Converter (BEC) rather than RCA with in the regular CSLA to reach lower area and power consumption [1],[2],[7],[8]. Though the CSLA need more area as a result of using multiples of ripple carry adder for generating sum and continue the dependency of carry input cin=0 and cin =1[7]. Then the ultimate consequence of sum and carry are selected by the multiplexers from bit to bit likely to increase. Finally reliable results at the output will depend upon how many stages.

### 1.1 **BEC** Binary to excess-1 converter

As stated above the main idea of this work is to use BEC instead of the RCA with C = 1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, An n+1 bit BEC is required. A structure of a 4-bit BEC is shown in Fig. 1.

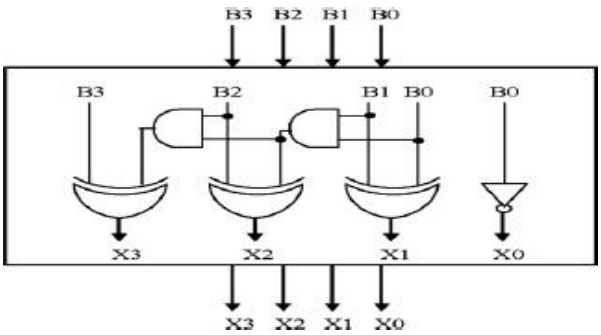


Fig.1 basic block diagram BEC 16-bit adder

The significance of the BEC logic stems from the large silicon area reduction once the CSLA with large quantity of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols NOT, & AND, XOR)

$$X0 = \sim B0$$

$$X1 = B0 \wedge B1$$

$$X2 = B2 \wedge (B0 \,\&\, B1)$$

$$X3 = B3 \wedge (B0 \,\&\, B1 \,\&\, B2)$$

### 1.2 **RCA** Ripple Carry Adder:

Generally in most computers, the augmented operand is replaced by the sum, whereas the addend is unchanged. High speed adders are not just for addition but additionally for subtraction, multiplication and division. The speed of an electronic processor the sum, whereas the addend is unchanged. High speed adders are not just for addition but additionally for subtraction, multiplication and division. The speed of an electronic processor depends heavily on the speed of adders. The adders add vectors of bits and the principal problem is always to speed- up the carry signal.

A conventional and non optimized 16-bit adder may be created by the usage of the generic one-bit adder. Cell

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connected someone to the other (figure 2). It is named RCA. In this case, the sum resulting at each stage need to attend for the incoming carry signal to perform the sum operation. The carry propagation may be speed-up in two ways. The very first ñ and most obvious way is to employ a faster logic circuit technology. The 2nd way is always to generate carries in the shape of forecasting logic that doesn't depend on the carry.

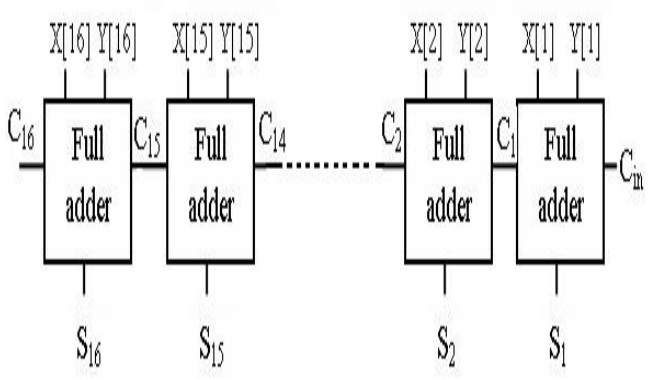


Fig.2 16-bit full adder RCA

## II. DELAY EVALUATION METHODOLOGY OF MODIFIED 16-bit BEC CSLA

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We adding up the number of gates in the longest path of a logic block that plays a role in the maximum delay. The region evaluation is completed by counting the total quantity of AOI gates required for each logic block. Centered on this method, Half Adder and full adder are evaluated and listed in Table I. As mentioned above the main idea with this work is by using BEC rather than the RCA with Cin=1 to be able to reduce the area and power consumption of the regular CSLA. To restore the n-bit RCA, an n+1 bit BEC is required.[4] Show in fig.3

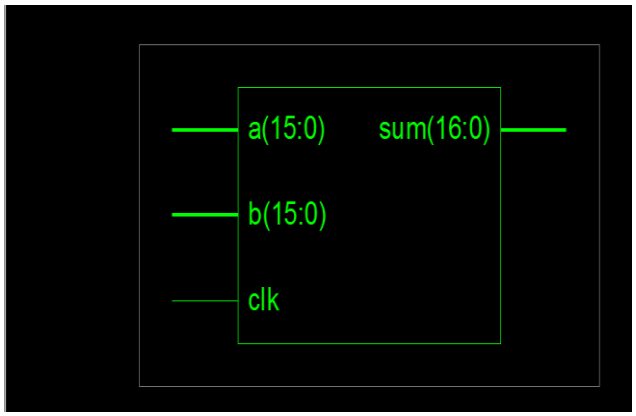


Fig.3 BEC 16-bit

```
HDL Synthesis Report

Macro Statistics
# Latches                                          : 18
 1-bit latch                                       : 18
# Xors                                             : 30
 1-bit xor2                                        : 19
 1-bit xor3                                        : 11

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=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================

Loading device for application Rf_Device from file '3s500e.nph' in environment C:\Xilinx92i.

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Latches                                          : 18
 1-bit latch                                       : 18
# Xors                                             : 30
 1-bit xor2                                        : 19
 1-bit xor3                                        : 11

=========================================================================
```

TABLE-1

## II. DELAY EVALUATION METHODOLOGY OF MODIFIED 16-bit RCA CSLA

Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction). Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs a **Cin**, which is the **Cout** of the previous adder. This kind of adder is a **Ripple Carry Adder**, since each carry bit "ripples" to the next full adder. The first (and only the first) full adder may be replaced by a half adder.[5]The block diagram of 16-bit Ripple Carry Adder is shown table-2 how many gates are use and basic diagram show fig.4,fig.5& table-2 blow here below –

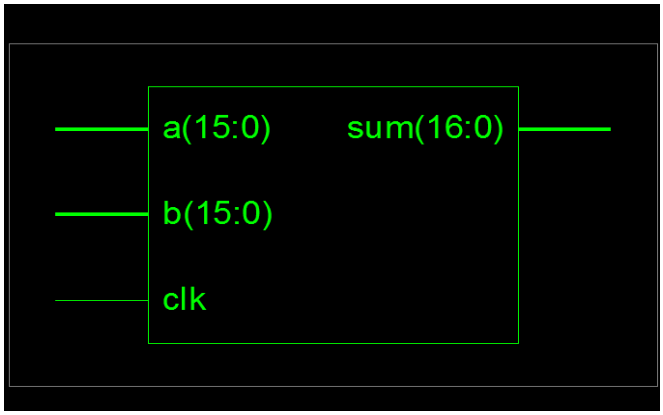


Fig.4 RCA16-bit adder

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a) BEC Adder

```
HDL Synthesis Report

Macro Statistics
# Latches                                : 23
 1-bit latch                            : 23
# Xors                                   : 36
 1-bit xor2                             : 35
 1-bit xor3                             : 1

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================

Loading device for application Rf_Device from file '3s500e.nph' in environment C:\Xilinx92i.

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Latches                                : 23
 1-bit latch                            : 23
# Xors                                   : 36
 1-bit xor2                             : 35
 1-bit xor3                             : 1

=========================================================================
```

TABLE-2

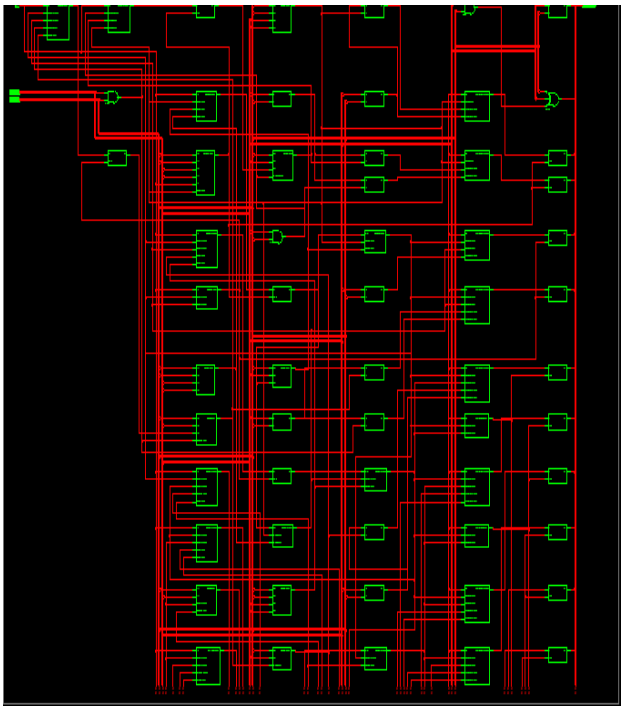

Fig.5 internal structure BEC-16 bit adder

## III. Result Analysis

The simulation results are carried out for Area-delay-power carry select adder to find out the area-delay. The simulation is carried out by Modelsim 6.4c as a simulator tool. The simulation result is shown as snapshots.fig.6 and table 3

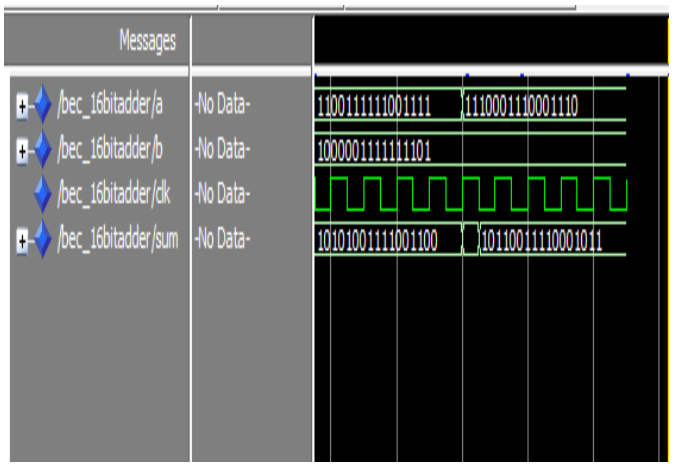


Fig.6 Modelsim results BEC 16bit adder

```
Data Path: sum_3 to sum<3>
                                   Gate     Net
   Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
   ----------------------------------------  ------------
    LD:G->Q               1   0.676   0.420  sum_3 (sum_3)
    OBUF:I->O                 3.272          sum_3_OBUF (sum<3>)
   ----------------------------------------
   Total                      4.368ns (3.948ns logic, 0.420ns route)
                              (90.4% logic, 9.6% route)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 6 / 2
-------------------------------------------------------------------------
Delay:               6.320ns (Levels of Logic = 3)
  Source:            a<0> (PAD)
  Destination:       sum<1> (PAD)

  Data Path: a<0> to sum<1>
                                   Gate     Net
   Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
   ----------------------------------------  ------------
    IBUF:I->O             3   1.218   0.706  a_0_IBUF (a_0_IBUF)
    LUT4:I0->O            1   0.704   0.420  Mxor_sum<1>_xo<1>1 (sum_1_OBUF)
    OBUF:I->O                 3.272          sum_1_OBUF (sum<1>)
   ----------------------------------------
   Total                      6.320ns (5.194ns logic, 1.126ns route)
                              (82.2% logic, 17.8% route)
```

Table-3 area delay BEC16bit adder

b) RCA adder

The simulation results are carried out for Area-delay-power carry select adder to find out the area-delay. The simulation is carried out by Modelsim 6.4c as a simulator tool. The simulation result is shown fig.7 and table-4 as snapshots.

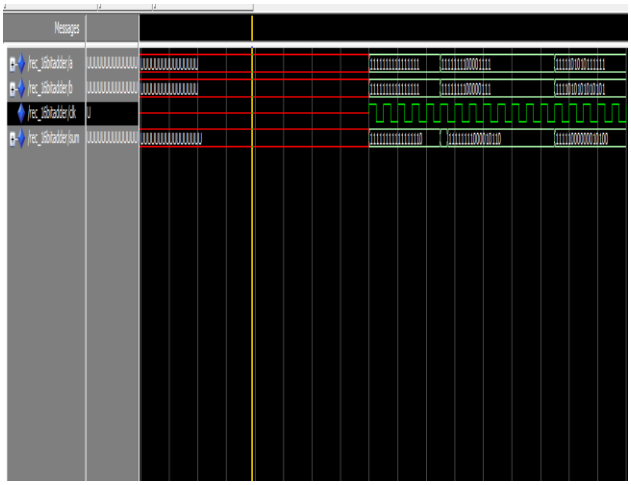

Fig.7 modlesim RCA16 bit result

```
================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 6 / 2
--------------------------------------------------------------------------------
Delay:               6.320ns (Levels of Logic = 3)
  Source:            a<0> (PAD)
  Destination:       sum<1> (PAD)

  Data Path: a<0> to sum<1>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   1.218   0.706  a_0_IBUF (a_0_IBUF)
     LUT4:I0->O            1   0.704   0.420  Mxor_sum<1>_xo<1>1 (sum_1_OBUF)
     OBUF:I->O                 3.272          sum_1_OBUF (sum<1>)
    ----------------------------------------
    Total                      6.320ns (5.194ns logic, 1.126ns route)
                                       (82.2% logic, 17.8% route)

================================================================================
CPU : 28.88 / 29.44 s | Elapsed : 29.00 / 30.00 s
```

Table-4area-delay 16 bit adder

## V. CONCLUSION

The logic operations active in the conventional and BEC-based CSLAs to study the info dependence and to identify redundant logic operations. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. As a result of small carry output delay, the proposed CSLA design is a great candidate for the SQRT adder. The RCA synthesis result suggests that the present BEC-based SQRT-CSLA design involves more Area Delay Product and consumes energy than the proposed SQRT CSLA. RCA better then BEC adder.

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