ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 5, Issue 1, January 2016

A Power Efficient 2:1 Multiplexer Designfor Low Power VLSI Applications

[1]SaumyaPandey
Student, Dept. of Electronics and Communication Engineering, IGDTUW, Kashmere Gate, Delhi-110006, India

[2]Dr. Nidhi Goel
Associate Professor, Dept. of Electronics and Communication Engineering, IGDTUW, Kashmere Gate, Delhi-110006, India

ABSTRACT

Today power dissipation has become the main design concern in VLSI circuits. As the technology advances, the number of transistors integrated on a single chip continuously increases and the switching speed of the transistors also increases.Forhigh performance systems very expensive packaging and cooling techniques are required because of more heat dissipation and it also degrades the system reliability. In this paper, a new technique based on adiabatic logic will be presented for reducing power dissipation that shows an increasing growth as the technology is scaled down.Using adiabatic technique, power dissipation minimization can be achieved as well as the energy stored on the load capacitance can be reutilized instead of dissipated as heat.In this paper, we have proposed a 2:1 multiplexer using ECRL, PFAL & DFAL adiabatic logic design techniques and then compared with the conventional CMOS multiplexer. A multiplexer is an integral part of the any digital circuit and is used in variety of applications e.g. in Full Adders, Shift registers, Arithmetic Logic Unit(ALU),Digital Compressor etc. Tanner 14.1 EDA tool is used for the simulation & verification of the circuit with 90nm CMOS Technology.

Keywords

Adiabatic, ECRL, PFAL, DFAL, T-SPICE,Fully Adiabatic, Partially Adiabatic Circuit (Quasi), Multiplexer.

1. INTRODUCTION

Due to growing market of portable electronic devices such as personal digital assistants, laptops,cellphones etc., low power consumption has now become a major concern in integrated circuit design. Due to the limited power of the batteries, the circuitry involved in such devices must be designed to consume less power.Among many design techniques, adiabatic approach is one method of reducing power dissipation in logic circuits. Conventional CMOS based circuit designs consume a lot of energy during the charging and discharging of the node capacitances of the circuits[1]. Such part of the total power dissipated by a circuit is called dynamic power. Dynamic power dissipation can be reduced by using an alternative approach to the traditional techniques of power consumption reduction called adiabatic switching.

Adiabatic switching technique reduces the energy dissipated through PMOS during charging phase and reuses some of the energy stored on the load capacitor during the discharging phase.[4]

2. ADIABATIC LOGIC

The term “adiabatic” describes a thermodynamic process in which there is no exchange of energy with the environment, and hence no dissipation of energy or power occurs. It works on the principal of reversible logics. The power clock is used both as a power supply & as a clock signal.
The power-clock voltage is dynamically adjusted according to constant-current charging results in adiabatic-charging effect[2].The load capacitor is charged adiabatically by power supply clock during the time it ramps up and allows the energy stored on load capacitor to recycle back when ramps down.

The two key rules by which adiabatic circuits try to conserve the energy are:
1. Never turn on a transistor when voltage difference existsbetween source and drain.
2. Never turn off a transistor that has current flowing through it.[4]

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 5, Issue 1, January 2016

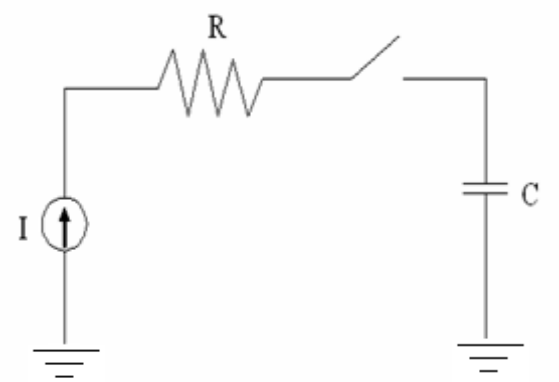

Figure.1: Circuit explaining Adiabatic Switching

Fig. 1 shows the RC model for the adiabatic circuit where the load capacitance C is charged by a time dependent current source I(t) instead of the constant-voltage source as in the conventional CMOS circuits.

Voltage across the Capacitor $V_C(t) = 1/C.I(t).t$
The average current from 0 to t, $I(t) = C. V_C(t)/t$

Total energy dissipation in resistor R from 0 to t= T is given by

$$E = E_{diss} = R\int_0^T I^2 dt = \frac{2RC}{T}\left(\frac{1}{2}CV^2\right)$$

where,
E — Energy dissipated during charging,
C —Load capacitance,
R — Resistance of the MOS switch turned on,
V — Final value of the voltage at the load,
T — Charging time.

From the above equation of energy dissipation, following conclusions can be made:
1. For T >2RC, the dissipated energy is quite small as compare to the conventional CMOS.
2. Energy dissipation can be made arbitrarily small by further increasing the charging time.
3. The dissipated energy is proportional to R. Thus, reducing the on-resistance of the PMOS network results in lower dissipation.[4]

3. ADIABATIC LOGIC FAMILY

The two fundamental classes in which adiabatic circuits can be categorized are:

1. Fully Adiabatic Circuit
2. Partially energy recovery Adiabatic Circuit.

In fully adiabatic circuits, all the charges stored on the load capacitance is recovered by the power supply whereas in partially adiabatic logic some amount of charges is transferred to the ground.

Partial adiabatic methods are:

- Efficient Charge Recovery Logic (ECRL)
- Positive Feedback Adiabatic Logic (PFAL)
- 2N-2N2P Adiabatic Logic
- NMOS Energy Recovery Logic (NERL)
- Source-coupled Adiabatic Logic (SCAL)

Full adiabatic methods are:

- Pass Transistor Adiabatic Logic (PAL)
- Split-Rail Charge Recovery Logic (SCRL).[3]

3.1 EFFICIENT CHARGE RECOVERY LOGIC(ECRL)

ECRL has two cross coupled PMOS and two NMOS tree structure. An AC power supplyis used to recover the charge & reuse the supplied energy.[4] Both Out and $\overline{Out}$is generated so that power clock generator always drive a load capacitance which is independent of the input signal. The logic function which is to be implemented is realized using NMOS transistors, in both true and complementary forms.

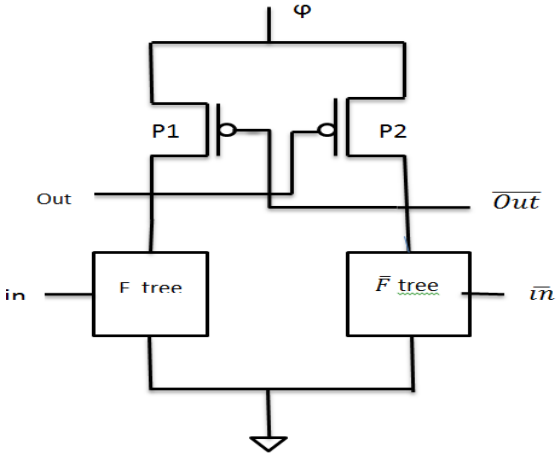

Figure.2: ECRL logic circuit

In above figure, let us assume in isat high&inbar is low. As power supply ramps up from 0 to V_{DD}, 'out' remains at a ground level &outbar follows power clock (ϕ) through P2.When power clock reaches V_{DD}, out &outbar holds the valid logic levels & during the hold phasethese values are maintained and are used for the evaluation of the next stage. As ϕ ramps down from V_{DD} to ground, outbar returns its energy to power clock i.e. delivered charge is recovered back to the power supply.[5]

3.2 POSITIVE FEEDBACK ADIABATIC LOGIC(PFAL)

PFAL consists of 2 cross-coupled inverters as latch known as sense amplifier which drives the two complementary outputs& the logic function N_F and its compliment are realized using NMOS networks which is connected parallel to PMOS.[11] One of the logic blocks connects the desired input to the power clock through a low resistance path and on the same time the other network provides a very high resistance path in between the power clock and the other output. But the inverter's down network provides the second output a conducting path to the ground. Thus one of the two outputs (either complementary or un-complementary one) is pulled up to the power clock and other down to the ground. PFAL uses four phase clocking technique to recover the charge delivered by the power supply.[7]

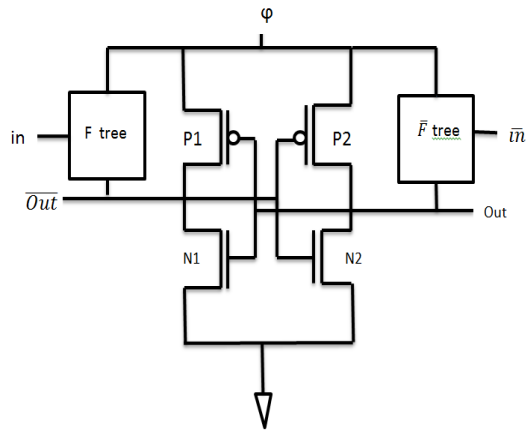

Figure.3: PFAL logic circuit

3.3 DIODE FREE ADIABATIC LOGIC (DFAL)

In this logic, no diode is used in the charging or discharging path. DFAL uses a two phase clocked split-level sinusoidal power clock supply VPC and $V\overline{PC}$to minimize the voltage difference between the current-carrying electrodes and consequently reduce the power consumption. Split level clock charges/discharges the load capacitance slightly slowly than the other adiabatic power clocks.[9] Since the efficiency of adiabatic logic circuits depends upon how slowly the load capacitance is charged or discharged so power dissipation has been minimized further.

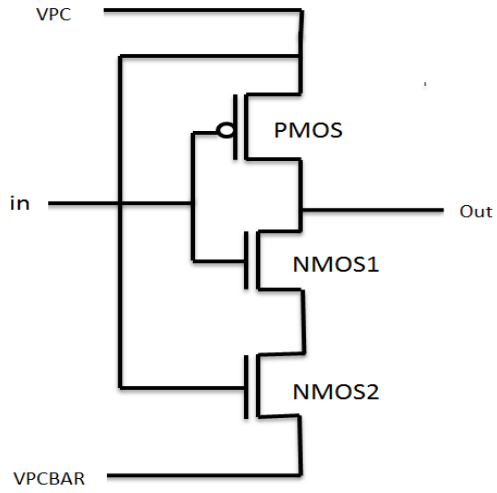

Figure.4: DFAL inverter circuit

Circuit operation is divided into two stages, evaluation and holdphase depending on the supply clock signal phases. In evaluation phase, VPC swings up while VPCBAR swings down and in the hold phase, VPC swings down and VPCBAR swings up.

In evaluation phase, PMOS tree is turned ON& load capacitancegets charged through PMOS transistor which results in High output. When NMOS tree turns ON then value at the output node gets discharged through NMOS transistor. In hold phase, NMOS tree is ON & output is Low then no transitions occur at the output.During the hold phase, dynamic switching is reduced and thus energy dissipation is also reduced.

4. CIRCUIT IMPLEMENTATION

In this paper, three adiabatic techniques (ECRL, PFAL & DFAL) & conventional CMOS logic were used to design 2:1 Multiplexer. The schematic & simulations of 2:1 Mux designed using the logic styles are shown in the figures.

4.1.Conventional CMOS 2:1 MUX

A multiplexer is a combinational circuit that selects one of the data inputs and transmits it to the output depending on the control signals. It implements the function F = A$\bar{S}$ + BS. When select(S) is Low, it outputs the signal A & when select(S) is High, it outputs the signal B.

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 5, Issue 1, January 2016

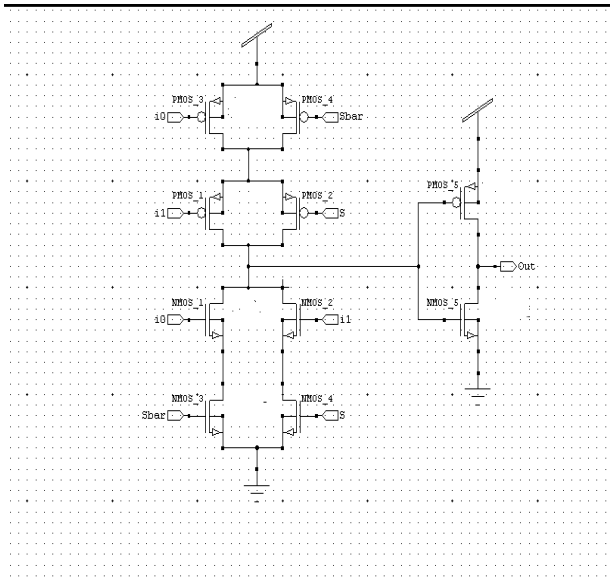

Figure.5: Schematic for 2:1 MUX using conventional CMOS

4.2 2:1 MUX using ECRL

The logic density of ECRL is more as compared to conventional CMOS that is achieved by elimination of PMOS transistors from each logic function. All functions are implemented using NMOS only, and PMOS transistors serve only as the pull-up devices. In ECRL circuits, the latch is realized using 2 cross-coupled PMOS transistors & the cascade complementary logic array is realized with a NMOS logic tree.

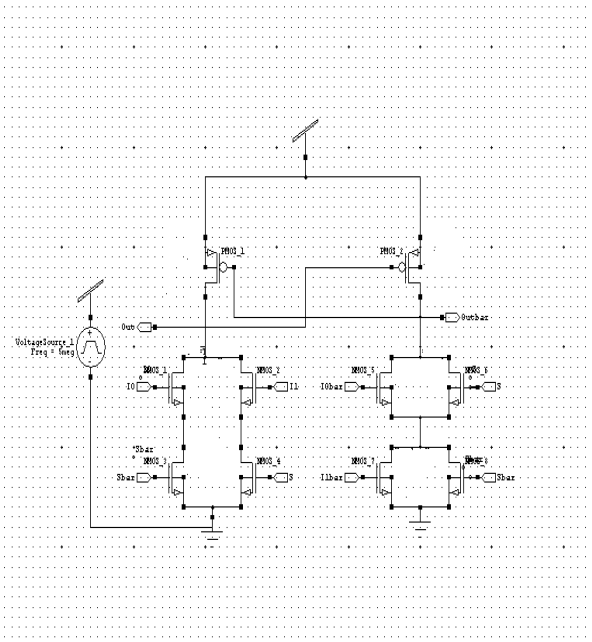

Figure.6: Schematic for ECRL inverter based 2:1 MUX.

4.3. 2:1 MUX using PFAL

The two cross coupled inverters drives the two complementary outputs of the circuit. The logic function F = A$\bar{S}$ + BS is realized using NMOS network which is connected parallel to PMOS transistor & results in the reduction of equivalent resistance of the logic network thereby reducing the power dissipation.

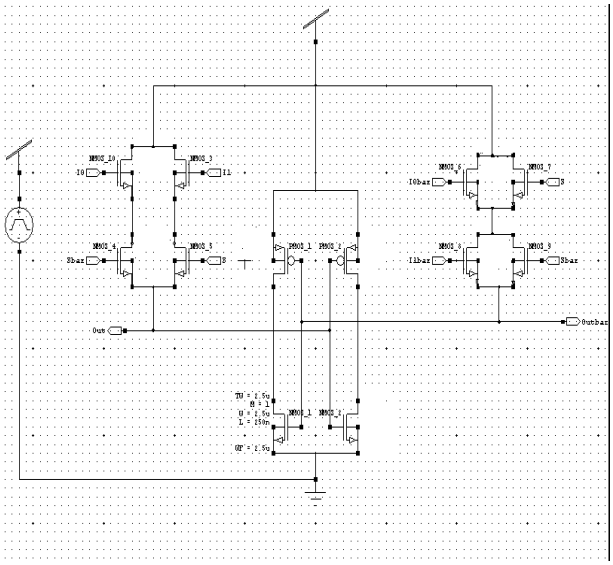

Figure.7: Schematic for PFAL based 2:1 MUX

4.4. 2:1 MUX using DFAL

Using DFAL 2:1 Mux, we can achieve low power dissipation as compared to CMOS logic design circuit.

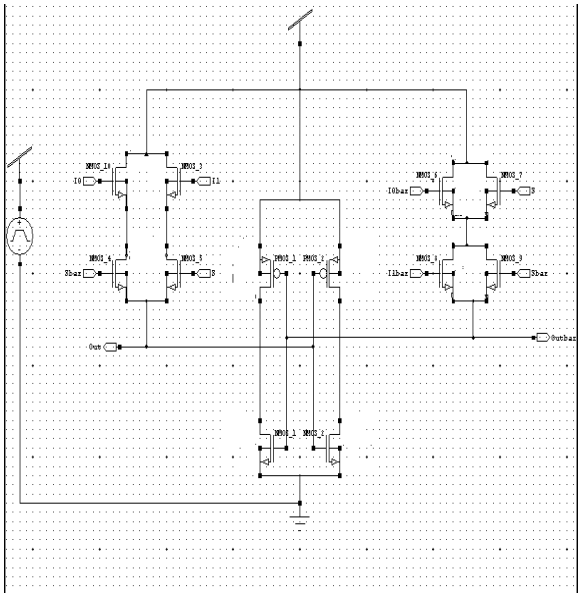

Figure.8: Schematic for DFAL 2:1 MUX

When select line is high then DFAL inverter output becomes low and select line directly gets connected to NMOS, as a result of this PMOS and NMOS transistor gets ON and In2 input comes to output.When select line is low, then DFAL inverter output becomes high and select line directly connects PMOS, so both PMOS and NMOS transistor turns on and input In1 will appear at the output.

5. SIMULATION RESULTS

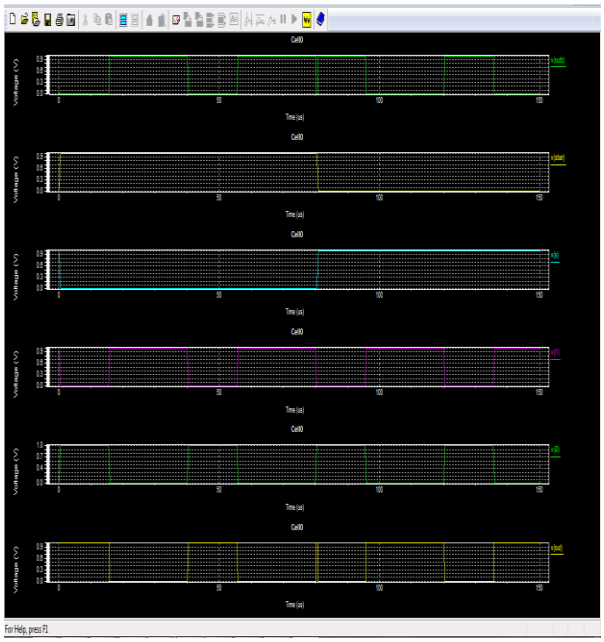

Figure.9: Simulation waveform of CMOS 2:1 MUX

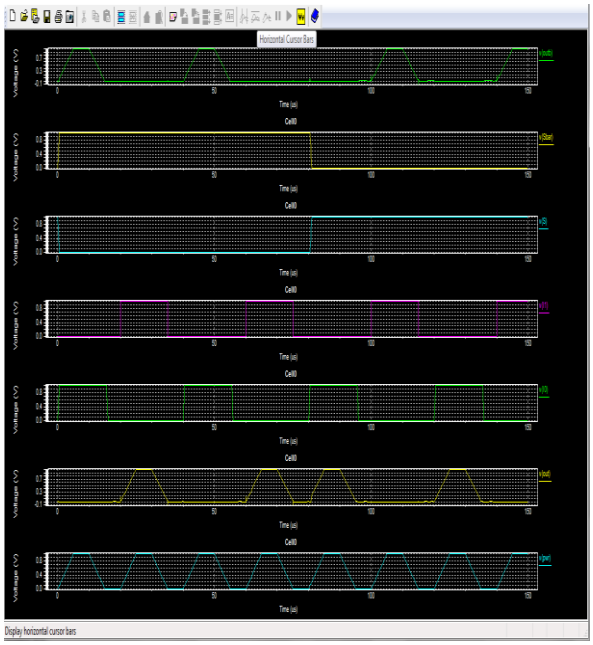

Figure.10: Simulation waveform of 2:1 MUX using ECRL

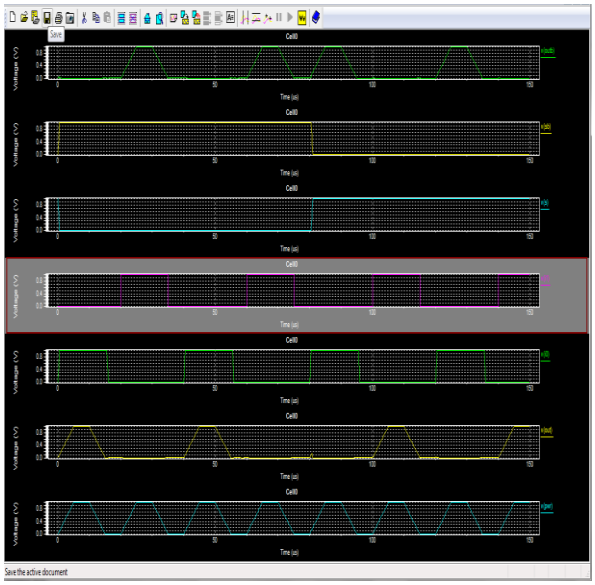

Figure.11: Simulation waveform of 2:1 MUX using PFAL**.**

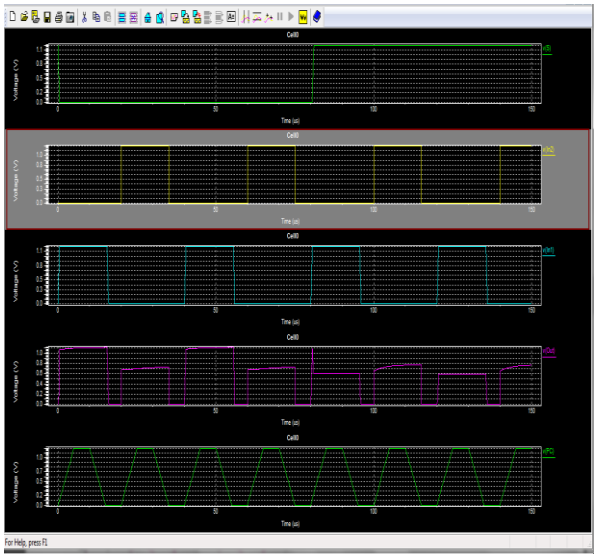

Figure.12: Simulation waveform of DFAL 2:1 MUX

6. CONCLUSION

A 2:1 Multiplexer has been implemented using various adiabatic techniques and was compared with the conventional CMOS logic. Table.1 shows the average power dissipation of ECRL, PFAL, DFAL& CMOS based 2:1 Mux at different frequencies. It was observed that the power dissipation in DFAL, ECRL & PFAL is very less as compared to CMOS based design. These adiabatic techniques can be used for low power applications over the wide range of parameter variations. Tanner EDA v14 is used for the simulation of the circuits in 90nm CMOS technology at 1V supply voltage. A 2:1 Mux designed using adiabatic techniques can further be

used in applications such as Barrel Shifters, Memory designing & other low power applications.

Frequency	CMOS	ECRL	PFAL	DFAL
15MHz	79.8nW	4.46nW	4.37nW	0.45nW
25MHz	79.8nW	4.67nW	4.82nW	0.67nW
50MHz	81.1nW	5.53nW	6.37nW	1.83nW

Table.1: Average power dissipation v/s frequency for 2:1Mux.

7. REFERENCES

[1] A.G.Dickinson and J.S.Denker, ***Adiabatic Dynamic Logic***, IEEE Journal of Solid-state Circuits, Vol. 30 No.3.

[2] J. S. DENKER, "*A Review of Adiabatic Computing"*,IEEESymposium Low Power Electronics, SanDiego,1994.

[3] RobertoSaletti& Antonio Blotti ,"*Ultralow Power Adiabatic Circuit Semi-Custom Design*", IEEE Transactions on VLSI system, vol.12, November 2004.

[4] W. C. Athas, J.Svensson, J G Koller, NestorasTzartzanis and E. Chou "*Low Power Digital system based on Adiabatic-Switching Principles*." *IEEE Trans VLSI systems*, Vol. 2, pp. 398-407, Dec 1994.

[5] A.P. Chandrakasan and R. W. Brodersen, *Low-power CMOS digital design, Kluwer Academic*,1995.

[6] Y. Moon and D. K. Jeong, "*An Efficient Charge Recovery Logic Circuit*," IEEE JSSC Vol.31, No. 04, pp. 514-522, 1996.

[7]. Manoj Sharma &ArunKumar,"*Design and Analysis of mux using adiabatic technique ECRL And PFAL",* International conference on advanced computing and communications, 2013.

[8] Vetuli, A., S.D. Pascoli and L.M. Reyneri, 1996. Positive feedback in adiabatic logic Electronics Letters,September 1996 Vol. 32 No. 20pp: 1867-1869.

[9] ShipraUpadhya, R.A. Mishra, R.K. Nagari,andS.P.Singh, "*Diode free adiabatic logic circuits",* Hindawani published corporations ISRN Electronics Volume 2013.

[10] Athas, W.C., Svensson, L., Koller, J.G., "*Low power digital systems based on adiabaticswitching principles"*. IEEE Transactions on VLSI SystemVol. 2,Dec.1994,pp.398-407.

[11] KanchanaBhaaskaran V.S, "*Asymmetrical PositiveFeedback Adiabatic Logic for Low Power and Higher Frequency"*,2010 International Conference on Advances inRecent Technologies in Communication andComputing.