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Various method analyses for optimizing Noise Tolerance for Dynamic CMOS Logic by Layout Designing.

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Abstract: Dynamic CMOS circuits are drastically used in high-performance very large-scale integrated (VLSI) systems. Nevertheless, they suffer from restrictions such as noise tolerance, charge leakage and power consumption. Noise in dynamic CMOS circuit has become an essential design challenge with the increasing impact of process variations on design performance and technology scaling .In this paper noise tolerance of dynamic logic can be improved which is demonstrated through simulation and analysis by using proposed methodology namely(1)node point insertion technique for raising sourse voltage,(2)improving noise immunity using(a)Weak always-on keeper(b)feedback keeper(3)Feed-through logic by precharging internal nodes (4) Stacking technique.

Keywords: Node point insertion technique; Weak always-on keeper; Feedback keeper; Feed-through logic by pre-charging internal nodes; Stacking technique.

INTRODUCTION

I. Node Point Insertion Technique for raising Source Voltage:

One effective method to improve noise tolerance against each internal and external noise is to extend the supply voltage of the transistors within the pull-down network. Since the gate voltage needs to be bigger than the total of the supply voltage and threshold voltage once a transistor is turned on, higher supply voltage directly ends up in increased gate activate voltage. Moreover, because of the body effect, junction transistor threshold voltage is increased once the supply voltage rises. This conjointly contributes to rising gate turn-on voltage. The PMOS pull-up technique shown in Fig.1(a) employs a PMOS semiconductor device (transistor) at node N2 forming a resistive voltage divider with the bottom clock controlled transistor. One major downside of this system is that the DC power consumption within the resistive voltage divider. Moreover, since the voltage level at the dynamic node S will never get below the voltage at node N2, the voltage swing at node S isn't rail-to-rail. Once the size of the PMOS pull-up junction transistor is giant in an attempt to sharply raise gate noise immunity, the gate output may additionally not have a rail-to-rail swing.

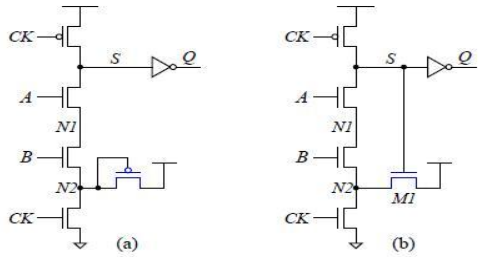

Fig.1. Schematic of source voltage at node n11 and n12

An enhanced methodology, shown in Fig.1 (b), employs a pull-up junction transistor with feedback management. Here NMOS junction transistor M1 is employed to drag up the voltage of an internal node. The gate of the pull-up junction transistor is connected to the dynamic node of the domino gate. This style permits the pull-up junction transistor to be shut off once the voltage of the dynamic node goes low; therefore, the dynamic node S undergoes rail-to-rail voltage swing. Also, the DC power consumption drawback is partly solved. It happens solely under certain input combinations that don't activate the pull-down

network

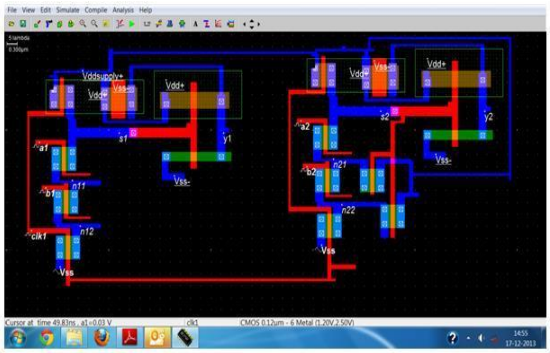

Fig.1.1 source voltage at node n11 and n12

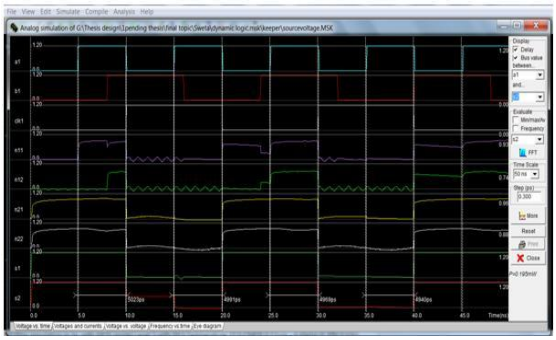

Fig.1.2.Timimg Simulation of source voltage at node n11 and n12.The simulation is done on NAND logic gate. The noise level at node n11 and n12 is observed to be suppressing at node n21 and n22.

II. Improving noise immunity of dynamic logic gates using keeper.

- **Weak always-on keeper**
- **Feedback keeper**

The keeper provides a tiny quantity of current from the power-supply network to the dynamic node of a gate in order that the charge hold on within the dynamic node is maintained. Within the original domino dynamic logic work, the gate of the PMOS keeper is tied to the bottom, Therefore, the keeper is often on. Afterward, feedback keepers, shown in Fig.5.17 (b), became additional wide used for the reason that they eliminate the potential DC power consumption downside utilizing the always-on keeper within the evaluation stage of domino gates.

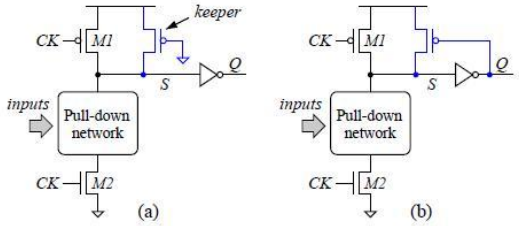

Fig.2.Improving noise immunity of dynamic logic gates using keeper. (a) Weak always-on keeper (b) Feedback keeper

III .Feed-through Logic by pre-charging Internal Nodes: With big pull-down network of complex dynamic logic gates, charge sharing between the internal nodes in the pull-down network and the dynamic node typically leads to false gates switching. An easy yet effective technique to prevent the charge sharing problem is to pre-charge the internal nodes in the pull-down network alongside pre-charging the dynamic node S. Take for an instant3-input dynamic AND gate by means of this technique is shown in Fig.3. Once all internal nodes are pre-charged, this method is able to eliminate the charge sharing drawback at the price of using a big number of pre-charge transistors and then the augmented load capacitance on the clock net. Partial pre-charge, as shown in Fig.3 (b), has also be been utilized in design practice as a trade-off between overheads in chip area and in clock load and noise immunity.

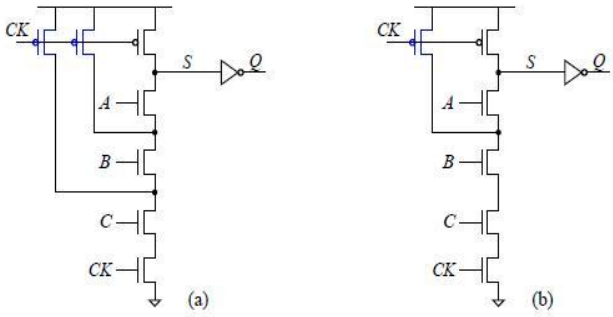

Fig.3.Pre-charging internal nodes (3-input AND gate). (a) Pre-charge all internal nodes. (b) Partial pre-charge

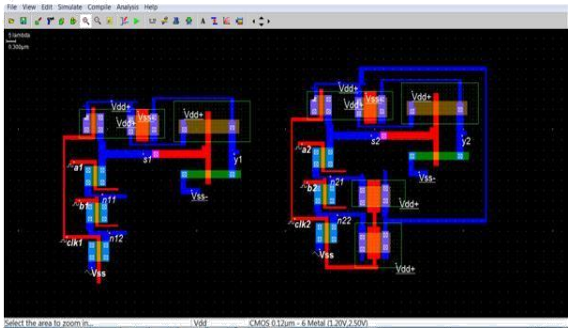

Fig.3.1.Precharging internal nodes (3-input AND gate). Pre-charge all internal nodes.

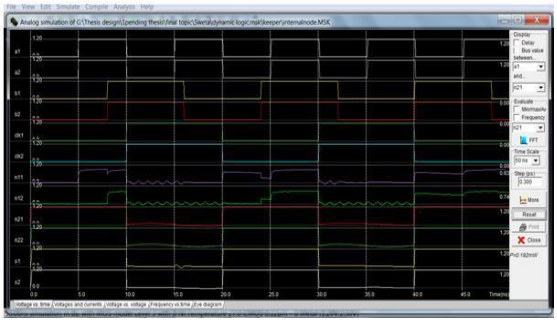

Fig.3.2.Simulation of Pre charging internal nodes (3-input AND gate). Pre charge all internal nodes.

IV. Stacking Technique: One of the techniques to reduce leakage power is to stack the transistors. Stacking results in reduction of sub threshold leakage current when two or more transistors are turned off together.

Proposed logic layout:

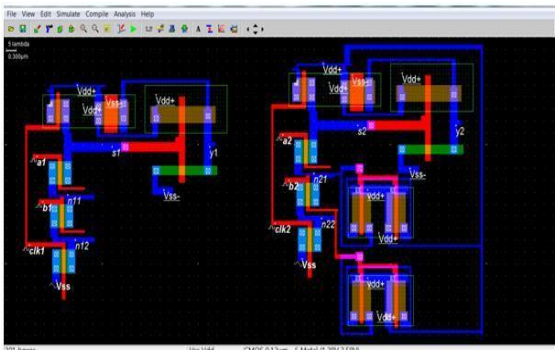

Fig.4.1. Propose logic layout in our design by transistor stacks method.

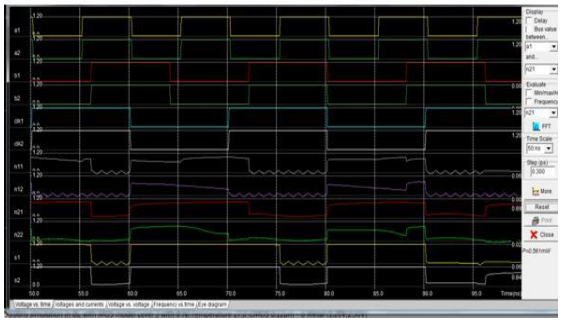

Fig.4.2.Simulation of Propose logic layout in our design by transistor stacks method.

Table.1. Parametric analysis of Noise level

Technique	Number of transistor		Maximum Ids mA		Power dissipation uW		Noise level V	
	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Source voltage at node With NMOS	7	9	0.426	0.475	115	98	0.2	0.04
Source voltage at node With PMOS	7	9	0.261	0.353	93	228	0.2	0.03
Feedback keeper	6	8	0.374	0.509	0.32	96	0.2	0.04
Precharge all internal nodes	7	9	0.432	0.573	115	96	0.2	0.03
Propose logic layout	7	11	0.432	0.616	95	391	0.2	0.02

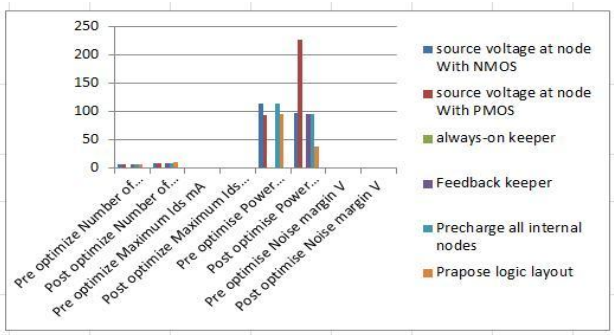

Fig.5.Graphical analysis of Noise level of table1.

Conclusion: From the above findings we conclude that keeper clocking technique is showing best results in terms of noise immunity while for low power and less delay Feed through logic is better at both deep submicron technologies. Also to improve noise immunity of the dynamic logic circuits node point insertion Clocking technique can be used as an effective technique. Although, other parameters such as power and delay of Delayed Clocking technique is more than that in Feed through logic but if we want noise L tolerant dynamic circuits then Delayed Clocking technique is best choice

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