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Design and Analysis of Convolutional Codes over Channel for Different Algorithm

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ABSTRACT: Any general communication that is of digital one is source generates data bit or message or input signals are to be transmitted over noisy channel to distant user. To encode digital data before transmission through noisy or error-prone communication channels to reduce occurrence of error. Here we present CC(2,1,3) encoder which belongs to the convolutional encoder's class. Presenting two different decoding techniques based on the Viterbi algorithm Hard and Soft decision decoding techniques. In this transmitted signal is corrupted mainly by additive white Gaussian noise (AWGN) for this Convolutional encoding with Viterbi decoding is a technique that is particularly suited to a channel. Coding allows in principle to design a communication system in

the methods that are described in that paper are not realizable for practical values of code length and number of erasures. Thus, a new separation method; the rank completer is proposed, which is realizable. In the part of the research that is related to error decoding, we have proposed a modification to reliability ratio based bit flipping algorithm, which improves the BER performance with very small additional complexity. In the part that is related to error erasure decoding, we have given a new guessing algorithm that performs better than some known guessing algorithms, and a new error erasure decoder that uses the rank completer idea. Both simulation results and analytical models are used to adjust variables of the described methods. Also simulation results are utilized to compare the proposed methods with existing methods. The rank completer (and the separation of erasures from errors) is a promising method that can be further studied for error

The basic communication problem, which is given in Figure 1-1, consists of three elements; the source with information to send to the sink, the sink to receive the information sent by the source, and the noisy channel

which both, information bit rate and error rate are independently and arbitrarily specified but subject to a constraint on bandwidth. The usual measure of performance of a coded system is the average error rate that is achieved at specified signal-to–noise ratio.

For low-end devices with limited battery or computational power, low complexity decoders are beneficial. In this research we have searched for low complexity decoder alternatives for error and error-erasure channels. We have especially focused on low complexity error erasure decoders, which is a topic that has not been studied by many researchers. The separation of erasures from errors idea seemed profitable to design a new error erasure decoder, so we have also worked on this idea. However, erasure decoding. However, we have shown that for already error erasure correcting methods, application of this method can degrade the BER performance of the original code. The modification that we propose for error decoders does not improve the BER performance much; however, it can be applied since it has nearly no additional complexity. The proposed error erasure decoders can be used for systems that do not require high reliability, but favor low complexity.

Index Terms—Convolutional codes, maximum distance separable (MDS) block codes, decoding, erasure channel, maximum distance profile (MDP) convolutional codes, reverse-MDP convolutional codes, complete-MDP convolutional codes, maximum distance profile (MDP) convolutional codes, reverse-MDP convolutional codes.

I. INTRODUCTION

which disrupts the information sent. The intended solution of this problem is transmission of data from source to the sink in an efficient and reliable way.

Figure 1: The communication problem

The basic communication problem introduced above has been formalized by Shannon in two separate parts; the first part deals with the information theoretical aspects of the data to be sent by the source, and the second part deals with the reliable transmission of this data through the noisy channel. The structure is given in Figure 1. There are four new blocks that have two different functions as stated before; the source encoder/decoder and the channel coder/decoder. Source encoder removes the redundancy of the source information, while the source decoder retrieves the full source information from the encoded data. Error correction coding is essentially a signal processing technique that is used to improve the reliability of communication system in digital channels. There are many efficient error correcting codes. Historically, these codes have been classified in to Block codes and Convolutional codes. On the other hand, channel encoder introduces redundancy for reliable transmission of the data through the noisy channel (or storage medium), and the channel decoder retrieves -of course depending on the capabilities of the channel encoding/decoding blocks and the noise- the source coded data from the received data. Source coding part is not explained any further in this thesis, depending on Shannon's source-channel separation theorem, which simply states that an efficient and reliable transmission is possible by dealing with source coding and channel coding separately. The distinguishing feature for this particular classification is the presence or absence of memory in the encoders for the two codes. Conceptually, encoder for the block code is a memory-less device, which maps an X-symbol input sequence in to n-symbol output sequence. Therefore, in the channel coding perspective the source and the source coding can be thought as a single large block. These blocks are shown in Figure 1 by the big dashed rectangles. Using the channel coding perspective described in the previous paragraph, the transmitter part is reduced to a source that generates arbitrary number information symbols from an alphabet, and a channel encoder encodes k of these symbols and produces an output of length n, where $n-k$ is the redundancy of the channel encoder. In the channel some of these n encoded symbols are corrupted due to noise which might cause errors and/or erasures. The effect of errors occurring during transmission is reduced by adding redundancy to the data, prior to transmission in a controlled manner. The redundancy is used to enable a decoder in the receiver to detect and correct errors. The Binary Symmetric Channel (BSC) is completely described by the transition probability p. A symbol is called erroneous if its value is changed through the channel, and erased if no value or an erasure flag is received for that symbol. In the receiver, the received symbol sequence, which has length n is decoded to the k symbols that is closest to the received sequence. The term "closest" might be in the sense of maximum likelihood, Hamming distance, etc. depending on the type of the decoder. The majority of coded digital communication systems employ binary coding with hard decision decoding. But its use prior to decoding causes an irreversible loss of information in the receiver. To reduce this loss, Soft decision decoding is used.

The usual measure of performance of a coded system is the average error rate that is achieved at a specified Signal to Noise ratio. The usual method of determining the coding gain (the amount of improvement that is achieved when a particular coding scheme is used) is to plot the probability of errors versus E_b/N_o for both coded and un coded operations and to read the difference in required E_b/N_o at a specified error rate.

Convolution coding with hard and soft decision "Viterbi Decoding" has found application in many space and satellite communication system. The different aspects of Decoders are Decoder Delay and Decoding Techniques. By using different decoding algorithms we have made plots between Probabilities of Bit Error Rate (P_e) v/s Signal to Noise Ratio (SNR).

II. RELATED WORK

In 2011 A 15.8 pJ/bit/iter Quasi-Cyclic LDPC Decoder for IEEE 802.11n in 90 nm CMOS This paper present a low-power quasi-cyclic (QC) low density parity check (LDPC) decoder that meets the throughput requirements of the highest-rate (600 Mbps) modes of the IEEE 802.11n WLAN standard. The design is based on the layered offset-min-sum algorithm and is runtime-programmable to process different code matrices (including all rates and block lengths specified by IEEE 802.11n.In 2012 Shortening design time through multiplatform simulations with a portable Open CL golden-model: the LDPC decoder case. Here Hardware designers and engineers typically need to explore a multi-parametric design space in order to find the best configuration for their designs using simulations that can take weeks to months to complete.In June-2013 Alexios Balatsoukas-Stimming analyze performance of quantized min-sum decoding of low-density parity-check codes under unreliable message storage. This paper shows the a simple bit-level error model and decoder symmetry is preserved under this model. Subsequently, the formulization corresponding density evolution equations to predict the average bit error probability in the limit of infinite block length. Also present numerical threshold results and shows that using more quantization bits is not always beneficial in the context of faulty decoders. In 2004 LDPC versus Convolutional Codes for 802.11n Application in January by Aleksandar Purkovic, Nina Burns, Sergey Sukobok, Levent Demirekler shows LDPC codes offer considerable performance advantages over the existing convolutional codes. With the proper design LDPC codes can be made flexible enough to satisfy demands of 802.11n applications.Nortel Networks In 2011 Windowed Decoding of Protograph-based LDPC Convolutional Codes over Erasure Chanels: Here consider a windowed decoding scheme for LDPC convolutional codes that is based on the belief-propagation (BP) algorithm. In this advantages of this decoding scheme and identify certain characteristics of LDPC convolution code ensembles that exhibit good performance with the windowed decoder. We will consider the performance of these ensembles and codes over erasure channels with and without memory and then show that the structure of LDPC convolution code ensembles is suitable to obtain performance close to the theoretical limits over the memory less erasure channel, both for the BP decoder and windowed decoding.

II. *LDPC codes*

LDPC codes are linear block codes, that are defined by their sparse parity check matrices. By density, we mean the ratio of the number of ones in the matrix to the number of all elements in the matrix. If for each row (or column) ratio of the number of ones to the length of that row (or column)

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is equal, then the code is called a regular LDPC code. The low-density condition can be satisfied especially for larger block lengths.

LDPC codes have been proposed by Gallager in [4] in 1960s. However, the long block LDPC codes were too complex to be implemented at that time, and the codes were largely forgotten. In 1980s Tanner has given a bipartite graph interpretation of LDPC codes with other types of codes in [5]. After Turbo codes have emerged and iterative decoding methods for large codes are designed, two groups independently rediscovered the LDPC codes in [6] and [7]. LDPC codes that has been proposed by Gallager were regular LDPC codes, that has a constant column and row in their parity check matrices. Shortly after the rediscovery of LDPC codes, a new type of LDPC codes has been introduced in [8], which are called irregular LDPC codes. This type of LDPC codes can have different density rows and columns in its parity check matrices, and they can perform better than regular LDPC codes as shown in [9]. LDPC codes are mostly represented by their parity check matrices or the corresponding Tanner graphs. Tanner graph is a bipartite graph representation for the parity check matrix of the code. Say the size of H is a $m \times n$ matrix, the m parity check (or check) nodes and n codeword (or variable) nodes correspond to two disjoint sets in the bipartite graph. An element ci of "check nodes" set is connected to an element vj of "variable nodes" set if the corresponding entry in the parity check matrix is one, $hij = 1$. Previously introduced (7,3,4) simplex code is used to show the relationship between the parity check matrix and the Tanner graph. The parity check matrix is given in (1-3) and the corresponding Tanner graph representation is given in Figure 2. An important definition about the Tanner graph is the definition of neighbor nodes, two nodes are neighbors if they are connected by an edge in the Tanner graph of the corresponding code.

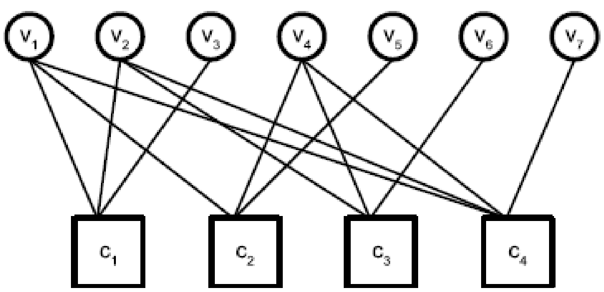

Figure 2: Tanner graph of (7,3,4) simplex code

$$H=\begin{pmatrix} 1 & 1 & 10 & 0 & 00 \\ 1 & 0 & 01 & 1 & 00 \\ 0 & 1 & 01 & 0 & 10 \\ 1 & 10 & 10 & 0 & 1 \end{pmatrix} \qquad \ldots(1\text{-}3)$$

To understand why LDPC codes perform so well, Shannon's important argument about transmission on noisy channels should be taken into account. The argument states that assigning very large block codes randomly to every message, it is possible to reach the limit for nearly error-free communication which is called the Shannon limit. Therefore if very large block codes can be decoded in a feasible time, we can reach the limit set by Shannon in 1940s. The sparse parity check matrices of LDPC codes combined with iterative decoding techniques has opened the way for decoding of large block codes and made it possible to come real close to Shannon bounds.

A. Error Control For Data Communication

In digital communication system, error detection and error correction is important for reliable communication. Error detection techniques are much simpler than forward error correction (FEC). But error detection techniques have certain disadvantages. Error detection pre supposes the existence of an automatic repeat request (ARQ) feature which provides for the retransmission of those blocks, segments or packets in which errors have been detected. This assumes some protocol for reserving time for the retransmission of such erroneous blocks and for reinserting the corrected version in proper sequence. It also assumes sufficient overall delay and corresponding buffering that will permit such reinsertion. The latter becomes particularly difficult in synchronous satellite communication where the transmission delay in each direction is already a quarter second. A further drawback of error detection with ARQ is its inefficiency at or near the system noise threshold. For, as the error rate approaches the packet length, the majority of blocks will contain detected errors and hence require retransmission, even several times, reducing the throughput drastically. In such cases, forward error correction, in addition to error detection with ARQ, may considerably improve throughput. Forward error correction may be desirable in place of, or in addition to, error detection for any of the following reasons:

(1) When a reverse channel is not available or the delay with ARQ would be excessive.

(2) The retransmission strategy is not conveniently implemented.

B. Channel Coding

It is known that noise-immunity is one of the basic attributes of information transmission systems. Since errors are possible in communication channels during the data transmissions we must apply error-correcting codes to combat these errors [1]. The purpose of forward error correction (FEC) is to improve the capacity of channel by adding some carefully designed redundant information to the data being transmitted through the channel. The process of adding this redundant information is known as channel coding. The various building blocks of digital communication system are channel encoder, binary modulator, channel, demodulator, detector and channel decoder as mentioned in figure 1

C. Block Codes:

Early attempts at designing error control techniques were based on block codes. For every block of **k** information bits, **n-k** redundant parity-check bits are generated as linear (modulo-2) combinations of the information bits and transmitted along with information bits as a code of rate **k/n** bits/symbol. These can be generated by means of a linear feedback shift register encoder. Error detection can be easily implemented with any parity-check block code. At the decoder the received information bits are re-encoded into parity checks and compared bit-by-bit with the received redundant parity check bits. If any discrepancy occurs, a block error is declared. Shift register encoders and decoders in the form of a cyclic redundancy code can most easily implement this technique, called syndrome decoding. Some of the commonly used block codes are Hamming Codes, Golay Codes, BCH Codes, and Reed Solomon Codes. Emphasis in the last decade has turned to convolutional codes. Convolutional encoder may be viewed as a digital filter, whose output is the convolution of the input data and the filter impulse response. In almost every application, convolutional codes outperform block codes for the same implementation complexity of the encoder-decoder [4].

III. CONVOLUTIONAL CODING

The basic objective of the channel coding is to increase the resistance of the digital communication system to channel noise. Convolution code is basically a finite state machine. Convolutional codes are widely used to encode digital data before transmission through noisy or error prone channels. During encoding, k input bits are mapped to n output bits to give rate k/n coded bit stream. The encoder consists of a shift register of K stages, where K is described as the Constraint length of the code.

Convolutional encoder plays an important role in the development of modulation schemes for wireless systems. Convolutional codes add a structured redundancy to the information source that mitigates the effect of the random noise corrupting the data stream. Convolutional codes perform better in the marginal regions of Bit Error Rates {10^ (-2) - 10^ (-4)} than block codes such as Reed-Solomon. Since voice communication systems performs satisfactory in this range and are often designed for those Bit Error Rates. Convolutional codes are a common element in wireless systems.

Convolutional codes gain their name from the fact that the information source is mathematically convolved with the impulse response of the code. This impulse response is defined by generator function for a particular code. There is a generator function for every output of a Convolutional encoder. These Convolutional Encoders are physically constructed by using shift registers with taps determined by the generator functions as shown in the figure 2. The rate of the encoder is defined as the ratio of inputs to the outputs. The number of taps on the shift register determines how many of the output bits are influenced by the input bits. The number of influenced output bits is called the Constraint Length. To avoid confusion, in practice the constraint length of an encoder is usually taken to the number of memory elements in the shift register plus one.

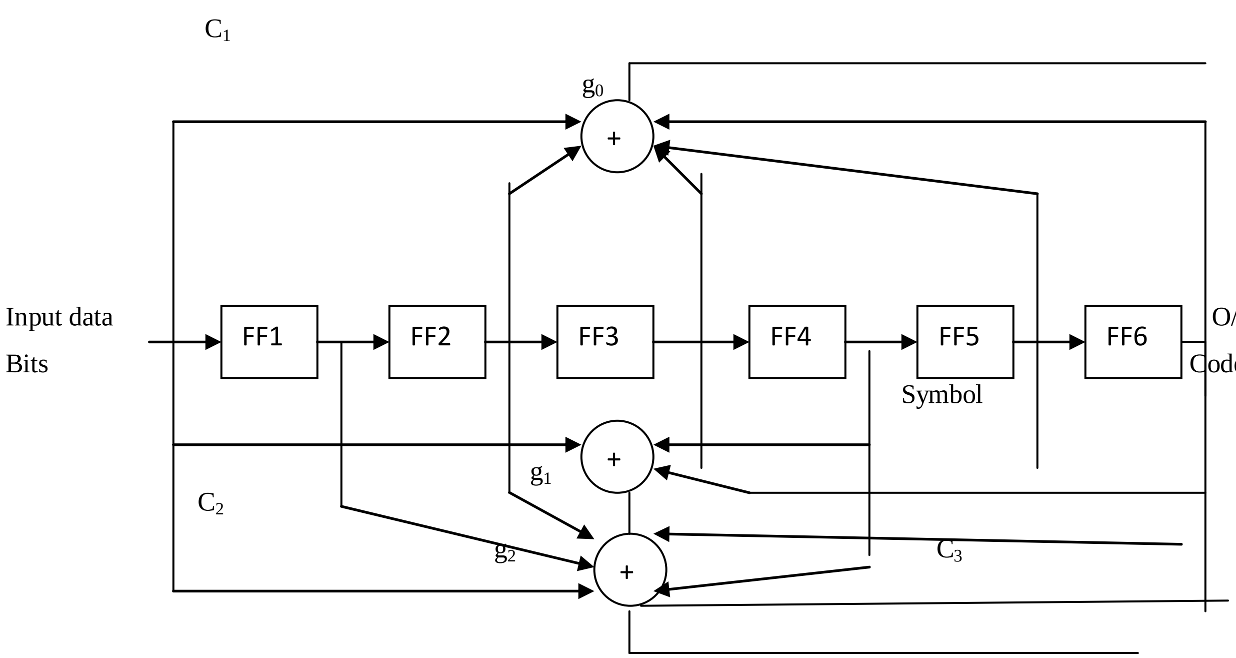

Fig 3: Convolutional Encoder

Convolutional codes can be used when bandwidth is more constrained, and allow for a more modest expansion of bit rate from input to output.

We give an example below, where there are two output bits for each input bit. Such a code is said to have a rate ½. More generally, such codes can produce **m**-tuple of output bits for each **k**-tuple of input bits but arbitrary integers **k<m**. These are said to have rate **k/m**.There is another difference between a convolutional code and a discrete time filter, the inputs and outputs for a convolutional code are binary and the addition is modulo-2.

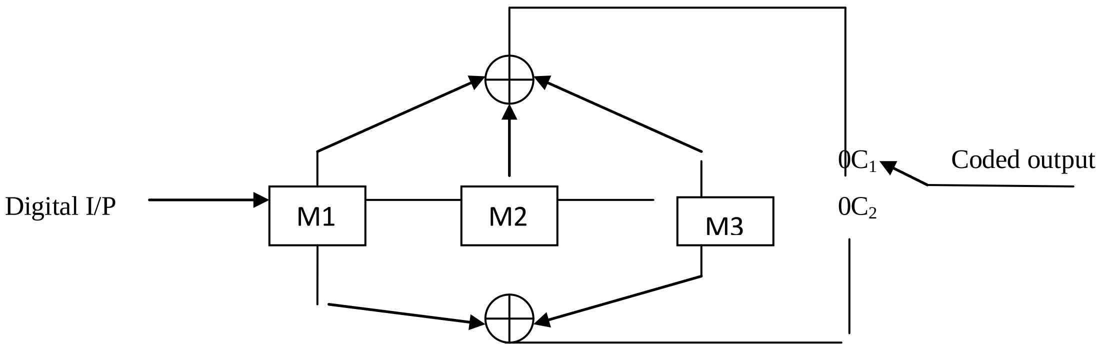

Fig 4: Convolutional Encoder with 3 shift registers

A. Code Generation

A Convolutional code is generated by combining the output of k- shift registers through employment of EXCLUSIVE-OR logic summers. Such an Encoder is illustrated in fig3. For the case k=3 and v=2, here M1 through M3 are 1-bit storage devices such as flip-flops. The output v_1 and v_2 of adder are

$$v_1=s_1\oplus s_2\oplus s_3$$
$$v_2=s_1\oplus s_3$$

Thus the number of code bits is v times the number of message bits, v being the number of commutator segments. Accordingly, also the rate of code is 1/v.If number of bits in the message stream is L, the number of bits in output code is v(L+K). Generally L is large number while K is relatively small. Hence

$$v(L+K)\cong vL.$$

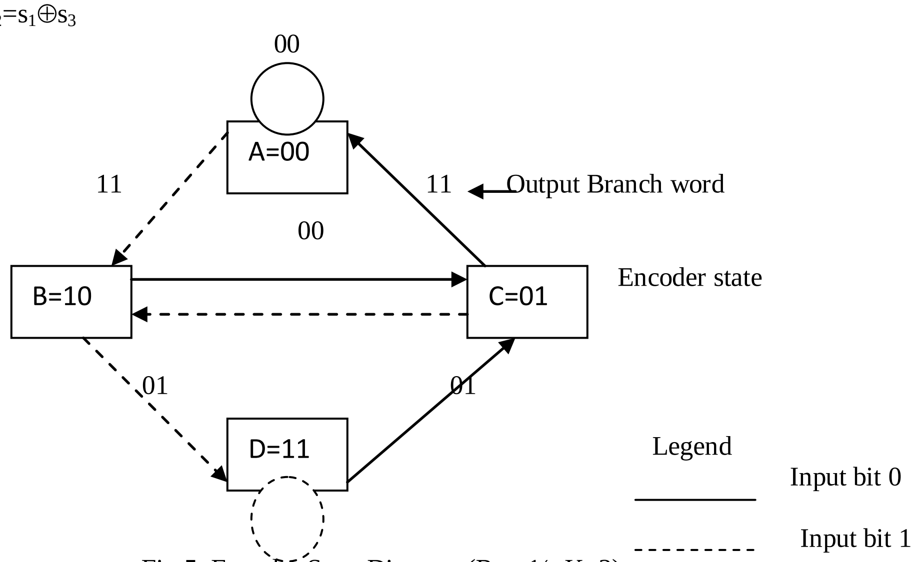

Fig.5: Encoder State Diagram (Rate ½, K=3)

IV. DECODING ALGORITHS FOR CONVOLUTIONAL CODES

The Decoding of the convolution code can be done by various decoding techniques; Viterbi algorithm is one of the practical techniques. In the absence of noise, the code word will be received as transmitted, hence simple to reconstruct the original message. The maximum likelihood decoding technique was given by Forney, he was the first to point out that the Viterbi algorithm can be used to produce the maximum likelihood estimate of the transmitted sequence over a band-limited channel with inter-symbol interference

A. The Viterbi Algorithm

The equivalence between maximum likelihood decoding and minimum distance decoding for a binary symmetric channel implies that a convolutional code may be decoded by choosing a path in the code tree whose coded sequence differs from the received in the fewest number of places. Since a code tree is equivalent to a trellis, trellis representation is considered. the reason for preferring the trellis over the tree is that the number of nodes at any level of the trellis does not continue to grow as the number of increasing message bit increases; rather, it remains constant at $\mathbf{2^K-1}$, where K is the constraint length of the code.

4.3 Types of Viterbi Decoding:

In order to realize a certain coding scheme a suitable measure of similarity or distance metric between two code words is vital. The two important metrics used to measure the distance between two code words are the Hamming distance and Euclidian distance adopted by the decoder depending on the code scheme, required accuracy, channel characteristics and demodulator type.

4.3.1 Hard decision decoding

In the hard-decision decoding, the path through the trellis is determined using the Hamming distance measure. Thus, the most optimal path through the trellis is the path with the minimum Hamming distance. The Hamming distance can be defined as a number of bits that are different between the observed symbol at the decoder and the sent symbol from the encoder. Furthermore, the hard decision decoding applies one bit quantization on the received bits.

4.3.2 Soft decision Viterbi decoding:

Soft-decision decoding is applied for the maximum likelihood decoding, when the data is transmitted over the Gaussian channel. On the contrary to the hard decision decoding, the soft-decision decoding uses multi-bit quantization for the received bits, and Euclidean distance as a distance measure instead of the hamming distance. The demodulator input is now an analog waveform and is usually quantized into different levels in order to help the decoder decide more easily. A 3-bit quantization results in an 8-ary output [11, 14].

4.4 Limitation of Veterbi decoding:

When a binary convolutional code with k=1 and constraint length K is decoded by means of Vetebi Algorithm, there are 1 2K− states. Convolutional code in which k bits are shifted at a time into 29 the shift register with **K** stages generates a trellis that has (1) 2 k K− states. Consequently, the decoding of such a code by means of VA requires keeping track of (1) 2 k K− surviving paths and (1) 2 k K− metrics. At each stage of the trellis, there are k 2 paths that merge at each node. Since each path that converges at common node requires the computation of a metric, there are k 2 metrics computed for each node. Of the k 2 paths that merge at each node, only one survives and this is the minimum distance path. Thus the number of computations in decoding performed at each stage increases exponentially with k and K. The exponential increase in computations and storage required to implement make it impractical for convolutional codes with large constraint length [2].

4.5 Performing Viterbi Decoding

The Viterbi decoder itself is the primary focus of this tutorial. Perhaps the single most important concept to aid in understanding the Viterbi algorithm is the trellis diagram. The figure 4.1 shows the trellis diagram for our example rate 1/2 K=3 convolutional encoder, for a 15 bit message.The four possible states of the encoder are depicted as four rows of horizontal dots. There is one column of four dots for the initial state of the encoder and one for each time instant during the message. For a 15 bit message with two encoder memory flushing bits, there are 17 time instants in addition to t=0,which represent the initial condition of the encoder. The solid lines connecting dots in the diagram represent state transitions when the input bit is zero. The states of the trellis that are actually reached during the encoding of our example 15 bit message.

The encoder input bits and output symbols are shown in the diagram. The two-bit numbers labeling the lines are the corresponding convolutional encoder channel symbol outputs. The dotted lines represent cases where the encoder input is a zero, and solid lines represent cases where the encoder input is a one. (In the figure 4.3, the two bit binary numbers labeling dotted lines are on the left, and the two bit binary numbers labeling solid lines are in the right.)

4.6 Sequential /Fano Decoding Algorithm -

The Fano sequential decoding algorithm searches for the most probable path trough the tree or trellis by examining one path at a time. The increment added to the metric along each branch is proportional to the received bit sequence for that branch and a negative constant is also added to each branch metric. The value of the negative constant is chosen such that the metric for the correct path will increase on the average while the metric for the incorrect path will decrease on average. By comparing the metric of the candidate path with increasing threshold Fano algorithm detects and discard the incorrect paths. The principle advantage of sequential decoding is that such decoding allows the decoder to avoid the lengthy process of examining every branch of the possible 2^K possible branches of the code tree in the decoding of single message bit. In sequential decoding at the arrival of first v message bits the decoder compares these bits with the two branches diverge from the starting node. If one of the branches matches exactly with these v code bits, then the encoder follows this branch. If because of the noise, there are errors in received bits, the encoder follows the branch with less discrepancy .At the second node a similar comparison is made between the diverging branches and the second set of bits and so on at succeeding nodes.

V. SIMULATION AND RESULT OF FANO ALGORITHM

A Fano algorithm for decoding the convolutional codes of fixed code rate, fixed constraint length. While going from rate-1/2 convolutional codes, improvement in performance of Fano decoding algorithm, for all constraint lengths considered as shown in figures 7 to 10.These figure performance shows how the fano algorithm work with constraint lengths.

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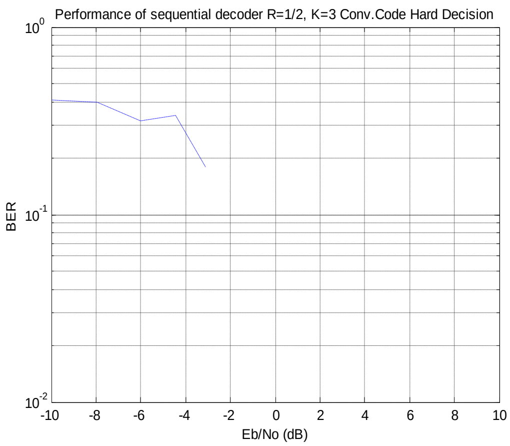

Fig.6 Performance Of Fano/Sequential Decoder For 10000 Bits Message.

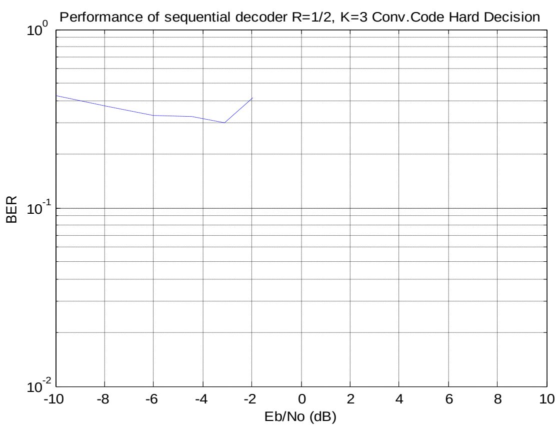

fig.7 Performance Of Fano/Sequential Decoder For 10000 Bits Message.

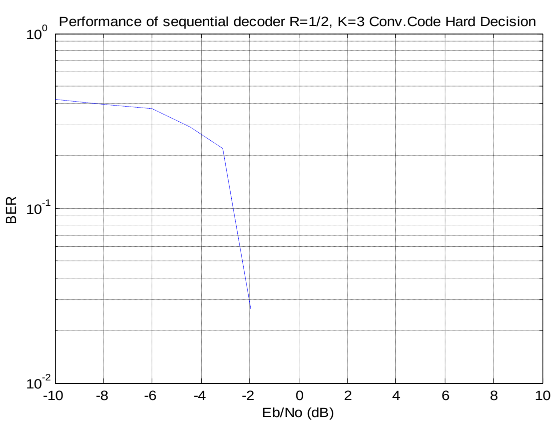

Fig.8 Performance Of Fano/Sequential Decoder For 10000 Bits Message.

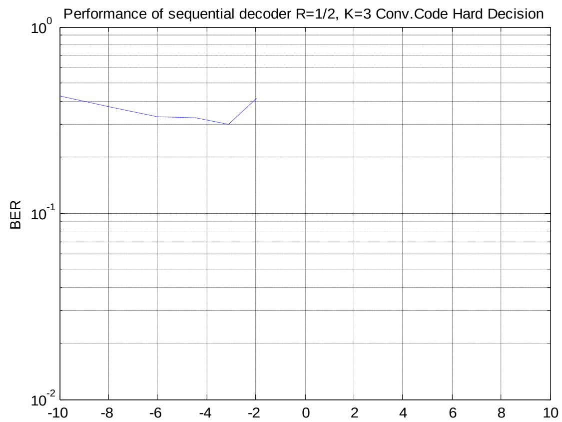

Fig9. Performance Of Fano Sequential Decoder For 10000 Bits Message

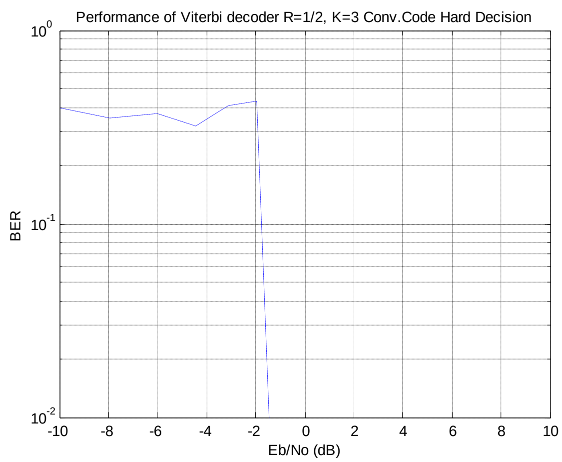

Fig10. Performance Of Viterbi Decoder For 10000 Bits Message.

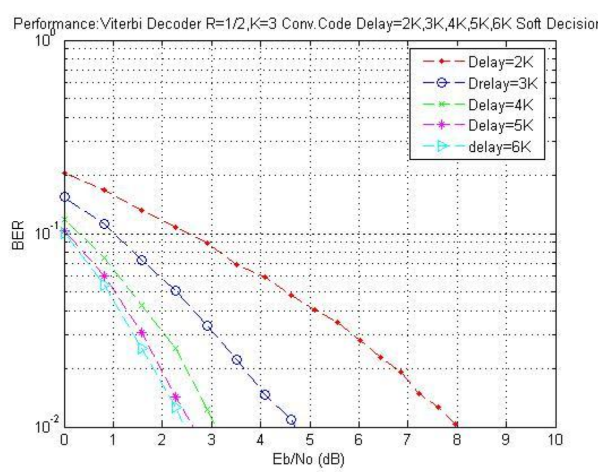

Fig11. Performance Of Vetrbi Decoder R=1/2, =3,D=2,3,4,5,6K For Soft Decision Decoding

VI. CONCLUSION

To conclude my Paper, the forward error correction technique (FEC) is a technique, particularly suited for decoding of convolutional codes with fano Decoding in AWGN channel. A fano Decoding Algorithm can show the bit error rate performance of decoding Algorithm for Soft and Hard Decision decoding Algorithm.The encoding process was demonstrated using a (2,1,3) convolutional encoder. A 3-bit input stream was encoded as an example to show the working of this encoder. A decoding process was shown using a Hard Decision Viterbi Decoding and a Soft Decision fano Decoder. Performance factors affecting the FEC technique was mentioned. These included the encoder memory size and move significant factor of SNR. Fano algorithm had a significant impact on our understanding of certain problems, notably in the theories of convolutional codes and of Intersymbol interference.

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